# 7 Data Converters

## 7.1 Analog-to-Digital Converter Principles

All analog domains interface with digital systems through Analog-to-Digital Converters (ADC). In Fig. 7.1, an analog signal from a sensor is amplified to a certain level before sampling takes place in a sample-and-hold circuit inside an ADC. The sampled analog signal is then converted into digital form and directed to the CPU for processing according to an embedded program.

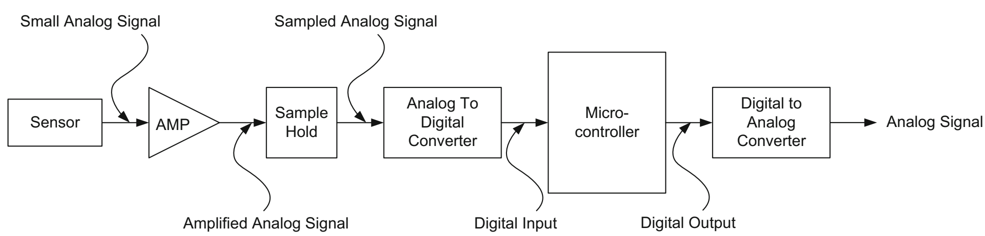


**Fig. 7.1** Typical Analog-to-Digital and Digital-to-Analog Converter data-paths

The signal resolution is an important factor to consider in an ADC design. It simply means dividing a sampled analog signal by $2^N$ number of voltage levels to represent its value where N is the number of bits in digital domain. The second important consideration is the range of analog values an ADC can capture and process.

Figure 7.2 describes the ADC resolution in a numerical example where an analog signal changes between 0 and 5 V. The bit resolution is only three bits. Therefore, ADC divides the range of an analog signal into $2^3 = 8$ levels between its maximum and minimum value, and identifies each analog level with three output bits. For example, an analog signal of 2.501 V is identified by a digital output of 100. If the analog signal increases to 3.124 V, the digital output that represents this voltage value still stays at 100. In other words, in a three-bit ADC there is no difference between 2.501 and 3.124 V in terms of their digital representation. The


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0.625 V step size is the natural occurring error in a three-bit ADC, and it can be reduced only if the number of bits in the ADC is increased. In general, increasing the number of ADC bits by one halves the error. Therefore, designing a four-bit ADC instead of a three-bit ADC reduces the quantization error by 0.3125 V.

Reference voltage is generally determined by the maximum voltage level of the analog signal, and it is used to calculate the step size. In this three-bit ADC example in Fig. 7.2, the reference voltage is 5 V because the amplified analog voltage at the input of the ADC is limited not go beyond 5 V.

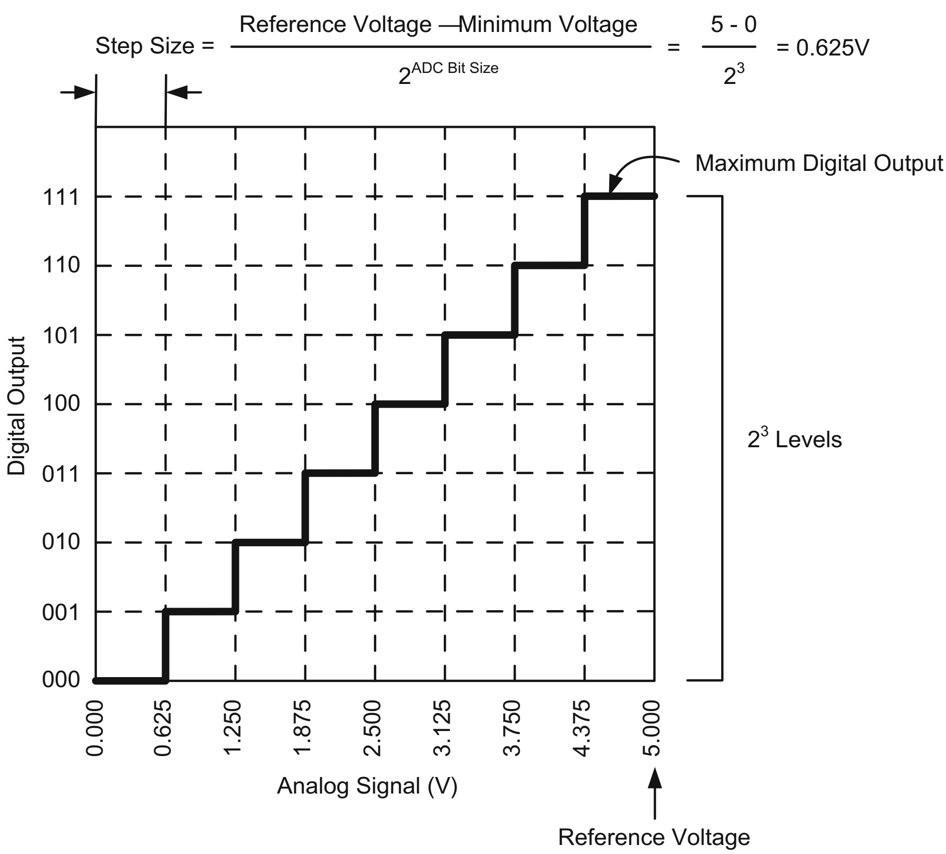



**Fig. 7.2** Input-output description of a three-bit ADC

ADC samples non-periodic analog signals in regular time intervals as described in Fig. 7.3. The time interval between sampling points is called the sampling period. The sampling period is adjusted according to the processing speed of the ADC in order to generate accurate digital outputs.

Once sampled, the analog voltage at the input of an ADC is held steady throughout the sampling period while the conversion takes place as shown in Fig. 7.4. The shape of the converted signal may be quite different from the original analog signal due to the ADC resolution and the time duration between samples. In a three-bit ADC, sampling takes place

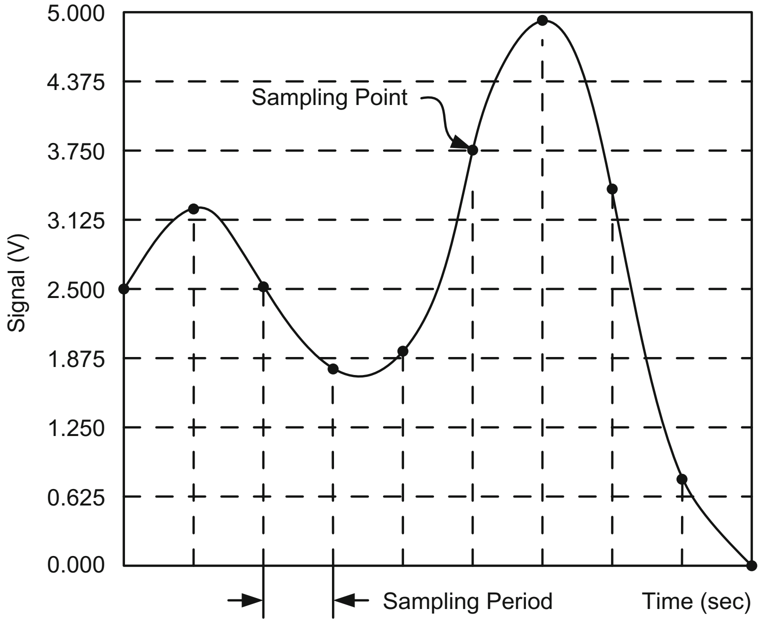



**Fig. 7.3** Sampling a continuous analog signal

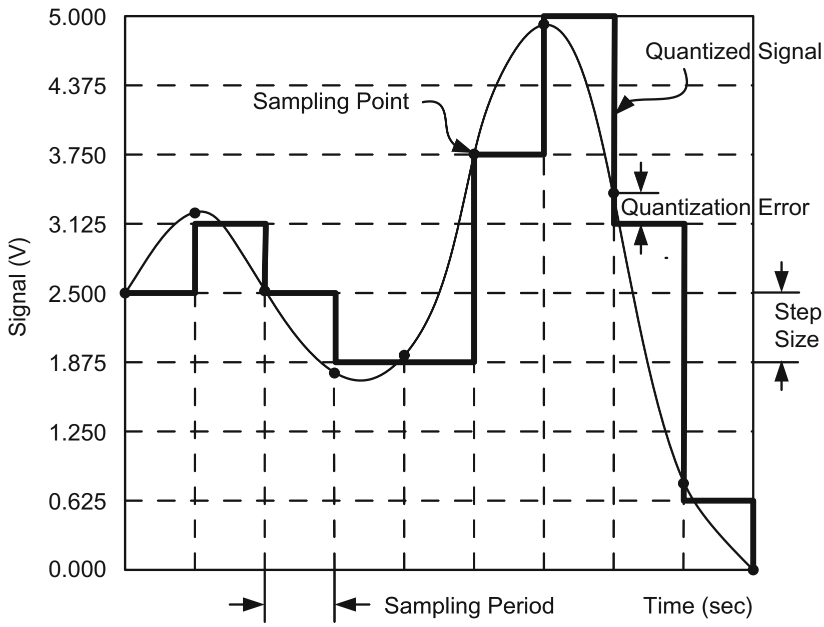



**Fig. 7.4** Sampling period, hold concept and regeneration of an analog signal

in 0.625 V increments. Therefore, each sampling point becomes subject to a dynamic quantization error which changes between 0 and 0.625 V. For example, a three-bit ADC samples 3.4 V according to its closest sampling level of 3.125 V, and produces a 0.275 V error. Arbitrary signals that change with a frequency faster than the sampling frequency are subject to much larger dynamic errors. When converted back to their analog form, these signals show large deviations from their original shapes.

## 7.2 Sample and Hold Principle

A basic sample-and-hold circuit consists of an NMOS transistor and a capacitor as shown in Fig. 7.5. The control input simply turn on an N-channel MOSFET for a short period of time, called sampling width, during which the analog voltage level at the input is stored on the capacitor. When the transistor is turned off, this analog value is held constant until the next sampling point.

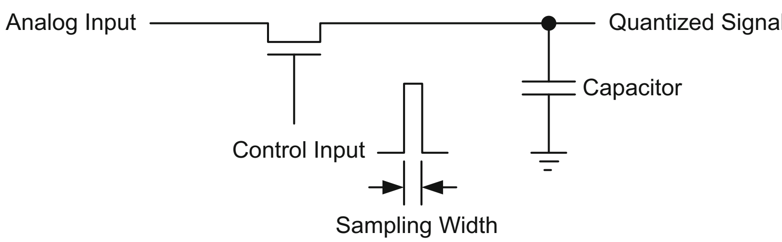



**Fig. 7.5** A typical sample-and-hold circuit

## 7.3 Flash Type Analog-to-Digital Converter

The simplest ADC is the flash-type as shown in Fig. 7.6. This three-bit ADC contains $2^3 = 8$ operational amplifiers. The analog signal is applied to all eight positive input terminals. The reference voltage is distributed to each negative input terminal via a voltage divider circuit. Each operational amplifier acts as a differential amplifier and amplifies the difference between a continuously changing analog signal and the portion of the reference voltage.

Figure 7.7 describes the operation of the three-bit flash ADC and its encoder in a truth table. When the analog voltage is less than or equal to 0.625 V, only Out[0] becomes logic 1, all other outputs from Out[1] to Out[7] become logic 0. When the analog signal exceeds 0.625 V but less than 1.25 V, only Out[0] and Out[1] become logic 1, and again all others become logic 0. Higher analog voltages at the input successively produce more logic 1 levels as shown in Fig. 7.7. An encoder is placed at the output stage of all operational amplifiers to transform the voltage levels at Out[7:0] into a three-bit digital output, DOut[2:0]. The digital output is subject to an error of 0.625 V because only three bits are used for conversion.

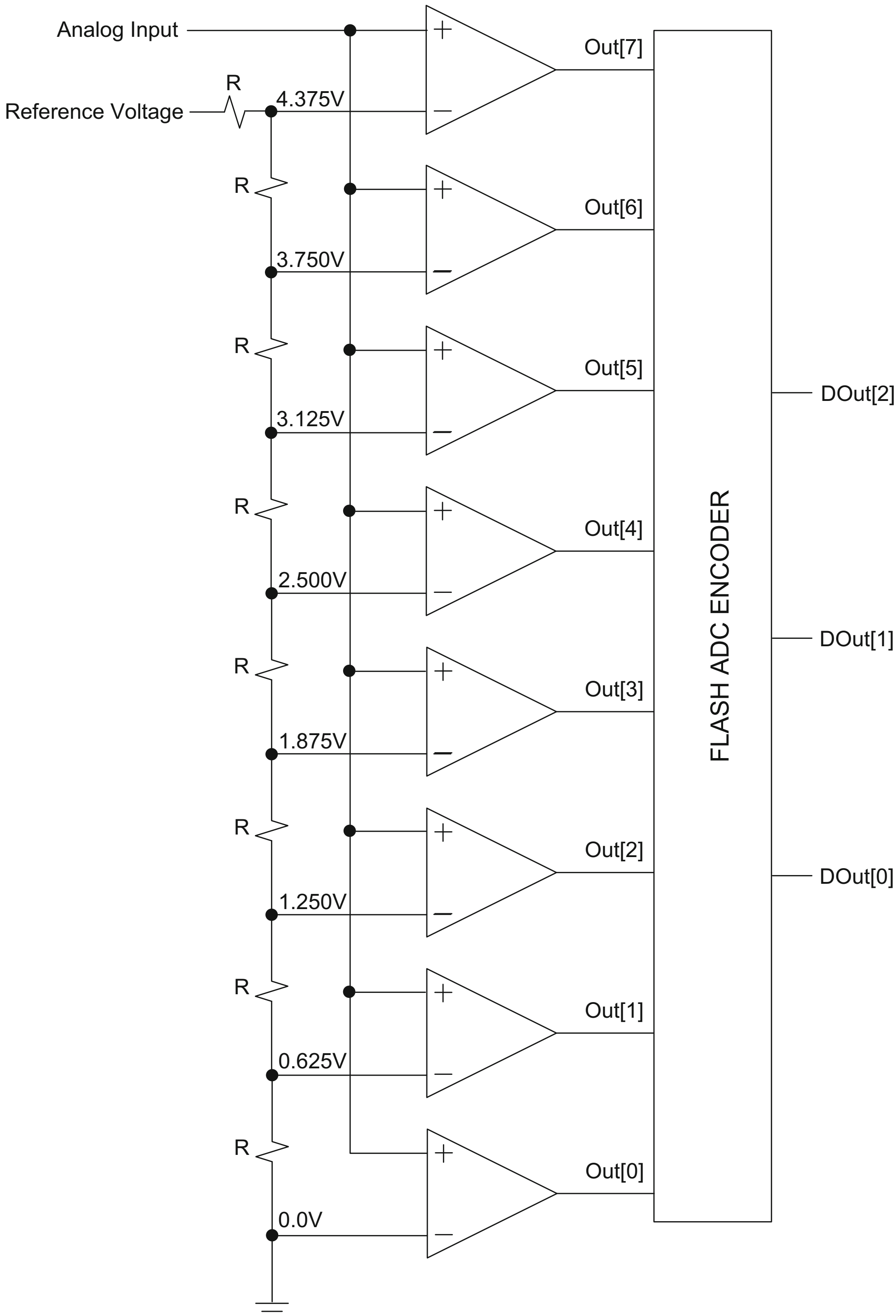



**Fig. 7.6** Typical three-bit flash ADC schematic

| Analog Input | Out[7] | Out[6] | Out[5] | Out[4] | Out[3] | Out[2] | Out[1] | Out[0] | DOut[2] | DOut[1] | DOut[0] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $0.625 > V_{IN} > 0.000$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| $1.250 > V_{IN} > 0.625$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| $1.875 > V_{IN} > 1.250$ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| $2.500 > V_{IN} > 1.875$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| $3.125 > V_{IN} > 2.500$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| $3.750 > V_{IN} > 3.125$ | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| $4.375 > V_{IN} > 3.750$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| $5.000 > V_{IN} > 4.375$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Fig. 7.7** Three-bit flash ADC truth table describing its operation

## 7.4 Ramp Type Analog-to-Digital Converter

The ramp ADC uses only a single operation amplifier, but it employs an up-counter as well as a Digital-to-Analog Converter (DAC) in a loop structure a shown in Fig. 7.8. The digital output is obtained from C[3:0] terminals, and it progressively forms within several clock periods as opposed to being almost instantaneous as in the flash ADC.

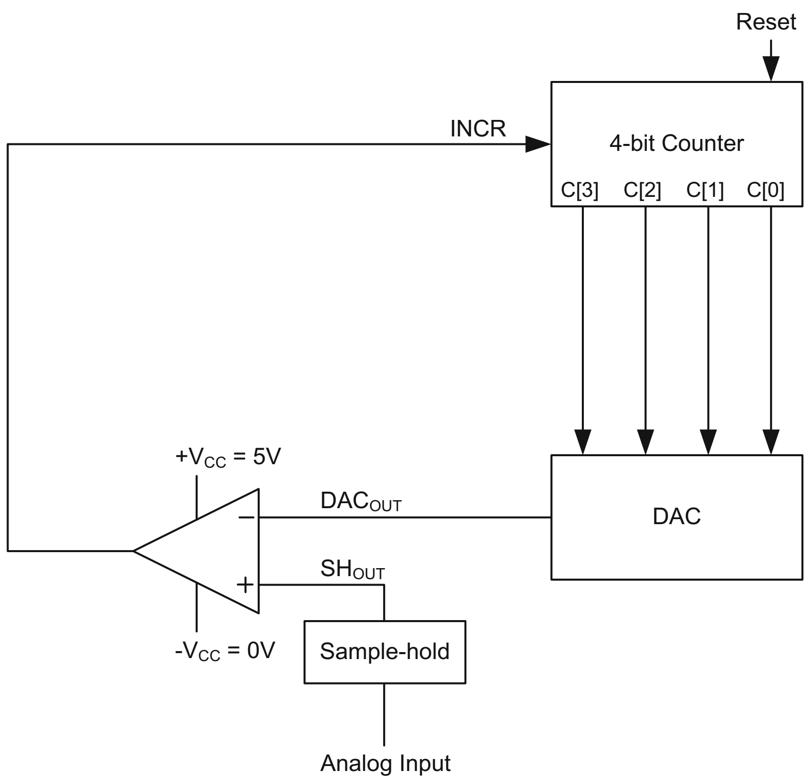



**Fig. 7.8** Typical four-bit ramp ADC schematic

The top portion of Fig. 7.9 describes the output voltage assignments of a four-bit ramp ADC using two different types of number-rounding schemes. The down-rounding scheme assigns a lower analog value for each digital output compared to the up-rounding scheme. For example, the down-rounding scheme produces a digital output of C[3:0] = 0100 for analog voltages between 1.0937 and 1.4062 V applied to its input. If the up-rounding scheme is used, the same digital output becomes equivalent to an analog voltage anywhere between 1.4062 and 1.7187 V.

The middle table in Fig. 7.9 shows how the conversion takes place if the down-rounding mechanism is used in this four-bit ADC. Prior to its operation, the four-bit up-counter is reset and produces C[3:0] = 0000. Assuming an analog voltage of 2 V is applied to the input, which must be kept constant until the conversion is complete, C[3:0] = 0000 forces the DAC output, $DAC_{OUT}$, to be 0 V according to the down-rounding scheme. Since this value is less than 2 V at the sample/hold circuit output, $SH_{OUT}$, the output of the differential amplifier, INCR, transitions to the positive supply potential of the operational amplifier, $+V_{CC}$ = 5 V, which prompts the four-bit counter to increment to C[3:0] = 0001. Consequently, the DAC generates $DAC_{OUT}$ = 0.3125 V according to the truth table in Fig. 7.9. However, this value is still less than $SH_{OUT}$ = 2 V. Therefore, the differential amplifier produces another INCR = 5 V which prompts the counter to increment again to C[3:0] = 0010. Up-counting continues until C[3:0] = 0111 or $DAC_{OUT}$ = 2.1875 V. Since this last voltage is greater than $SH_{OUT}$ = 2 V, the differential amplifier output switches back to its negative supply voltage, $-V_{CC}$ = 0 V, and stops the up-counter from incrementing further. The digital output stays steady at C[3:0] = 0111 from this point forward, representing 2 V analog voltage with a dynamic error of 0.1875 V.

The table at the bottom part of Fig. 7.9 represents the conversion steps if the up-rounding mechanism is used in this ADC. External reset still produces C[3:0] = 0000 initially. However, the DAC output starts the conversion with an increased amount of 0.3125 V instead of 0 V. The counter increments until C[3:0] = 0110, and produces 2.1875 V at the $DAC_{OUT}$ node. At this value INCR becomes 0 V, and the up-counter stops incrementing further. C[3:0] = 0110 becomes the ADC result for 2 V.

Step Size = $5/2^4$ = 0.3125V

| C[3] | C[2] | C[1] | C[0] | Down-Round(V) | Up-Round(V) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0.0000 | 0.3125 |
| 0 | 0 | 0 | 1 | 0.3125 | 0.6250 |
| 0 | 0 | 1 | 0 | 0.6250 | 0.9375 |
| 0 | 0 | 1 | 1 | 0.9375 | 1.2500 |
| 0 | 1 | 0 | 0 | 1.2500 | 1.5625 |
| 0 | 1 | 0 | 1 | 1.5625 | 1.8750 |
| 0 | 1 | 1 | 0 | 1.8750 | 2.1875 |
| 0 | 1 | 1 | 1 | 2.1875 | 2.5000 |
| 1 | 0 | 0 | 0 | 2.5000 | 2.8125 |
| 1 | 0 | 0 | 1 | 2.8125 | 3.1250 |
| 1 | 0 | 1 | 0 | 3.1250 | 3.4375 |
| 1 | 0 | 1 | 1 | 3.4375 | 3.7500 |
| 1 | 1 | 0 | 0 | 3.7500 | 4.0625 |
| 1 | 1 | 0 | 1 | 4.0625 | 4.3750 |
| 1 | 1 | 1 | 0 | 4.3750 | 4.6875 |
| 1 | 1 | 1 | 1 | 4.6875 | 5.0000 |

Analog Input = 2V with Down-Rounding Mechanism

| Step | C[3] | C[2] | C[1] | C[0] | $DAC_{OUT}$(V) | INCR(V) |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0.0000 | 5.0 |
| 2 | 0 | 0 | 0 | 1 | 0.3125 | 5.0 |
| 3 | 0 | 0 | 1 | 0 | 0.6250 | 5.0 |
| 4 | 0 | 0 | 1 | 1 | 0.9375 | 5.0 |
| 5 | 0 | 1 | 0 | 0 | 1.2500 | 5.0 |
| 6 | 0 | 1 | 0 | 1 | 1.5625 | 5.0 |
| 7 | 0 | 1 | 1 | 0 | 1.8750 | 5.0 |
| 8 | 0 | 1 | 1 | 1 | 2.1875 | 0.0 |

Final output with quantization error of 0.3125V

Analog Input = 2V with Up-Rounding Mechanism

| Step | C[3] | C[2] | C[1] | C[0] | $DAC_{OUT}$(V) | INCR(V) |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0.3125 | 5.0 |
| 2 | 0 | 0 | 0 | 1 | 0.6250 | 5.0 |
| 3 | 0 | 0 | 1 | 0 | 0.9375 | 5.0 |
| 4 | 0 | 0 | 1 | 1 | 1.2500 | 5.0 |
| 5 | 0 | 1 | 0 | 0 | 1.5625 | 5.0 |
| 6 | 0 | 1 | 0 | 1 | 1.8750 | 5.0 |
| 7 | 0 | 1 | 1 | 0 | 2.1875 | 0.0 |

Final output with quantization error of 0.3125V

**Fig. 7.9** Four-bit ramp ADC truth table describing its operation

## 7.5 Successive Approximation Type Analog-to-Digital Converter

The third type ADC is based on the successive approximation technique to estimate the value of the analog voltage. This type is a trade-off between the flash-type and the ramp-type in terms of speed and the number of components used in the circuit. As a numerical example, a typical four-bit successive approximation ADC schematic is shown in Fig. 7.10. In this figure, the up-counter in the ramp ADC is replaced by a control logic which successively converts an analog input into a digital form by a trial and error method. The output is obtained at the C[3:0] terminal.

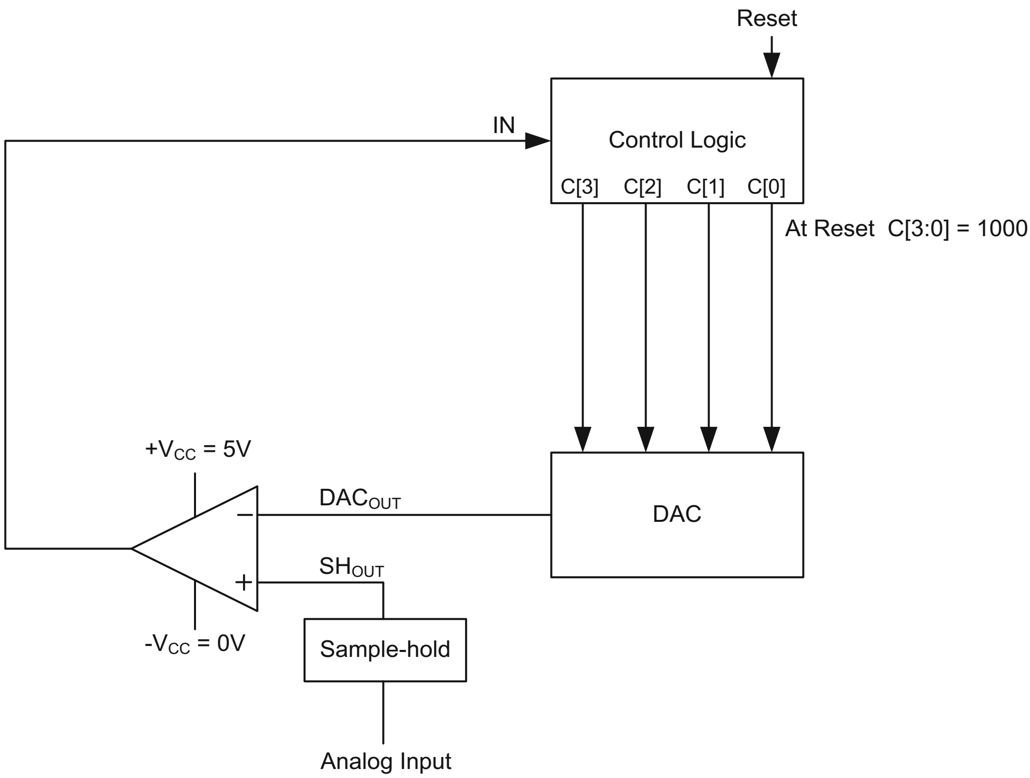



**Fig. 7.10** Typical four-bit successive approximation ADC schematic

The top portion of Fig. 7.11 shows the truth table to operate a four-bit successive approximation ADC. Two numerical examples in this figure illustrate the down-rounding and up-rounding schemes used during conversion.

The first example in Fig. 7.11 illustrates the down rounding mechanism in a four-bit successive approximation ADC. In this example, an analog voltage of 3.5 V is applied to the analog input of the ADC. An external reset starts the converter at C[3:0] = 1000, which is considered a mid point between C[3:0] = 0000, representing the minimum analog input of 0 V, and C[3:0] = 1111, representing the maximum analog input of 5 V for this ADC.

For C[3:0] = 1000, the DAC generates an initial analog voltage of 2.5 V at the $DAC_{OUT}$ node. Since this value is less than the sampled analog voltage of 3.5 V at the $SH_{OUT}$ node, the operational amplifier produces IN = 5 V, and prompts the control logic to try a slightly higher digital output. As a result, the control logic produces C[3:0] = 1100 as its first trial, which is equivalent to a midway point between C[3:0] = 1000 and 1111. $DAC_{OUT}$ becomes 2.5 + (2.5/2) = 3.75 V. But, this new voltage is larger than $SH_{OUT}$ = 3.5 V, and the operational amplifier produces IN = 0 V in return. The drop at IN node is an indication to the control logic that its initial attempt of C[3:0] = 1100 was too large, and it must lower its output. This time, the control logic tries C[3:0] = 1010, which is between C[3:0] = 1000 and 1100, and translates to $DAC_{OUT}$ = 2.5 + (2.5/4) = 3.125 V. This value, in turn, generates IN = 5 V, and prompts the control logic to try a slightly higher output between C[3:0] = 1010 and 1100. In the third round, the control logic produces C[3:0] = 1011. $DAC_{OUT}$ node becomes 2.5 + (2.5/4) + (2.5/8) = 3.4375 V and generates IN = 5 V. This new input suggests the control logic to try even higher digital output, such as 2.5 + (2.5/4) + (2.5/8) + (2.5/16) = 3.5937 V, in the fourth round. However, 2.5/8 = 0.3125 V is the resolution limit for this four-bit ADC, and as a result, the controller stalls at C[3:0] = 1011, revealing $DAC_{OUT}$ = 3.4375 V. This voltage differs from $SH_{OUT}$ = 3.5 V by only 0.0625 V.

The second example in Fig. 7.11 explains the successive approximation technique if the up-rounding scheme is employed. The conversion again starts at C[3:0] = 1000, but with an incremented value of 2.5 + 0.3125 = 2.8125 V at the DAC output. Since this voltage is below $SH_{OUT}$ = 3.5 V, IN node becomes 5 V and prompts the control logic to produce a larger digital output. The control logic responds this with a digital output of C[3:0] = 1100, which corresponds to the analog voltage of 2.8125 + (2.5/2) = 4.0625 V at the $DAC_{OUT}$ node. As a result, IN node becomes 0 V, and forces the control logic to lower its digital output. This time, the control logic tries C[3:0] = 1010 which is equivalent to 2.8125 + (2.5/4) = 3.4375 at the $DAC_{OUT}$ node. Due to the resolution limit of this four-bit ADC, this step also becomes the end of successive approximation.

Step Size = $5/2^4$ = 0.3125V

| C[3] | C[2] | C[1] | C[0] | Down-Round (V) | Up-Round (V) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0.0000 | 0.3125 |
| 0 | 0 | 0 | 1 | 0.3125 | 0.6250 |
| 0 | 0 | 1 | 0 | 0.6250 | 0.9375 |
| 0 | 0 | 1 | 1 | 0.9375 | 1.2500 |
| 0 | 1 | 0 | 0 | 1.2500 | 1.5625 |
| 0 | 1 | 0 | 1 | 1.5625 | 1.8750 |
| 0 | 1 | 1 | 0 | 1.8750 | 2.1875 |
| 0 | 1 | 1 | 1 | 2.1875 | 2.5000 |
| 1 | 0 | 0 | 0 | 2.5000 | 2.8125 |
| 1 | 0 | 0 | 1 | 2.8125 | 3.1250 |
| 1 | 0 | 1 | 0 | 3.1250 | 3.4375 |
| 1 | 0 | 1 | 1 | 3.4375 | 3.7500 |
| 1 | 1 | 0 | 0 | 3.7500 | 4.0625 |
| 1 | 1 | 0 | 1 | 4.0625 | 4.3750 |
| 1 | 1 | 1 | 0 | 4.3750 | 4.6875 |
| 1 | 1 | 1 | 1 | 4.6875 | 5.0000 |

Analog Input = 3.5V with Down-Rounding Mechanism START with (5.0/2) = 2.5

| Step | C[3] | C[2] | C[1] | C[0] | $DAC_{OUT}$(V) | Control Logic In |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 2.5000 | 3.5 > 2.5000<br>Thus try 2.5 + (2.5/2) = 3.75 |
| 2 | 1 | 1 | 0 | 0 | 3.7500 | 3.5 < 3.7500<br>Thus try 2.5 + (2.5/4) = 3.125 |
| 3 | 1 | 0 | 1 | 0 | 3.1250 | 3.5 > 3.1250<br>Thus try 2.5 + (2.5/4) + (2.5/8) = 3.4375 |
| 4 | 1 | 0 | 1 | 1 | 3.4375 | 3.5 > 3.4375<br>Stop at 3.4375 since there is no resolution under (2.5/8) |

Final output with quantization error of 0.3125V

Analog Input = 3.5V with Up-Rounding Mechanism START with (5.0/2) = 2.8125

| Step | C[3] | C[2] | C[1] | C[0] | $DAC_{OUT}$(V) | Control Logic In |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 2.8125 | 3.5 > 2.8125<br>Thus try 2.8125 + (2.5/2) = 4.0625 |
| 2 | 1 | 1 | 0 | 0 | 4.0625 | 3.5 < 4.0625<br>Thus try 2.8125 + (2.5/4) = 3.4375 |
| 3 | 1 | 0 | 1 | 0 | 3.4375 | 3.5 > 3.4375<br>Stop at 3.4375 since there is no resolution under (2.5/8) |

Final output with quantization error of 0.3125V

**Fig. 7.11** Four-bit successive approximation ADC truth table describing down-rounding and up-rounding approximation techniques

The control circuit of the four-bit ADC with down-rounding scheme is shown in Fig. 7.12. In this figure, the approximation process starts at the midpoint, C[3:0] = 1000, corresponding to $DAC_{OUT}$ = 2.5 V according to the table in Fig. 7.11. When the external reset is removed, and Δv, the difference between $SH_{OUT}$ and $DAC_{OUT}$, is found to be greater than the 0.3125 V step size, the control logic either goes to the state 1.25, and produces C[3:0] = 0100 (equivalent to 1.25 V) or the state 3.75, and produces C[3:0] = 1100 (equivalent to 3.75 V) in the first step of the successive approximation. This decision depends on the value of the control logic input, IN. If IN = 0, which translates to the analog input to be less than 2.5 V, the next state becomes the state 1.25. However, if IN = 1, the analog input is considered to be greater than 2.5 V, and the next state becomes the state 3.75. If Δv is less than 0.3125 V, on the other hand, the control logic cannot proceed further due to its resolution limit, and moves to the state DONE. In the second step of successive approximation, the state 1.25 either transitions to the state 0.625 or the state 1.875, depending on the value at IN node. Similar transitions take place from the state 3.75 to either the state 3.125 or the state 4.375, again depending on the value at IN. After this point, the state machine performs one last approximation to estimate the value of analog input voltage, and reaches the DONE state with an output value as shown in Fig. 7.12.

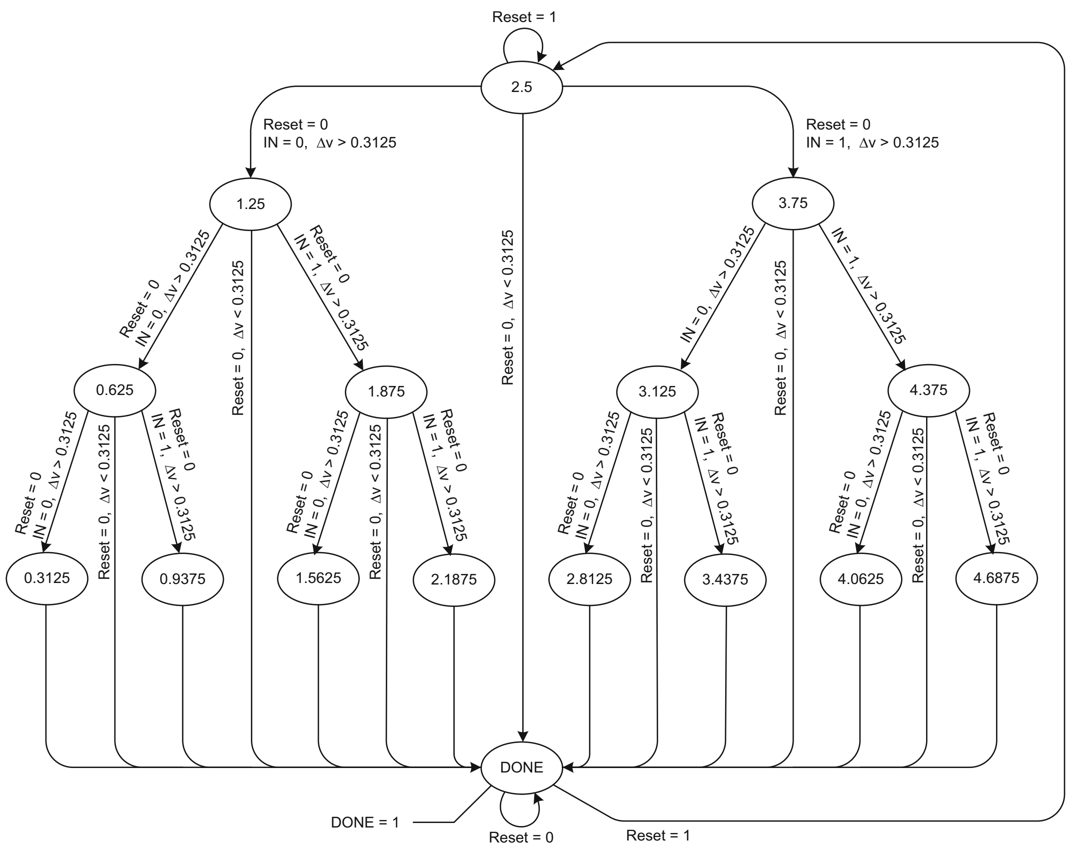



**Fig. 7.12** Four-bit successive approximation control circuit

## 7.6 Weighted Sum Type Digital-to-Analog Converter

The most common DAC utilizes the weighted summation method of digital inputs. A three-bit DAC with a weighted binary adder is shown in Fig. 7.13 as an example.

This circuit is composed of two parts. The first part adds all three binary input bits, IN[2] (the most significant bit), IN[1] and IN[0] (the least significant bit), and produces an output, $ADD_{OUT} = -(0.5\ IN[2] + 0.25\ IN[1] + 0.125\ IN[0])$ according to the equation in Fig. 7.14. The second part is an analog inverter which forms $OUT = -ADD_{OUT}$.

Therefore, the circuit in Fig. 7.13 generates $OUT = 0.5\ IN[2] + 0.25\ IN[1] + 0.125\ IN[0]$, where each binary value at IN[2:0] input is multiplied by the coefficients, $2^{-1}$, $2^{-2}$ and $2^{-3}$, before they are added to produce an output. For example, the combination of IN[2] = 1, IN[1] = 0 and IN[0] = 1, with +5 and 0 V logic levels generates OUT = 2.5 + 0.625 = 3.125 V. Similarly, all the other analog outputs in Fig. 7.14 can be generated using the equation at the top part of this figure with a maximum error of 0.625 V.

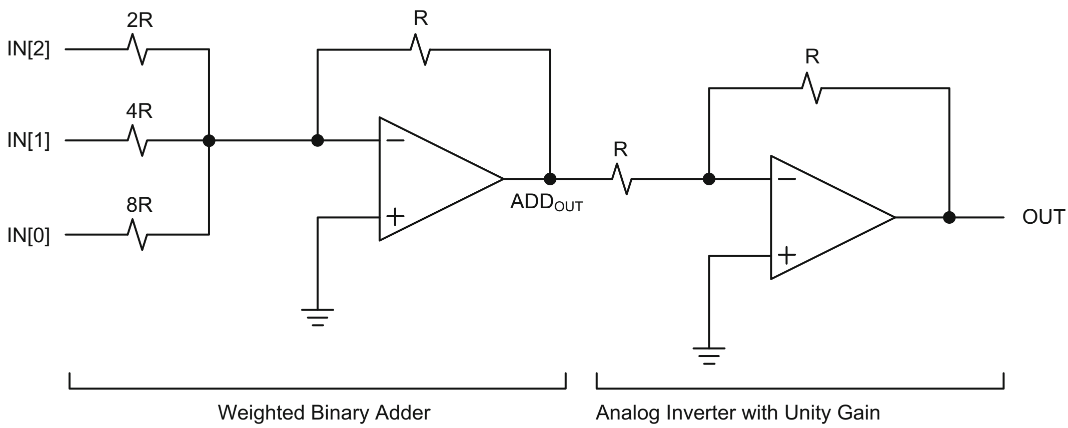



**Fig. 7.13** Three-bit DAC schematic with weighted binary adder

$$ADD_{OUT} = -\frac{R}{2R}\,IN[2] - \frac{R}{4R}\,IN[1] - \frac{R}{8R}\,IN[0]$$
$$= -\,0.5\,IN[2] - 0.25\,IN[1] - 0.125\,IN[0]$$

$$OUT = -ADD_{OUT} = 0.5\,IN[2] + 0.25\,IN[1] + 0.125\,IN[0]$$

| IN[2] | IN[1] | IN[0] | OUT(V) |
|---|---|---|---|
| 0 | 0 | 0 | 0.000 |
| 0 | 0 | 1 | 0.625 |
| 0 | 1 | 0 | 1.250 |
| 0 | 1 | 1 | 1.875 |
| 1 | 0 | 0 | 2.500 |
| 1 | 0 | 1 | 3.125 |
| 1 | 1 | 0 | 3.750 |
| 1 | 1 | 1 | 4.375 |

Example:

IN[2] = 1, IN[1] = 0, IN[0] = 1 with +5V/0V logic levels

$ADD_{OUT} = -2.5 - 0 - 0.625 = -3.125V$

OUT = + 3.125V with 0.625V quantization error

**Fig. 7.14** Three-bit DAC operation with weighted binary adder

## 7.7 Ladder Type Digital-to-Analog Converter

The second kind of DAC uses a ladder structure composed of resistors as shown in Fig. 7.15. Each ladder segment contains a switch, Si, where i = 0, 1, … (N–1). The switch can be thrown to ground or $V_{REF}$ depending on the value of the binary input.

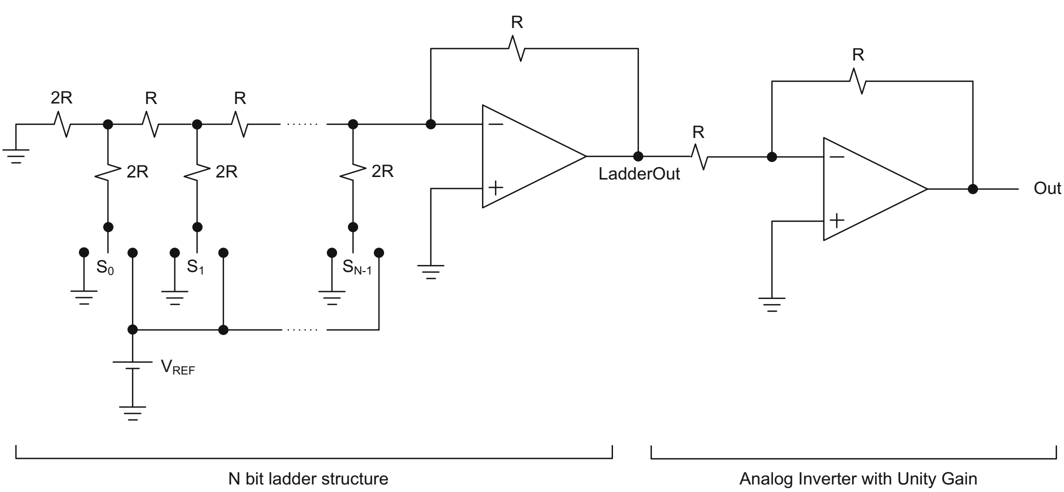



**Fig. 7.15** N-bit DAC schematic with ladder configuration

The ladder structure produces an intermediate output, LadderOut, which is the weighted sum of all N binary inputs. The ratio, $V_{REF}/2^N$, determines the final value of LadderOut when it is multiplied with the weighted sum as shown in Fig. 7.16. The analog inverter generates Out = −LadderOut and creates a positive value. The example of a three-bit DAC with ladder configuration is shown at the bottom section of Fig. 7.16. With $S_2$ and $S_0$ switches thrown to $V_{REF}$ = 5 V and $S_1$ to ground, this combination produces a weighted sum of $(2^2 + 2^0) = 5$ V. When this value is multiplied with the ratio, $V_{REF}/2^3 = 5/8 = 0.625$ V, the overall result becomes Out = 3.125 V for a digital input of $S_2 = 1$, $S_1 = 0$, $S_0 = 1$.

$$\text{LadderOut} = -\frac{V_{REF}}{2^N}(S_{N-1}\, 2^{N-1} + S_{N-2}\, 2^{N-2} + \ldots. + S_0\, 2^0)$$

$$\text{Out} = -\,\text{LadderOut} = \frac{V_{REF}}{2^N}(S_{N-1}\, 2^{N-1} + S_{N-2}\, 2^{N-2} + \ldots. + S_0\, 2^0)$$

Example:

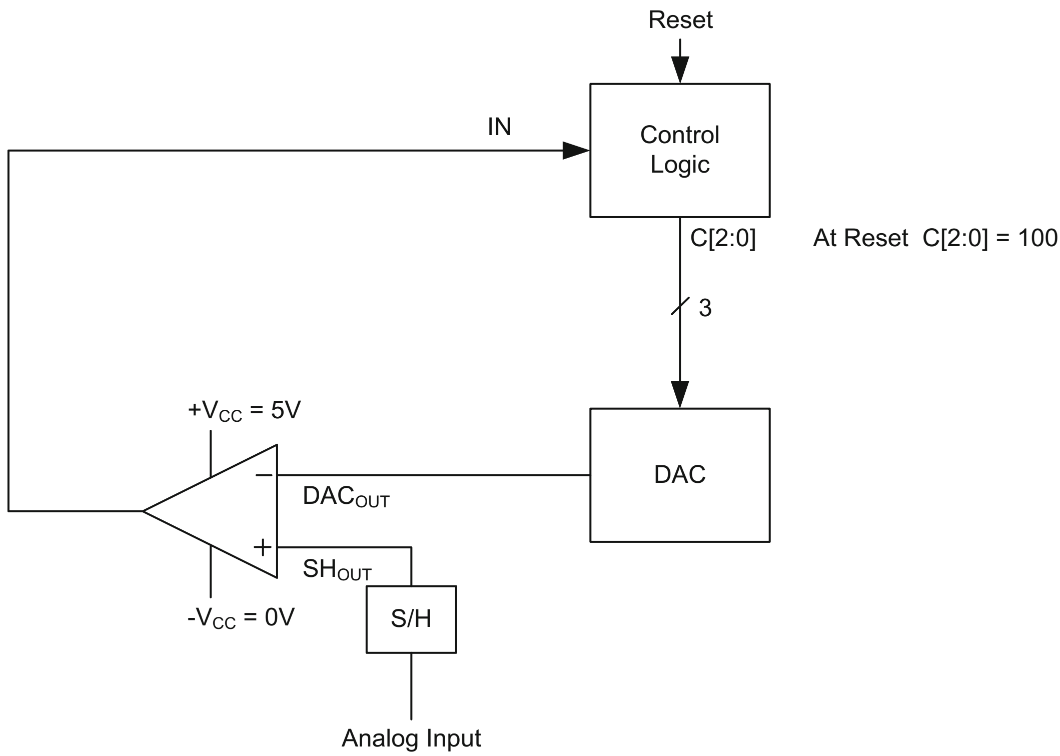
For a 3-bit DAC with $S_2 = 1$, $S_1 = 0$, $S_0 = 1$ and $V_{REF} = 5V$

$$\text{Out} = \frac{5}{2^3}(S_2\, 2^2 + S_1\, 2^1 + S_0\, 2^0) = \frac{5}{8}(4 + 0 + 1) = 3.125V$$

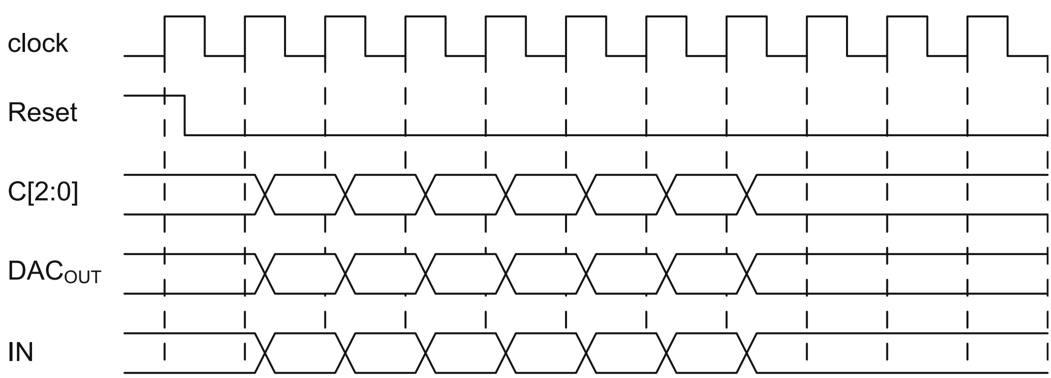
**Fig. 7.16** Three-bit DAC operation with ladder configuration

## Review Questions

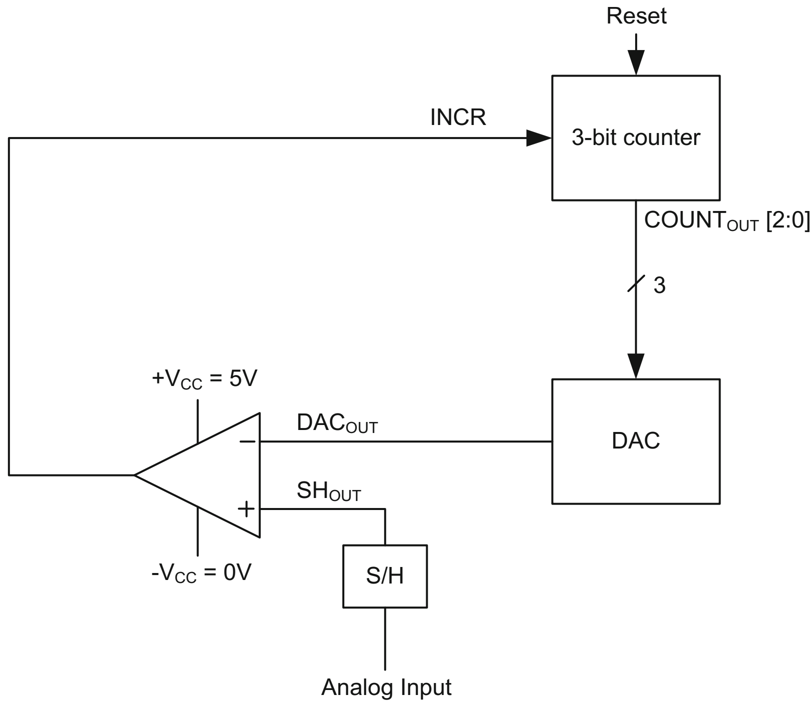
**1.** A three-bit successive approximation ADC is given below. A sample-Hold circuit (S/H) samples the Analog Input in periodic intervals and feeds the voltage level to the operational amplifier.




Use the timing diagram below, and fill the blanks with analog or digital data for an Analog Input = 0.5 V with down-rounding mechanism.



**2.** A three-bit ramp ADC below operates with $+V_{CC} = 3$ V and $-V_{CC} = 0$ V. Input to this ADC can take any value between 0 and 3 V.




(a) Assume that DAC has an up-rounding scheme to generate analog outputs from digital inputs. Apply 1.2 V to the Analog Input port, and draw the timing diagram that contains the clock, Reset, counter output ($COUNT_{OUT}$), DAC output ($DAC_{OUT}$) and operational amplifier output (INCR). Show what happens to the timing diagram when the active-high Reset signal transitions to logic 1 after the ADC produces the desired digital output.

(b) Now apply 2.9 V to the Analog Input. Draw the timing diagram with the same inputs and outputs listed above. Show what happens to the timing diagram when the active-high Reset signal transitions to logic 1 after the ADC produces the desired digital output.

(c) Assume that the DAC rounding scheme is changed from up-rounding to down-rounding scheme. Apply 1.2 V to the Analog Input and generate the timing diagram with the input and output signals listed above. Show what happens to the timing diagram when the active-high Reset signal becomes logic 1 after the ADC produces the desired digital output. Do you see any issues with the operation of this circuit?

(d) Now apply 2.9 V at the Analog Input port and generate the timing diagram with the input and output signals listed above. Do you see any issues in the operation of this circuit?

**3.** In a three-bit successive approximation ADC in Fig. 7.10, what kind of circuit can be built to detect the voltage difference between the Analog Input voltage at $SH_{OUT}$ and the DAC output at $DAC_{OUT}$ at each state to be able to make state transitions in Fig. 7.12?

**4.** Build an eight-bit DAC that uses weighted summation technique. Find the analog voltage levels for inputs, 00110011, 10000000, 00000001, 11111111 and 10101010. Compare the analog voltage values corresponding to 10000000, 00000001 and 11111111 inputs from this DAC with the analog output voltages corresponding to the 1000, 0001 and 1111 inputs from a four-bit DAC that uses weighted binary adder.

**5.** Build an eight bit DAC that uses ladder configuration. How can you implement the input switches used in the ladder configuration? Apply 00110011, 10000000, 00000001, 11111111 and 10101010 inputs to this DAC and show how the circuit works. Is there any difference between the output values between this type and the type that uses weighted summation?

**6.** Implement an eight-bit flash, ramp and successive approximation ADC. Compare each type in terms of speed, and the number of components used in the circuit.