MOS Transistors and CMOS Circuits 3

3.1 N-Channel MOSFET (NMOSFET)

N-channel Metal-Oxide-Semiconductor-Field-Effect-Transistor (NMOSFET) is a three-terminal device that produces a drain current, I_D, when positive voltages are applied to the gate and drain terminals with respect to the source terminal as shown in Fig. 3.1.

When the conduction starts, the device produces I_D-V_{DS} characteristics for different values of V_{GS} as shown in Fig. 3.2. Each curve in this figure is obtained by increasing V_{DS} and measuring I_D at a constant V_{GS}. Each I-V curve consists of two distinct regions: an active region and a saturation region. The device transitions from the active region into the saturation region when V_{DS} reaches a saturation potential, $V_{DSAT} = V_{GS} - V_{TN}$. Here, V_{TN} is the threshold voltage applied to the gate to turn on the transistor.

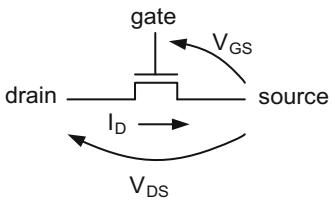


Fig. 3.1 NMOSFET circuit symbol

A. Bindal, *Electronics for Embedded Systems*,
DOI 10.1007/978-3-319-39439-8_3

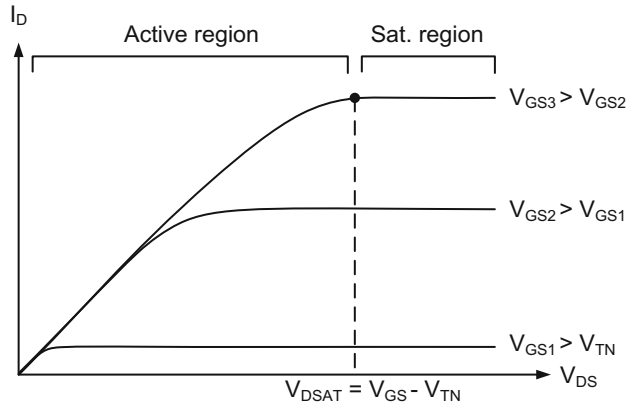


Fig. 3.2 NMOSFET current-voltage characteristics

The I-V curve in Fig. 3.2 can be explained using the following equation:

$$I_D = \frac{\mu_N C_{OX} W_N}{L_N}\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{3.1}$$

where,

μ_N is the mobility of electrons in the drain-source channel in $cm^2/Vsec$
C_{OX} is the gate oxide capacitance in F/cm^2
W_N is the width of the NMOS transistor
L_N is the length of the NMOS transistor
V_{TN} is the threshold voltage of the NMOS transistor

For small values of V_{DS}, Eq. 3.1 can be approximated as:

$$I_D = \frac{\mu_N C_{OX} W_N}{L_N}(V_{GS} - V_{TN})V_{DS} \tag{3.2}$$

This equation represents the active region of operation where the NMOS transistor reveals a linear relationship between I_D and V_{DS}. Therefore, in this region, NMOSFET can be represented as a resistor as shown in Fig. 3.3. In this figure, the power supply voltage, V_{DD}, is the maximum allowable voltage applied to the gate of the transistor.

$$R_N = \frac{V_{DS}}{I_D} = \frac{L_N}{\mu_N C_{OX}(V_{DD} - V_{TN})W_N} \tag{3.3}$$

The constant terms in Eq. 3.3 can be combined and equated to K_N as shown below.

$$K_N = \frac{L_N}{\mu_N C_{OX}(V_{DD} - V_{TN})}$$

Then Eq. 3.3 becomes:

$$R_N = \frac{K_N}{W_N} \tag{3.4}$$

Equation 3.4 becomes approximately equal to the inverse slope of the I_D–V_{DS} curve in Fig. 3.3 for V_{DS} smaller than $V_{DSAT} = V_{DD} - V_{TN}$.

For $V_{DS} > V_{DSAT} = V_{DD} - V_{TN}$, however, the NMOS transistor goes into the saturation region as shown in Fig. 3.3. I_{DSAT} can be obtained by substituting $V_{GS} = V_{DD}$ and $V_{DSAT} = V_{DD} - V_{TN}$ in Eq. 3.1. Thus,

$$I_D = \frac{\mu_N C_{OX} W_N}{2L_N}(V_{DD} - V_{TN})^2 \tag{3.5}$$

Equation 3.5 is a constant and independent of V_{DS}. Therefore, the NMOS transistor can be represented as a constant current when it is in saturation region.

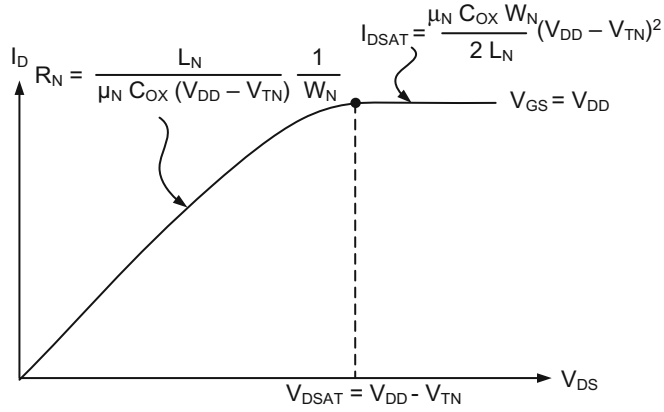


Fig. 3.3 NMOSFET I_D–V_{DS} curve when $V_{DS} = V_{DD}$ and the equivalent circuits

3.2 P-Channel MOSFET (PMOSFET)

As a complementary transistor to NMOSFET, P-channel MOSFET (PMOSFET) is also a three-terminal device which produces a drain current, I_D, when negative voltages are applied to the gate and drain terminals with respect to the source as shown in Fig. 3.4.

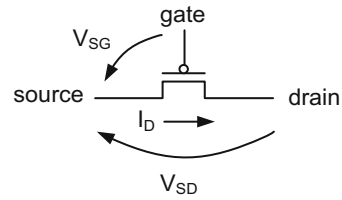


Fig. 3.4 PMOSFET circuit symbol

The device produces I_D–V_{SD} characteristics for different values of V_{SG} as shown in Fig. 3.5. Each curve in this figure is obtained at a constant V_{SG}, and composed of the active and saturation regions. As in NMOS transistor, the device transitions from the active region to the saturation region when V_{SD} reaches a saturation potential, $V_{DSAT} = V_{SG} - V_{TP}$, where V_{TP} is the threshold voltage to turn on the transistor.

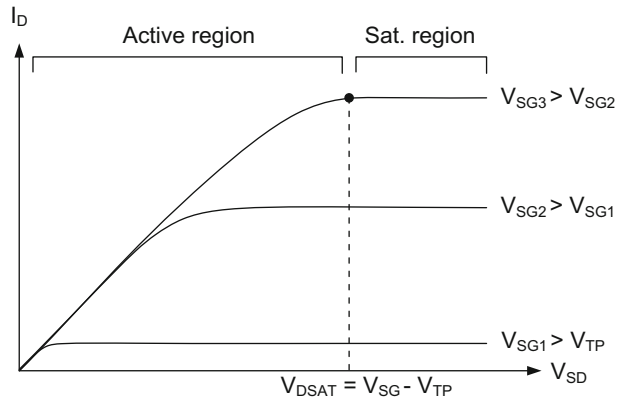


Fig. 3.5 PMOSFET current-voltage characteristics

The mathematical expression in Eq. 3.6 below identifies the I_D-V_{SD} characteristics above.

$$I_D = \frac{\mu_P C_{OX} W_P}{L_P}\left[(V_{SG} - V_{TP})V_{SD} - \frac{V_{SD}^2}{2}\right] \tag{3.6}$$

where,

μ_P is the mobility of holes in the drain-source channel in $cm^2/Vsec$
C_{OX} is the gate oxide capacitance in F/cm^2
W_P is the width of the PMOS transistor
L_P is the length of the PMOS transistor
V_{TP} is the threshold voltage of the PMOS transistor

For small values of V_{SD}, Eq. 3.6 becomes:

$$I_D = \frac{\mu_P C_{OX} W_P}{L_P}(V_{SG} - V_{TP})V_{SD} \tag{3.7}$$

Like its NMOS counterpart, Eq. 3.7 represents the active region of operation for the PMOS transistor. This equation can be approximated as a resistor in Eq. 3.8 when the power supply voltage, V_{DD}, is applied between the gate and source terminals.

$$R_P = \frac{V_{SD}}{I_D} = \frac{L_P}{\mu_P C_{OX}(V_{DD} - V_{TP})W_P} \tag{3.8}$$

Combining all constant terms in Eq. 3.8 yields:

$$K_P = \frac{L_P}{\mu_P C_{OX}(V_{DD} - V_{TP})}$$

Then Eq. 3.8 becomes:

$$R_P = \frac{K_P}{W_P} \tag{3.9}$$

This equation is approximately equal to the inverse slope of the I_D-V_{SD} curve in Fig. 3.6 when V_{SG} is smaller than $V_{DD} - V_{TP}$.

For $V_{SD} > V_{DSAT} = V_{DD} - V_{TP}$, the PMOS transistor goes into the saturation region. The current in this region can be obtained by substituting $V_{SG} = V_{DD}$ and $V_{DSAT} = V_{DD} - V_{TP}$ into Eq. 3.6. Thus,

$$I_D = \frac{\mu_P C_{OX} W_P}{2L_P}(V_{DD} - V_{TP})^2 \tag{3.10}$$

Equation 3.10 is also constant and independent of V_{SD}. Therefore, the PMOS transistor is represented as a constant current when it is in saturation region.

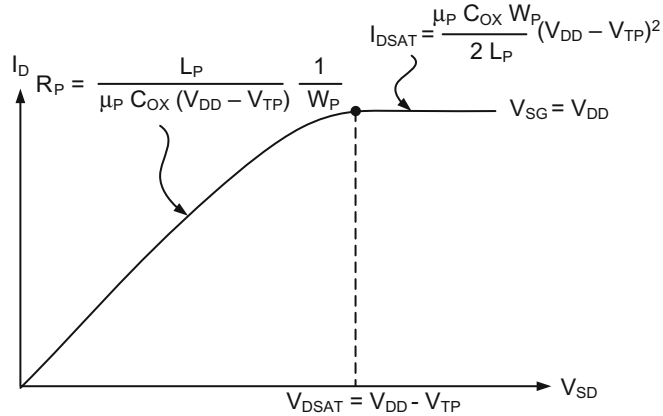


Fig. 3.6 PMOSFET equivalent circuit

3.3 Complementary MOS (CMOS) Inverter

The first Complementary-Metal-Oxide-Semiconductor (CMOS) logic gate we will examine is the inverter. This gate consists of a single NMOS transistor in series with a PMOS transistor as shown in Fig. 3.7.

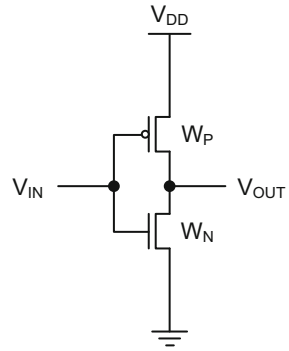


Fig. 3.7 CMOS inverter

In this circuit, when the input voltage, $V_{IN}(t)$, becomes equal to V_{DD} (logic 1), the NMOS transistor turns on (because $V_{GS} = V_{DD} > V_{TN}$), and the PMOS transistor turns off (because $V_{SG} = 0$ V). The capacitance, C_L, at the output terminal is then discharged through the equivalent NMOS resistance, R_N, as shown in the left side of Fig. 3.8, and the output voltage decays towards 0 V with a RC time constant of R_NC_L. In other words, V_{OUT} becomes:

$$V_{OUT}(t) = V_{DD}\,\mathbf{exp}\left(-\frac{t}{R_NC}\right) \tag{3.11}$$

When $V_{IN}(t) = 0$ V, on the other hand, NMOS transistor turns off (because $V_{GS} = 0$ V), and PMOS turns on (because $V_{SG} = V_{DD} > V_{TP}$). Consequently, a charge path forms through the equivalent PMOS resistor to charge the output capacitance from 0 V towards V_{DD} as shown in the right side of Fig. 3.8. In other words,

$$V_{OUT}(t) = V_{DD}\left[1 - \mathbf{exp}\left(-\frac{t}{R_PC}\right)\right] \tag{3.12}$$

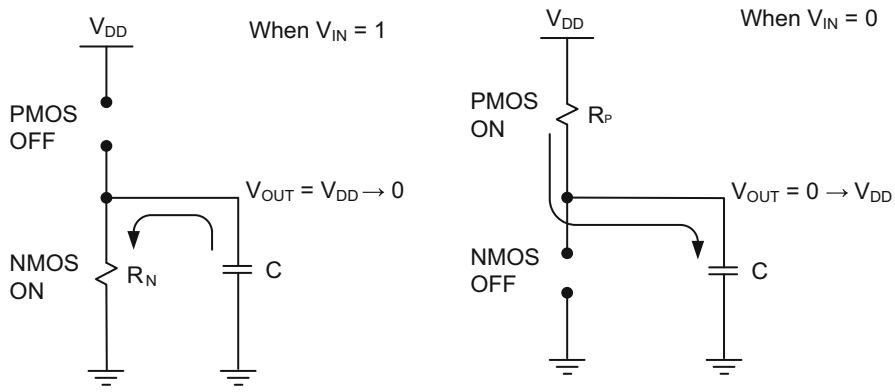


Fig. 3.8 CMOS inverter discharge path (*left*) and charge path (*right*)

3.4 Two-Input CMOS NAND Logic Gate

The two-input CMOS NAND gate is shown in Fig. 3.9. This logic gate is composed of two sections: an NMOS tree (between the output terminal and the ground), and a PMOS tree (between the power supply voltage and the output terminal). To construct the NMOS tree, two NMOS transistors are connected in series between the output terminal and the ground. The reason for this configuration is that if one of the NMOS transistors turns off, there will be no discharge path to lower V_{OUT}, and V_{OUT} stays at V_{DD}. However, if both NMOS transistors are turned on, V_{OUT} transitions to 0 V, which complies with the truth table for two-input NAND gate.

The next phase is to form the PMOS tree. The PMOS tree is configured in a complementary manner to the NMOS tree. This means that any series combination of NMOS transistors in the NMOS tree must be transformed into a parallel combination of PMOS transistors in the PMOS tree, and vice versa. Therefore, we need to connect two PMOS transistors in parallel to form the PMOS tree, and place it between V_{OUT} and V_{DD} as shown in Fig. 3.9.

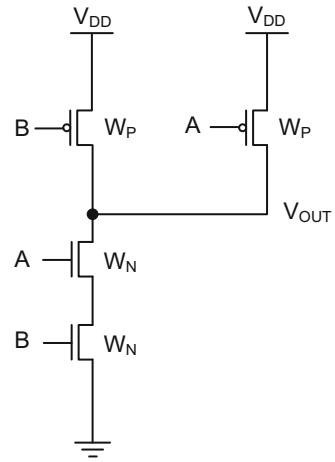


Fig. 3.9 Two-input CMOS NAND gate

Figure 3.10 shows the discharge and charge paths for the two-input NAND gate. The only discharge path in this figure is through the series combination of two equivalent NMOS resistors as shown by the leftmost figure in Fig. 3.10. This yields the following output voltage:

$$V_{OUT}(t) = V_{DD}\,\mathbf{exp}\left(-\frac{t}{2R_NC}\right) \tag{3.13}$$

The worst-case charge path, on the other hand, forms as a result of turning on only one of the PMOS transistors in the PMOS tree shown in the middle part of Fig. 3.10, and results in the following output voltage:

$$V_{OUT}(t) = V_{DD}\left[1 - \mathbf{exp}\left(-\frac{t}{R_PC}\right)\right] \tag{3.14}$$

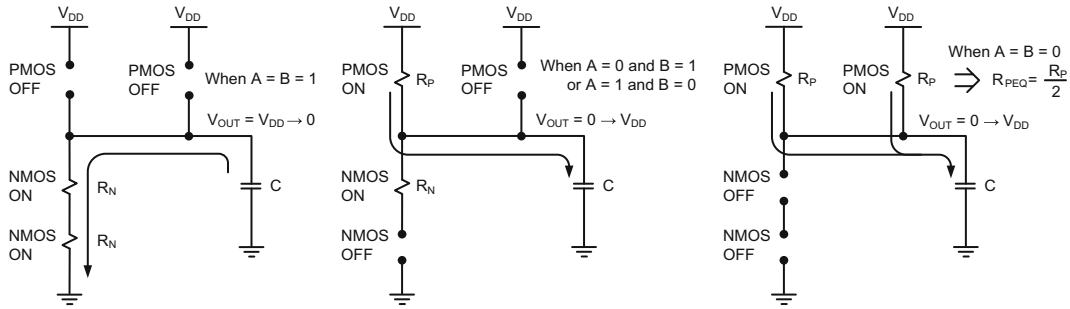


Fig. 3.10 Two-input CMOS NAND gate discharging (*left*) and charging (*middle* and *right*) paths

The best-case charge path turns on both PMOS transistors in the PMOS tree, and results in charging the output node in a faster pace as shown by the rightmost figure in Fig. 3.10. Equation 3.15 shows this behavior:

$$V_{OUT}(t) = V_{DD}\left[1 - \mathbf{exp}\left(-\frac{2t}{R_PC}\right)\right] \tag{3.15}$$

In Eqs. 3.13 to 3.15, the capacitance term, C, is associated with the intrinsic capacitance at the output node of the two-input NAND gate in Fig. 3.9. If there is an external capacitance at the output node, it must be added to the intrinsic capacitance before calculating the value of V_{OUT}.

3.5 Two-Input CMOS NOR Logic Gate

The two-input CMOS NOR gate is shown in Fig. 3.11. To configure this logic gate, an NMOS tree composed of two parallel NMOS transistors is formed first. This arrangement ensures V_{OUT} to be 0 V if one or more NMOSFETs in the NMOS tree are turned on. When both devices are turned off, then V_{OUT} becomes V_{DD} as dictated by the truth table of this gate.

The PMOS tree is formed in a complementary fashion to the NMOS tree, and results in two PMOS transistors in series between V_{DD} and V_{OUT} as shown in Fig. 3.11.

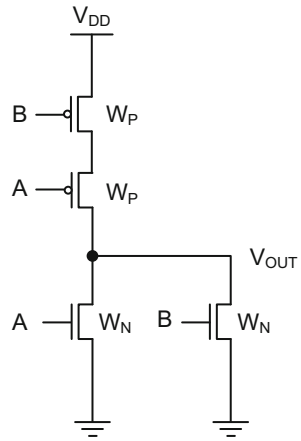


Fig. 3.11 Two-input CMOS NOR gate

Figure 3.12 shows a discharge path and two charge paths for the two-input NOR gate. The worst-case discharge path in this figure is through an NMOS transistor as shown by the leftmost figure in Fig. 3.12. This yields the following output voltage:

$$V_{OUT}(t) = V_{DD}\,\mathbf{exp}\left(-\frac{t}{R_N C}\right) \tag{3.16}$$

The best-case discharge path is when both NMOS transistors are turned on as shown by the center figure in Fig. 3.12. This produces a faster discharge rate as described by Eq. 3.17 below.

$$V_{OUT}(t) = V_{DD}\,\mathbf{exp}\left(-\frac{2t}{R_N C}\right) \tag{3.17}$$

The only charge path is to turn on both PMOS transistors in the PMOS tree as shown by the rightmost figure in Fig. 3.12. It results in the following output voltage:

$$V_{OUT}(t) = V_{DD}\left[1 - \mathbf{exp}\left(-\frac{t}{2R_PC}\right)\right] \tag{3.18}$$

In Eqs. 3.16 to 3.18, the capacitance term, C, is associated with the intrinsic capacitance at the output node of the two-input NOR gate in Fig. 3.11. If there is an external capacitance at the output node, this capacitance must be added to the intrinsic capacitance before calculating the value of V_{OUT}.

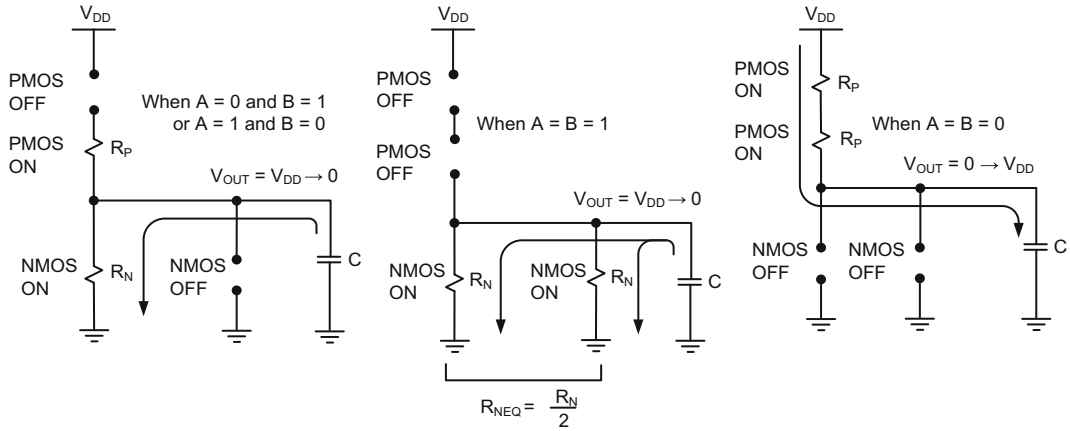


Fig. 3.12 Two-input CMOS NOR gate discharging (*left* and *middle*) and charging (*right*) paths

3.6 Complex CMOS Logic Gate Implementation

The best way to show how to build a complex CMOS logic gate is to give a comprehensive example, outlining each step in the implementation one at a time, and discussing the design trade-offs when they become necessary. For this particular reason, implementing a logic function, such as out = A . B . C + D, serves these two criteria. First, this logic gate is composed of AND and OR logic functions. Second, it calls for numerous design trade-offs during its implementation. There are basically two ways to implement this logic function.

The first method uses discrete CMOS gates. This produces a three-input AND gate with the A, B and C inputs, and a two-input OR gate, combining the D input with the output of the AND gate.

The second method integrates all the AND and OR functions of this complex gate in a single gate. This method forms a combined NMOS tree first, and then builds a complementary logic function in the PMOS tree. When forming the NMOS tree, we must remember connecting all NMOS transistors in series if we need to implement an AND function, and in parallel to implement an OR function.

Therefore, to implement out = A . B . C + D, we start with connecting three NMOS transistors with the A, B and C inputs in series to form the AND function. Then, we connect another NMOS transistor with the D input in parallel to this combination to complete the NMOS tree as shown in Fig. 3.13.

PMOS tree is formed in a complementary fashion: the PMOS transistors with the A, B and C inputs have to be connected in parallel because NMOS transistors with the same inputs were connected in series in the NMOS tree. This parallel combination is then connected in series with a PMOS transistor with the D input because the NMOS transistor with D input was connected in parallel in the NMOS tree. However, this process only produces an output function equal to out $= \overline{(A \,.\, B \,.\, C + D)}$ if the implementation stops here. We need to add an inverter at the output of the logic gate to further convert the complemented logic function to its uncomplemented form, out = A . B . C + D.

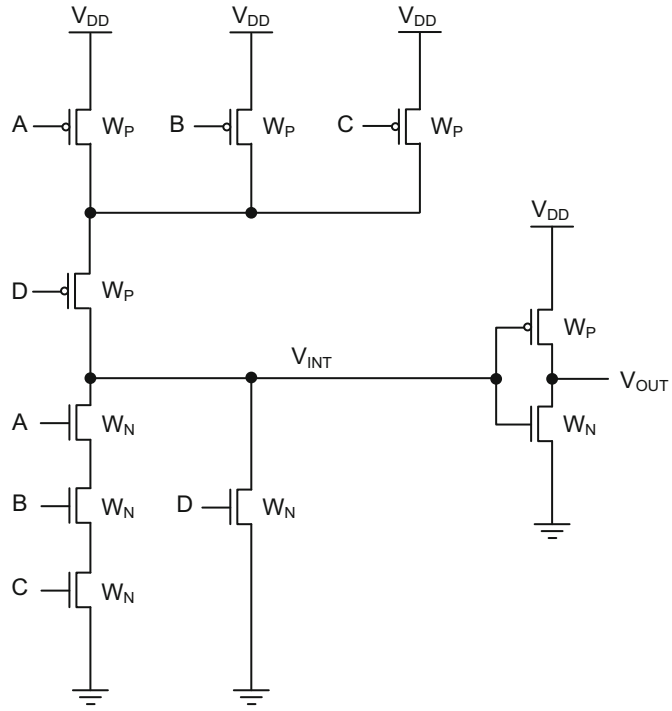


Fig. 3.13 Implementation of out = A . B . C + D

The worst-case discharge and charge paths of this circuit are shown in Fig. 3.14. Both charging and discharging the output node takes two steps.

To be able to charge the output node, three equivalent NMOS resistors connected in series need to discharge the intermediate node, V_{INT}, as shown by the top figure in Fig. 3.14. The total capacitance at V_{INT} is approximately the input capacitance of the inverter,

C_{INV}, which is the combination of NMOS and PMOS transistor gate capacitances. Therefore,

$$C_{INV} = C_{GN} + C_{GP} = C_{OX}(W_N + W_P)L \text{ where } L = L_N = L_p \tag{3.19}$$

Once the charge across C_{INV} is drained away, and V_{INT} is lowered to 0 V, then in the second step, the PMOS transistor in the inverter turns on to charge the output node towards V_{DD}.

To discharge the output node, the intermediate node needs to be charged by two equivalent PMOS resistors connected in series as shown by the bottom figure in Fig. 3.14. Once V_{INT} reaches V_{DD}, then the equivalent NMOS resistor in the inverter discharges the output node.

Another method to form out = A . B . C + D calls for the complemented inputs, $\overline{A}$, $\overline{B}$, $\overline{C}$ and $\overline{D}$, applied to the input of the logic gate if they are available. This method follows manipulating the logic function using De Morgan's theorem.

In other words,

$$\text{out} = A \,.\, B \,.\, C + D = \overline{\overline{(A \,.\, B \,.\, C + D)}} = (\overline{\overline{A} + \overline{B} + \overline{C}) \,.\, \overline{D}} \tag{3.20}$$

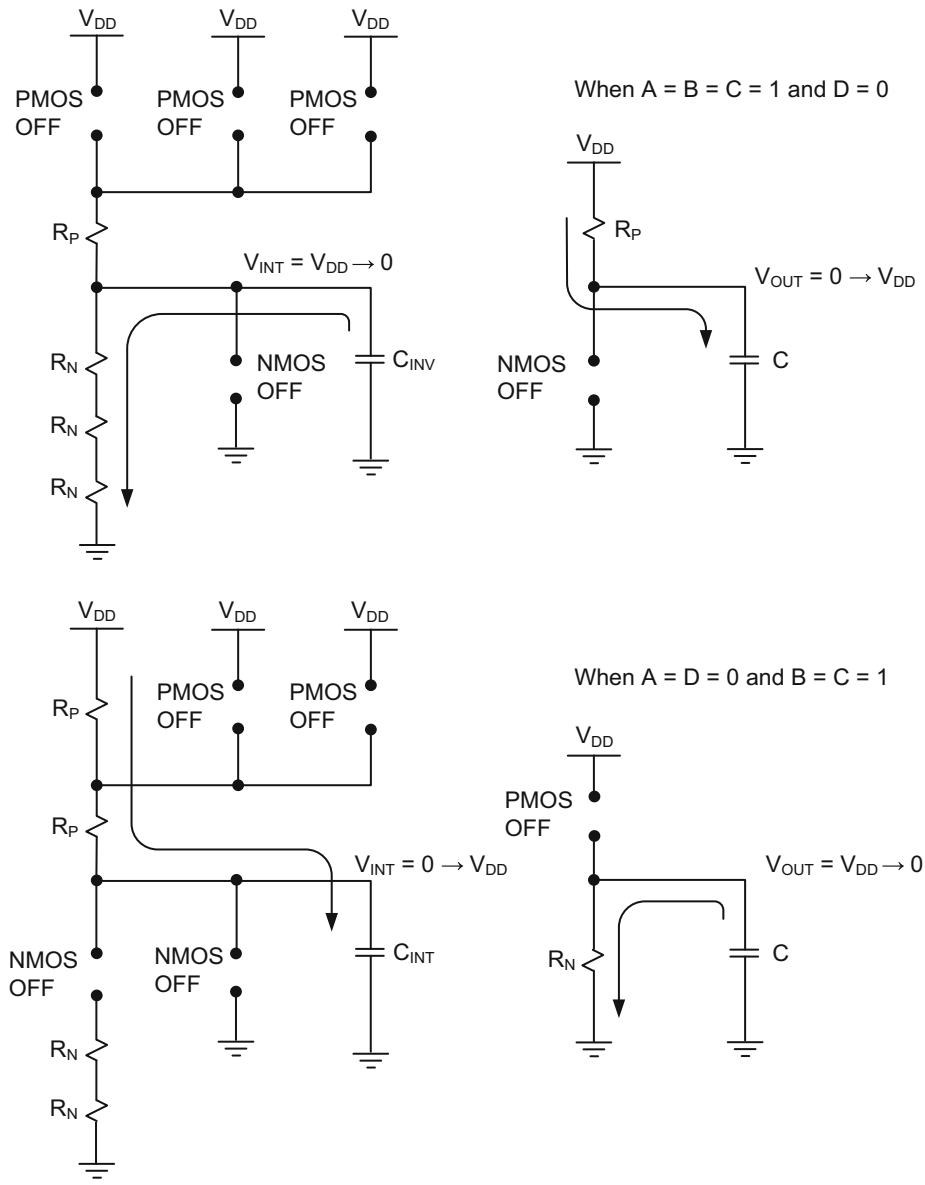


Fig. 3.14 Worst-case charge and discharge paths for out = A . B . C + D

The logic function in Eq. 3.20 has already been complemented, and does not require an additional inverter at the output as shown in Fig. 3.15. To form the NMOS tree of this circuit, three NMOS transistors with complemented inputs, $\overline{A}$, $\overline{B}$ and $\overline{C}$, are connected in parallel. Then this combination is connected in series with another NMOS transistor with $\overline{D}$ input as shown in Fig. 3.15. The PMOS tree requires three PMOS transistors in series with $\overline{A}$, $\overline{B}$ and $\overline{C}$ inputs, and a single PMOS transistor with $\overline{D}$ input in parallel to this combination.

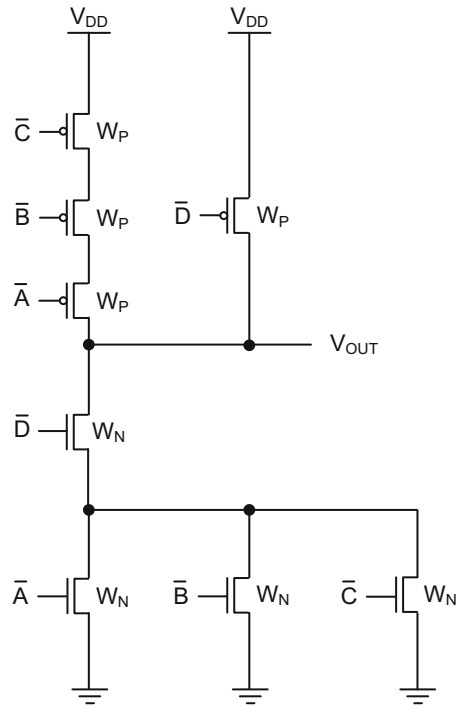


Fig. 3.15 Implementation of out $= A \,.\, B \,.\, C + D = \overline{(\overline{A} + \overline{B} + \overline{C}) \,.\, \overline{D}}$ (no output inverter is needed but all inputs need to be inverted)

Figure 3.16 shows the worst-case discharge and charge paths for the second implementation in Fig. 3.15. To discharge the output node, two equivalent NMOS resistors drain the output voltage towards 0 V as shown by the top figure in Fig. 3.16. Charging the output node, on the other hand, requires all three PMOS transistors to be turned on as shown by the bottom figure in Fig. 3.16.

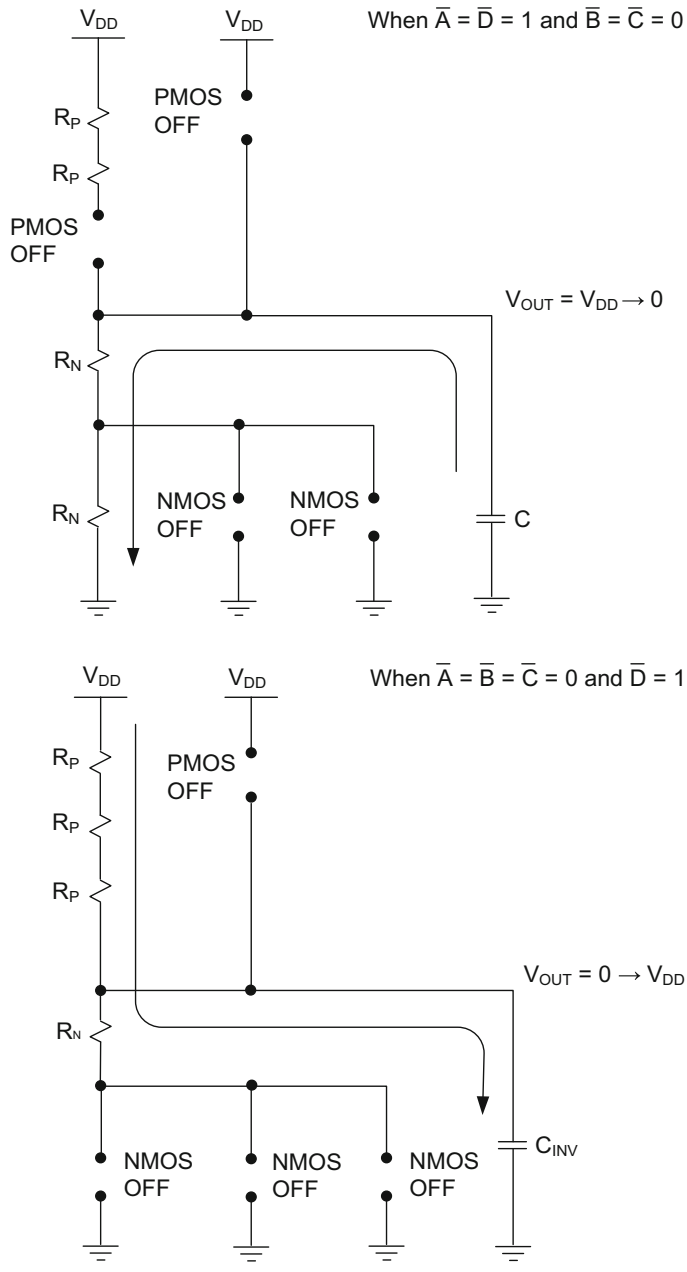


Fig. 3.16 Worst-case charge and discharge paths for out $= \mathrm{A} \,.\, \mathrm{B} \,.\, \mathrm{C} + \mathrm{D} = (\overline{\overline{\mathrm{A}} + \overline{\mathrm{B}} + \overline{\mathrm{C}}}) \,.\, \overline{\mathrm{D}}$

3.7 Rise and Fall Times

Rise time, T_R, is defined as the time interval during which the output rises from 20 to 80% of its final value as shown in Fig. 3.17. This value can be calculated analytically if the term R_P in Eq. 3.12 is replaced by R_{PEQ}, signifying a total equivalent PMOS resistance in the worst-case charge path. Therefore,

$$V_{OUT}(t) = V_{DD}\left[1 - \mathbf{exp}\left(-\frac{t}{R_{PEQ}C}\right)\right] \tag{3.21}$$

Here, C is the sum of all intrinsic and load capacitances at the output node. From this equation, 20% of V_{OUT} at $t = T_1$ becomes:

$$0.2V_{DD} = V_{DD}\left[1 - \mathbf{exp}\left(-\frac{T_1}{R_{PEQ}C}\right)\right]$$

or

$$T_1 = -R_{PEQ}C\ln(0.8) \tag{3.22}$$

Similarly, 80% of V_{OUT} at $t = T_2$ becomes:

$$0.8V_{DD} = V_{DD}\left[1 - \mathbf{exp}\left(-\frac{T_2}{R_{PEQ}C}\right)\right]$$

or

$$T_2 = -R_{PEQ}C\ln(0.2) \tag{3.23}$$

Then, using Eqs. 3.22 and 3.23 we can calculate the rise time, T_R:

$$T_R = T_2 - T_1 \approx 1.4\ R_{PEQ}C \tag{3.24}$$

Similar to rise time, the fall time is defined as the time interval during which the output falls from 80% to 20% of its final value as shown in Fig. 3.17. Rewriting Eq. 3.11, and replacing R_N in this equation by R_{NEQ} to signify the total equivalent NMOS resistance in the worst-case discharge path yields:

$$V_{OUT}(t) = V_{DD}\,\mathbf{exp}\left(-\frac{t}{R_{NEQ}C}\right) \tag{3.25}$$

Thus, 80% of V_{OUT} at $t = T_1$ becomes:

$$0.8V_{DD} = V_{DD}\,\mathbf{exp}\left(-\frac{T_1}{R_{NEQ}C}\right) \tag{3.26}$$

Similarly, 20% of V_{OUT} at $t = T_2$ becomes:

$$0.2V_{DD} = V_{DD}\,\mathbf{exp}\left(-\frac{T_2}{R_{NEQ}C}\right) \tag{3.27}$$

Extracting T_1 from Eq. 3.26 and T_2 from Eq. 3.27, and computing the fall time, T_F, yields:

$$T_F = T_2 - T_1 \approx 1.4\,R_{NEQ}C \tag{3.28}$$

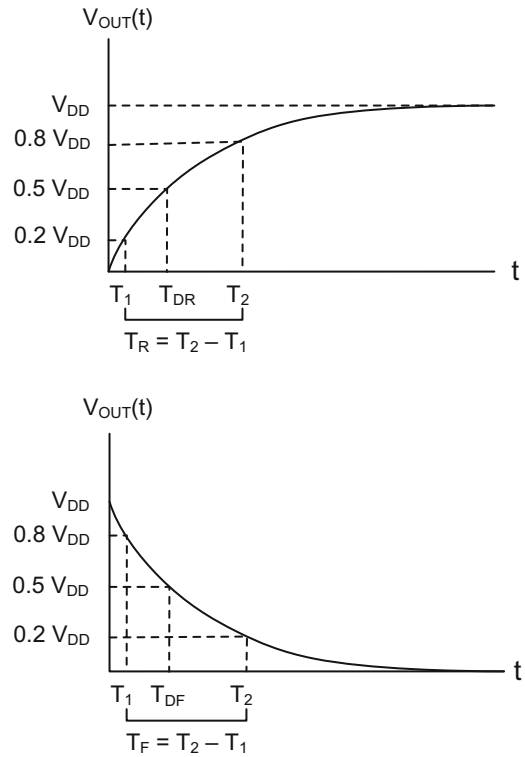


Fig. 3.17 Rise and fall times, rise and fall delays of a CMOS gate

3.8 Rise and Fall Delays

Rise delay, T_{DR}, is defined as the time interval between 50% mark of the input voltage and 50% mark of the rising output as shown in the top part of Fig. 3.17.

If the input voltage is assumed to make an abrupt transition from V_{DD} to 0 V at t = 0, then the 50% mark of the input voltage still resides at t = 0. Thus,

$$T_1 = 0 \tag{3.29}$$

For T_2, the output rises 50% of its final value. Therefore, we must refer to Eq. 3.12.

$$0.5V_{DD} = V_{DD}\left[1 - \mathbf{exp}\left(-\frac{T_2}{R_{PEQ}C}\right)\right]$$

or

$$T_2 = -R_{PEQ}C\ln(0.5) \tag{3.30}$$

Thus, the rise delay, T_{DR}, becomes:

$$T_{DR} = T_2 - T_1 \approx 0.7\ R_{PEQ}C \tag{3.31}$$

Similar to T_{DR}, the fall delay, T_{DF}, is computed by using Eq. 3.11. Graphically, T_{DF} is also shown in the bottom part of Fig. 3.17.

Again, $T_1 = 0$ because the input abruptly transitions at t = 0. For T_2, however, one can write:

$$0.5V_{DD} = V_{DD}\,\mathbf{exp}\left(-\frac{T_2}{R_{NEQ}C}\right)$$

Thus,

$$T_{DF} = T_2 - T_1 \approx 0.7\ R_{NEQ}C \tag{3.32}$$

Example 3.1 Assume that rise and fall times, and rise and fall delays of the circuit in Fig. 3.15 need to be computed.

From Eq. 3.24,

$$T_R \approx 1.4\ R_{PEQ}C = 1.4 \times 3\ R_PC = 4.2\ R_PC \tag{3.33}$$

From Eq. 3.28,

$$T_F \approx 1.4\ R_{NEQ}C = 1.4 \times 2\ R_NC = 2.8\ R_NC \tag{3.34}$$

From Eq. 3.31,

$$T_{DR} \approx 0.7\ R_{PEQ}C = 0.7 \times 3R_PC = 2.1\ R_PC \tag{3.35}$$

From Eq. 3.32,

$$T_{DF} \approx 0.7\ R_{NEQ}C = 0.7 \times 2R_NC = 1.4\ R_NC \tag{3.36}$$

The values of R_N and R_P can be calculated using the technology-dependent NMOS and PMOS transistor parameters, respectively. C is the value of the output capacitance.

Example 3.2 Again assume the complex gate in Fig. 3.15. Size each transistor width in this logic gate in terms of a minimum transistor width, W, to ensure $T_R = T_F$.

Since $T_R = T_F$, then $4.2\ R_P C = 2.8\ R_N C$
Thus,

$$1.5\ R_P = R_N \tag{3.37}$$

Substituting the values for R_N and R_P from Eq. 3.4 and Eq. 3.9 yields:

$$1.5\frac{K_P}{W_P} = \frac{K_N}{W_N} \tag{3.38}$$

But,

$$K_P = \frac{L_P}{\mu_P C_{OX}(V_{DD} - V_{TP})}$$

and

$$K_N = \frac{L_N}{\mu_N C_{OX}(V_{DD} - V_{TN})}$$

Assume that $\mu_N = 3\ \mu_P$ (due to the device technology), $L = L_P = L_N$ and $V_{TN} = V_{TP} \approx 0.2\ V_{DD}$
Then,

$$K_P = \frac{L}{\mu_P C_{OX}(0.8V_{DD})} \tag{3.39}$$

and

$$K_N = \frac{L}{3\mu_P C_{OX}(0.8V_{DD})} \tag{3.40}$$

Substituting Eqs. 3.39 and 3.40 into Eq. 3.38 yields:

$$1.5\frac{L}{\mu_P C_{OX}(0.8V_{DD})W_P} = \frac{L}{3\mu_P C_{OX}(0.8V_{DD})W_N}$$

$$\frac{1.5}{W_P} = \frac{1}{3W_N}$$

or

$$W_P = 4.5W_N$$

Assuming W_N = W (minimum geometry) yields:

$$W_P = 4.5W$$

Therefore, all NMOS transistors are sized W, and all PMOS transistors are sized 4.5W in order to ensure that the rise and fall times, computed through the worst-case critical paths, are equal to each other.

Example 3.3 Suppose the transistor widths of a two-input AND gate is given by the top figure in Fig. 3.18. The hole and electron mobilities are measured to be μ_P = 100 cm^2/Vsec and μ_N = 300 cm^2/Vsec, respectively. All transistor lengths are L = 0.1 μm, V_{DD} = 3 V, $V_{TN} = V_{TP}$ = 0.6 V and $C_{OX} = 10^{-8}$ F/cm^2.

The fall gate delay, T_{DF}, and the rise gate delay, T_{DR}, are computed as ($T_{DR1} + T_{DF2}$) and ($T_{DF1} + T_{DR2}$) respectively, and they are shown by the center and the bottom figures in Fig. 3.18. The worst-case gate delay is simply the larger of these two values.

First, let us compute ($T_{DR1} + T_{DF2}$). Since C_L is given, the computation always starts from the last stage. We know that:

$$R_N = \frac{K_N}{W_N} \text{ where } K_N = \frac{L}{\mu_N C_{OX}(V_{DD} - V_{TN})}$$

$$R_P = \frac{K_p}{W_p} \text{ where } K_p = \frac{L}{\mu_p C_{OX}(V_{DD} - V_{Tp})}$$

Substituting W_N = 10 μm and W_P = 30 μm from Fig. 3.18 and the physical device parameters given above yields $R_N = R_P \approx 1.4$ KΩ.

Then,

$$T_{DF2} = 0.7\, R_{N2}C_L = 0.7(1400)\, 0.1 \times 10^{-12} = 98\,\text{ps}$$

and

$$T_{DR1} = 0.7\, R_{P1}C_{INT}$$

Here, C_{INT} is the combination of NMOS and PMOS input gate capacitances of the inverter in Fig. 3.18.

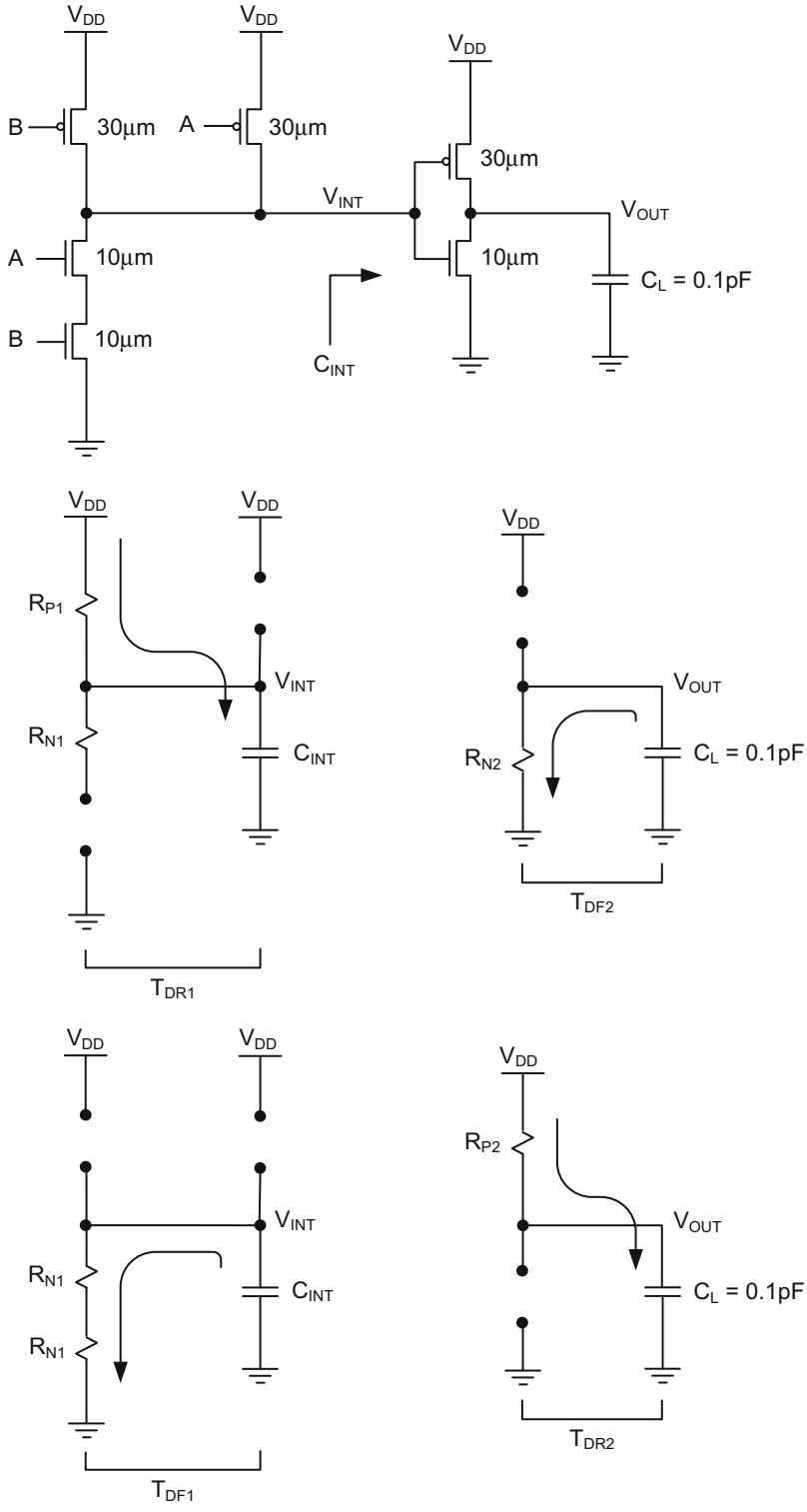


Fig. 3.18 Computation of worst-case gate delay of 2-input AND gate

Thus,

$$C_{INT} = C_{OX} L (W_N + W_P) = 10^{-8} \times 0.1 \times 10^{-4} \times (10 + 30) \times 10^{-4} = 0.4\text{fF}$$
$$T_{DR1} = 0.7(1400)4 \times 10^{-15} = 3.9\,\text{ps}$$

Consequently, $T_{DR1} + T_{DF2} = 0.4 + 98 \approx 98\,\text{ps}$
The computation of (T_{DF1} + T_{DR2}) starts from calculating T_{DR2} first.

$$T_{DR2} = 0.7\ R_{P2}C_L = 0.7(1400)\,0.1 \times 10^{-12} = 98\,\text{ps}$$
$$T_{DF1} = 0.7\ 2R_{N1}C_{INT} = 0.7(2 \times 1400)\ 0.4 \times 10^{-15} = 0.8\,\text{ps}$$

Consequently, $T_{DF1} + T_{DR2} = 98 + 0.8 \approx 99\,\text{ps}$
Therefore, the worst-case gate delay for this AND gate is T_D = 99 ps.

Review Questions

1. Implement the following functions using CMOS circuits

(a) Implement the following function with a two-stage CMOS circuit (with an output inverter).

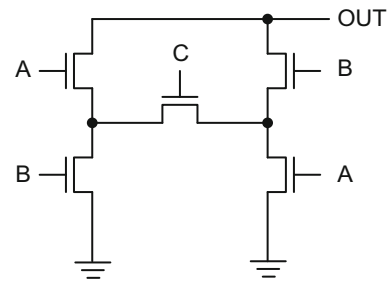
$$OUT = (A + B + C) . \overline{D}$$

(b) Implement the following function with a single stage CMOS circuit (without an output inverter).

$$OUT = (A + B + C) . \overline{D}$$

2. The NMOS tree of a CMOS circuit is given below.

(a) Find the logic function of this circuit at the out terminal.
(b) Determine the PMOS tree for this circuit. Explain the configuration steps clearly.



3. Design the CMOS gate that implements the following function:

$$OUT = \overline{A \oplus B}$$

(a) Draw the circuit schematic without any output inverter.
(b) Size all the transistors in this circuit such that $T_R = 3T_F$. The minimum geometry is W.

4. The following function is given:

$$OUT = A + B . \overline{(C + D + E)}$$

Design a single-stage CMOS circuit with $T_{DR} = 2T_{DF}$. Determine all transistor widths in terms of minimum geometry, W.

5. The following function is given:

OUT = (A + B + C)

Design a two-stage CMOS circuit that maintains $T_R = 2T_F = 500$ ps at all nodes (internal or output) for a load capacitor of 100fF. Find all transistor widths in μm.

Use the technology below:

$C_{OX} = 10^{-8}$ F/cm^2
L = 0.25 μm
$V_{DD} = 3$ V
$V_{TN} = V_{TP} = 0.5$ V
$\mu_N = 200$ cm^2/Vsec
$\mu_P = 100$ cm^2/Vsec

6. Implement one-bit SUM and C_{OUT} (carry-out) functions in an integrated CMOS logic gate with uninverted inputs, A, B, and C_{IN} (carry-in):

$$SUM = A \oplus B \oplus C_{IN}$$
$$C_{OUT} = A \,.\, B + C_{IN} \,.\, (A + B)$$

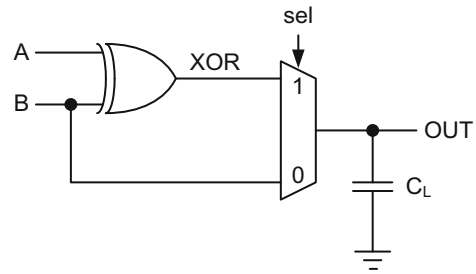
The design criterion requires that T_{DR} and T_{DF} are equal to 400 ps in each stage of this CMOS circuit. Size the transistors in the CMOS circuit using the following technology:

C_{LOAD} = 100fF = 100×10^{-15}F (placed both at the sum and carry-out nodes)
$V_{DD} = 3$ V
$V_{TN} = V_{TP} = 0.5$ V
$\mu_N = 300$ cm^2/Vsec
$\mu_P = 100$ cm^2/Vsec
L = 0.25 μm
$C_{OX} = 10^{-8}$ F/cm^2

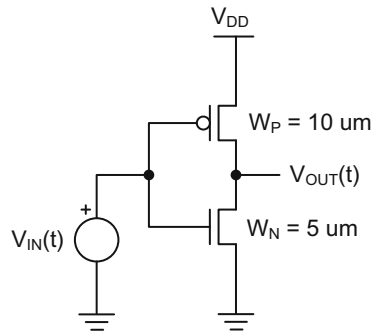
7. Design the following circuit that drives C_L = 500fF. In order to be able to drive such a large capacitance, the 2-1 MUX output must have an inverter stage. Start the design from the last stage. Inverted and uninverted inputs may be used during the design in order to minimize the number of transistors. Size the transistors such that the rise and fall times at all output nodes are 400 ps. Use the device technology specs below:

$V_{DD} = 3$ V
$V_{TN} = 0.5$ V
$V_{TP} = 0.5$ V
$C_{OX} = 10^{-8}$ F/cm^2

$L = 0.25\ \mu m$
$\mu_N = 600\ cm^2/Vsec$
$\mu_P = 200\ cm^2/Vsec$



8. An inverter is given below.



The NMOS and PMOS transistors are fabricated using the following technology:

$V_{DD} = 3\ V$
$V_{TN} = V_{TP} = 0.6\ V$
$\mu_N = 1200\ cm^2/Vsec$
$\mu_P = 600\ cm^2/Vsec$
$C_{OX} = 6.9 \times 10^{-7}\ F/cm^2$
$L = 0.25\ \mu m$

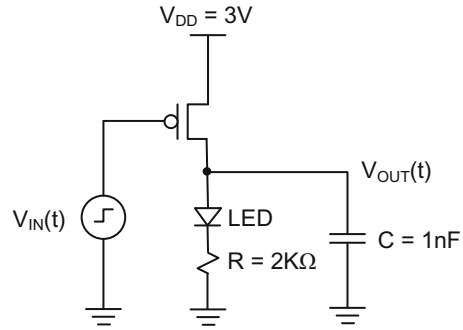
The current through a MOSFET is defined as:

$$I_D = \frac{\mu C_{OX} W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

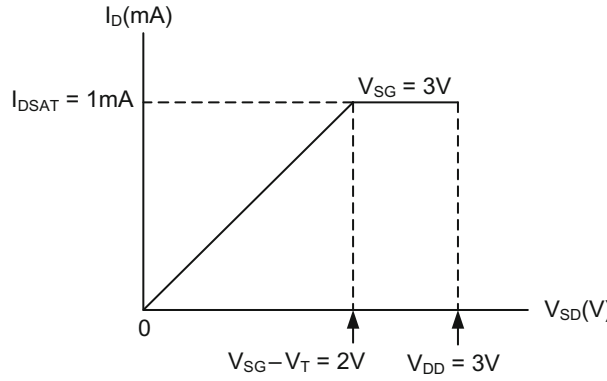
(a) Compute the static DC current when $V_{IN} = 2\ V$.
(b) Compute the output voltage when $V_{IN} = 2\ V$.

Consider the equivalent circuits of NMOS and PMOS transistors at this bias condition.

9. The circuit below operates a Light Emitting Diode (LED):



The approximate I-V characteristics of the transistor are given below:

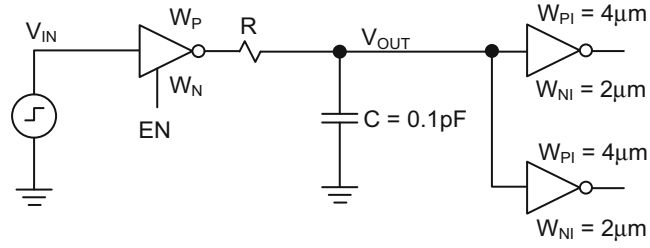


The LED needs to have 0.5 mA current and 1 V across its terminals to turn on. Otherwise, it does not conduct current. The input voltage, $V_{IN}(t)$, is initially at 3 V, but switches to 0 V at t = 0. The initial condition at V_{OUT} is 0 V.

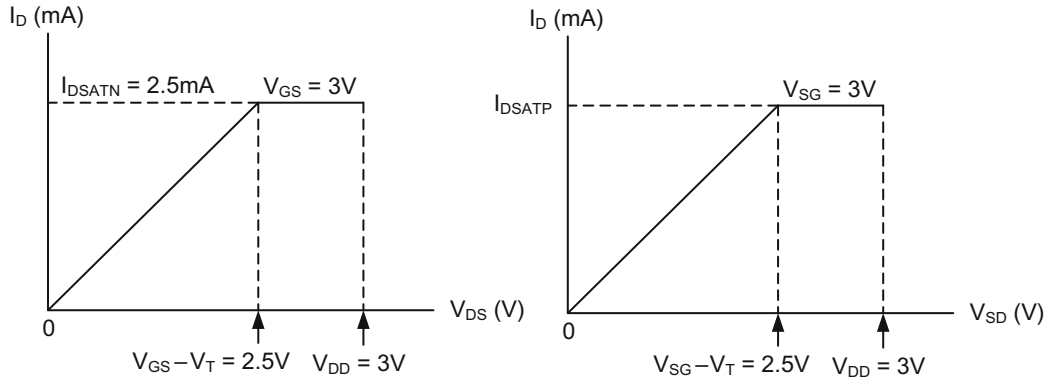
Using the I-V characteristics of the transistor and the component values in the circuit schematic above, derive the expression for $V_{OUT}(t)$. Plot $V_{OUT}(t)$ as function of time.

10. The circuit below illustrates a tri-state inverter driving a long wire with an equivalent resistance of R and capacitance of C.

At the end of the wire, two inverters, composed of a PMOS transistor with W_{PI} = 4 μm and NMOS transistor with W_{NI} = 2 μm, create a capacitive load.



NMOS and PMOS transistor I-V characteristics are shown below:

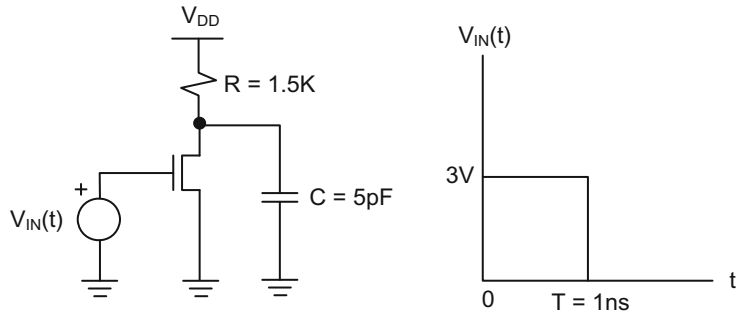


(a) If rise and fall times at V_{OUT} are 2 ns, find the actual wire resistance in ohms.
(b) What is the saturation current of the PMOS transistor in the tri-state inverter?

Use the following technology:

V_{DD} = 3 V
C_{OX} = 10^{-7} F/cm^2
L = 0.25 μm

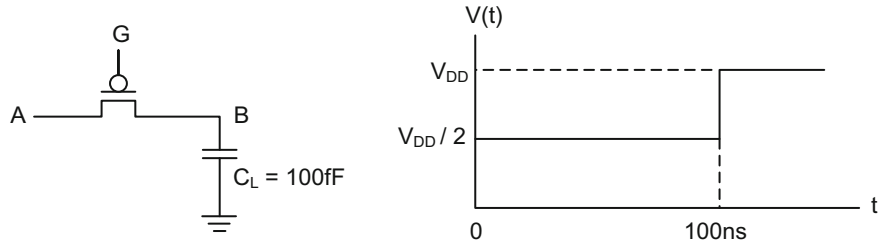
11. The following circuit is given:



Assuming that NMOS transistor is in the linear region when it is turned on, find the output voltage of the circuit and plot it using the following device parameters:

μ_N = 100 cm^2/Vsec
C_{OX} = 6.9 × 10^{-7} F/cm^2
L = 0.25 μm
W = 10 μm
V_{DD} = 3 V
V_{TN} = 0.6 V

12. The waveform, V(t), is applied to G terminal of the circuit below.



A constant voltage, V_{DD}, is applied to A.
PMOS I_D-V_{SD} characteristics are given below:

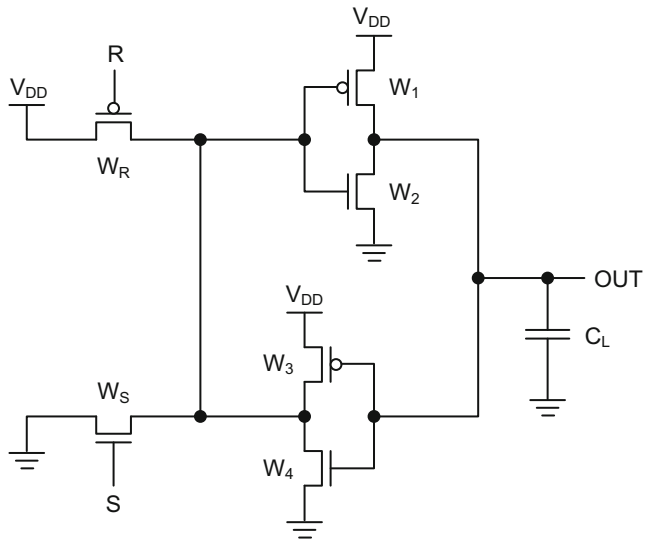
$$I_D = \frac{\mu_P C_{OX} W}{L}(V_{SG} - V_T)V_{SD} \text{ if } V_{SD} < (V_{SG} - V_T)$$
$$I_D = \frac{\mu_P C_{OX} W}{2L}(V_{SG} - V_T)^2 \text{ if } V_{SD} > (V_{SG} - V_T)$$

If V_{DD} = 4 V, V_T = 1 V, W = 5 μm, L = 0.25 μm and $\mu_P C_{OX} = 10^{-6}$ A/V^2, plot the waveform at B.

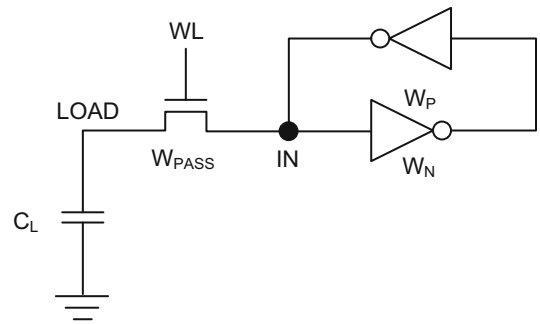
13. A Set-Reset (SR) latch is given below. This latch should be designed to drive a 100fF capacitive load. The rise and fall times at each node in the circuit are 500 ps. The device technology specs are as follows:

V_{DD} = 3 V
V_{TN} = 0.5 V
V_{TP} = 0.5 V
$C_{OX} = 10^{-8}$ F/cm^2
L = 0.25 μm
μ_N = 600 cm^2/Vsec
μ_P = 200 cm^2/Vsec

Size all the transistors in the circuit. To prevent contention between any two transistors, make sure to adjust the resistance of the transistor being sized to be about 20% of the resistance of the contending transistor.



14. A single ended SRAM cell is given below:



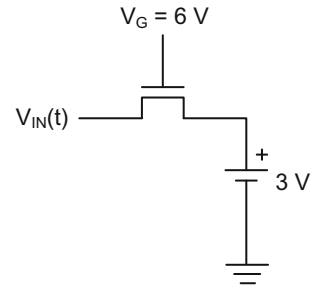
The device technology parameters for the NMOS and PMOS transistors are given below.
$C_{OX} = 7 \times 10^{-8}$ F/cm^2
$V_{DD} = 3$ V
$L = 0.25$ μm
$\mu_N = 200$ cm^2/Vsec
$\mu_P = 100$ cm^2/Vsec
$V_{TN} = V_{TP} = 0.6$ V

When WL = 0 V and the pass-gate NMOS transistor, W_{PASS}, is off, the voltage at LOAD node is 3 V, and the voltage at IN node is 0 V (cell stores logic 0). Transistor sizes in both inverters are $W_P = 2$ μm and $W_N = 1$ μm in the SRAM cell.

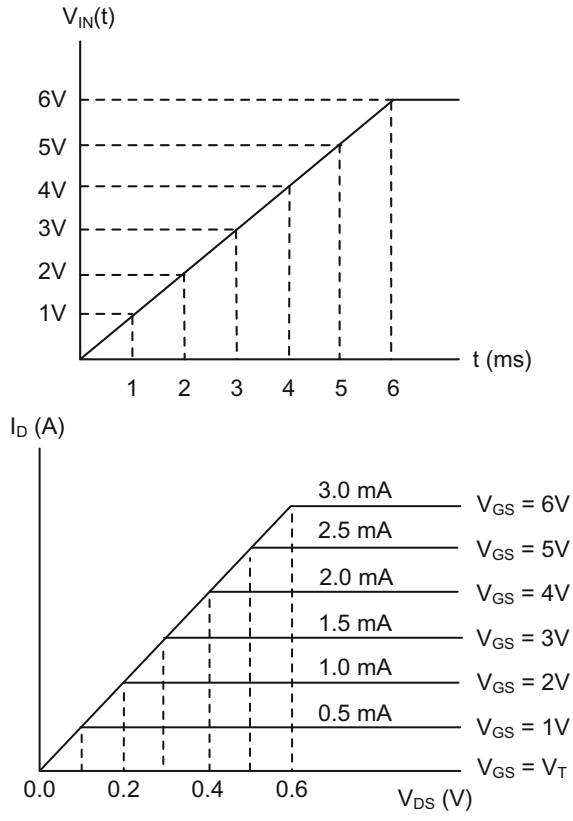
(a) Assuming that the pass-gate NMOS transistor acts as a switch with a channel resistance of 0 Ω when it is on, calculate the maximum allowed load capacitance value C_L such that the stored bit in the SRAM cell does not accidentally change from logic 0 to 1.

(b) What is the relationship(s) between transistor sizes to keep the logic state the same in the cell when the pass-gate NMOS transistor has a finite channel resistance when it is turned on? Assume identical rise and fall times at the internal nodes.

15. An NMOS transistor establishes the pass-gate functionality in the circuit below:

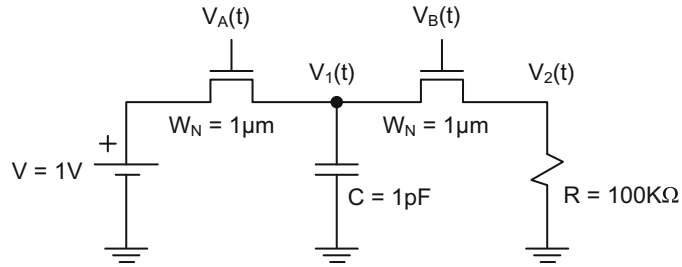


The input signal, $V_{IN}(t)$, and I_D-V_{DS} for this NMOS transistor are shown below.

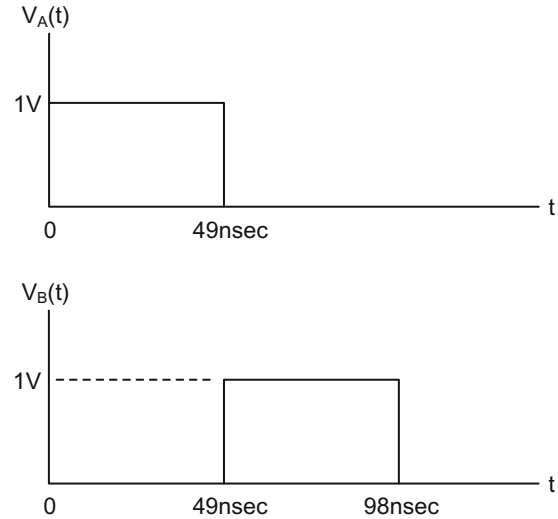


Calculate I_D from the data given above and plot the absolute value of I_D as a function of time.

16. The circuit given below includes two pass-gate NMOS transistors connected in series.



Here, $V_A(t)$ and $V_B(t)$ are the voltages applied at the gates of the NMOS transistors as shown below:



Compute the nodal voltages, $V_1(t)$ and $V_2(t)$, as a function of time using the device technology below:

V_{DD} = 1 V
V_{TN} = 0.3 V
L = 0.1 μm
μ_N = 200 cm^2/Vsec
C_{OX} = 7 × 10^{-8} F/cm^2