TTL Logic and CMOS-TTL Interface

4

4.1 TTL Inverter

Transistor-Transistor-Logic (TTL) is still used in limited capacity in discrete ICs due to its ability to deliver (or sink) large currents. However, power consumption, slow speed and the cost of fabrication are its main drawbacks. All TTL logic gates are composed of three stages. The simplest TTL logic gate, TTL inverter, is shown in Fig. 4.1.

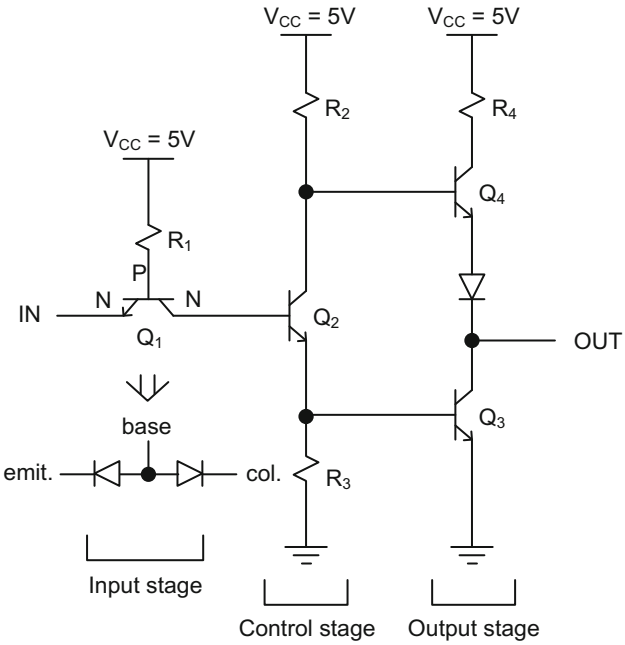

Fig. 4.1 A simplified TTL inverter

The input stage of this gate contains only a single transistor, Q_1. This transistor is equivalent to two back-to-back diodes as shown in the inset of Fig. 4.1, and this

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configuration directs the current flow either towards the IN terminal or towards the control stage to activate Q_2 depending on the logic value at the input.

The control stage contains Q_2. Its function is to supply part of its emitter current to saturate Q_3 or turn off this transistor.

The output stage, also called totem-pole configuration, consists of Q_3 and Q_4. Q_3 absorbs all the current (sink current) from an output load. Q_4 supplies current (source current) to an output load. Supply voltage for any commercially available TTL stage is usually 5 V.

TTL Inverter When IN = 5 V

When the input voltage at the IN node is raised to 5 V, there will be no voltage drop across the diode, D_1 (corresponding to the emitter-base junction of Q_1). As a result, D_1 turns off as shown in Fig. 4.2.

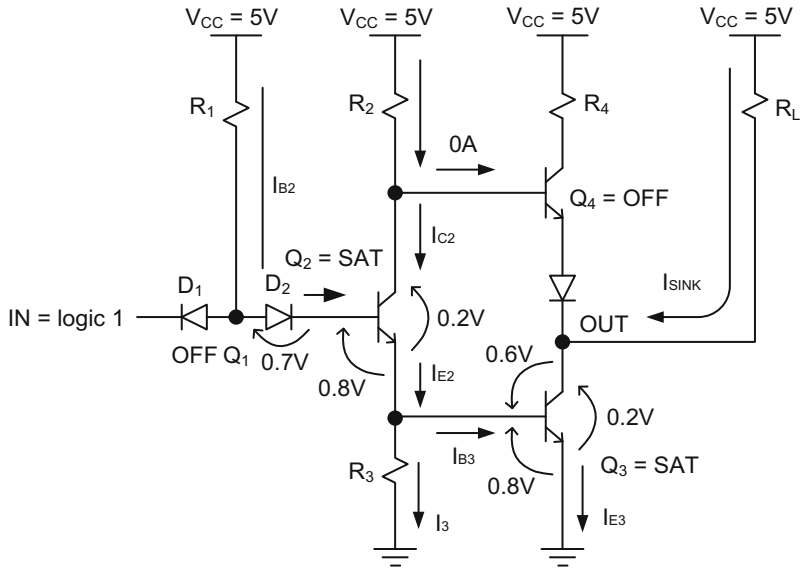


Fig. 4.2 Currents and voltages of the TTL inverter when IN = logic 1

Therefore, the current from the voltage supply, V_{CC}, directly flows into the base of Q_2 through D_2 (corresponding to the collector-base junction of Q_1), forming the base current for Q_2, I_{B2}, and driving this transistor into saturation.

When Q_2 is in the saturation region, its collector current, I_{C2}, combines with I_{B2}, and forms the emitter current for Q_2, $I_{E2} = I_{B2} + I_{C2}$. The majority of I_{E2} flows into the base of Q_3 and drives this transistor into saturation. The remaining part of I_{E2} flows through R_3, and biases the base-emitter junction of Q_3 with 0.8 V.

As a result of this scenario, the voltage drop between the base of Q_4 and the output terminal becomes 0.2 + 0.6 = 0.8 V. However, this potential difference is not sufficient to turn on Q_4 and the diode at the output stage simultaneously since they require at least 0.8 + 0.7 = 1.5 V. Thus, Q4 turns off.

As a result, I_{C3} becomes the "sink" current and absorbs all the output current from an external resistor, R_L, as shown in Fig. 4.2. This current is also called I_{OL}, corresponding to the low output current when the output is equal to V_{OL}.

TTL Inverter When IN = 0 V

When input voltage at IN is lowered to 0 V, current flows through the diode, D_1 (corresponding to the emitter-base junction of Q_1), and turns on the diode. The voltage developed across this diode, 0.7 V, then becomes equal to the sum of the voltage drops across D_2 (corresponding base-collector junction of Q_1), the base-emitter junction of Q_2 and the base-emitter junction of Q_3. However, 0.7 V is not enough to saturate the transistors, Q_2 and Q_3, and turn on the diode at the same time as shown in Fig. 4.3.

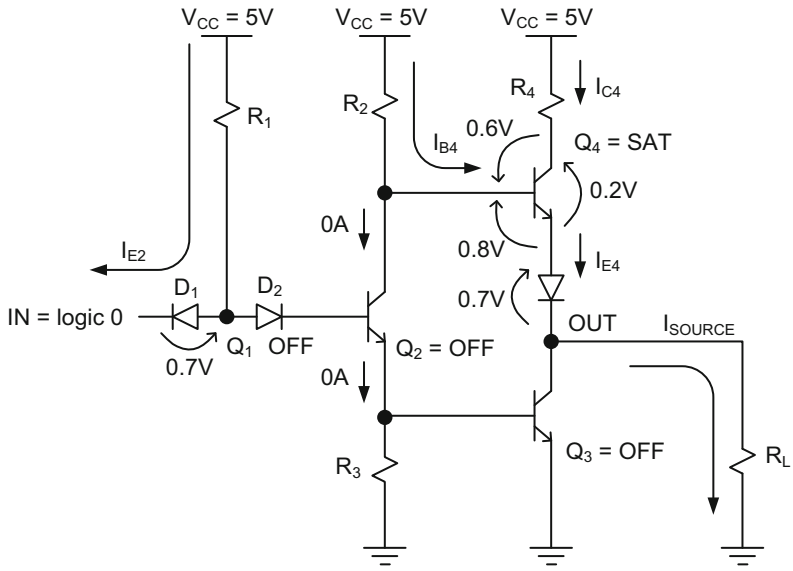


Fig. 4.3 Currents and voltages of the TTL inverter when IN = logic 0

Since Q_2 stays off, the supply current, I_{B4}, flows into the base of Q_4 and saturates this transistor. The collector current of Q_4, I_{C4}, combines with I_{B4} to form the emitter current for Q_4, I_{E4}. This current becomes the "source" current and flows into an external load resistor, R_L, as shown in Fig. 4.3. This current is also called I_{OH}, corresponding to the high output voltage, V_{OH}. However, V_{OH} never reaches the full supply voltage of 5 V, but stays around 3.5 V due to the combined voltage drop between V_{CC} and the OUT terminal, namely $R_4\ I_{C4} + 0.2 + 0.7 \approx 1.5$ V.

Example 4.1 There are two ways for a TTL inverter to drive an LED. The circuit configuration depends on the current requirement of the LED, and the relative values of I_{OH} and

I_{OL} given in the manufacturer's datasheet. If the LED requires high current, and I_{OH} happens to be much higher than I_{OL} in the datasheet, then the best way to connect the LED is between the output terminal and the ground as shown in Fig. 4.4. As a result, I_{OH} is used to turn on the LED.

The series resistance, R_L, is computed as follows:

$$R_L = \frac{(V_{OH} - V_{LED})}{I_{OH}} \tag{4.1}$$

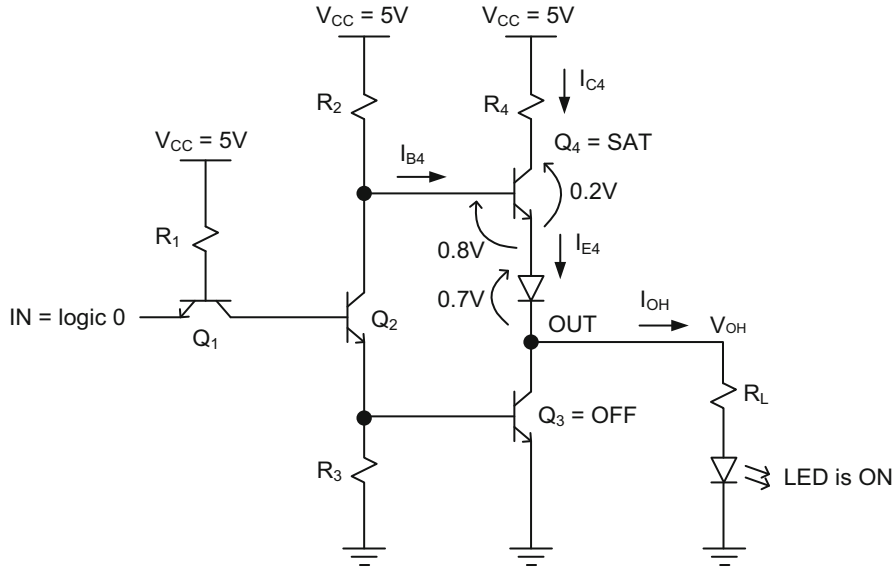


Fig. 4.4 TTL inverter driving LED if I_{OH} is much greater than I_{OL}

In this equation, V_{LED} is the voltage drop across the LED.

If the LED requires high current and the TTL manufacturer's datasheet specifies that I_{OL} is much higher than I_{OH}, then the better circuit configuration would be to connect the LED between the supply voltage and the OUT terminal as shown in Fig. 4.5. That way, I_{OL} of the TTL inverter supplies all the current the LED needs.

This time, R_L becomes:

$$R_L = \frac{(V_{CC} - V_{LED} - V_{OL})}{I_{OL}} \tag{4.2}$$

If the LED's current requirement is low and comparable to I_{OH} or I_{OL}, then either circuit configuration in Figs. 4.4 or 4.5 can be used to turn on the LED.

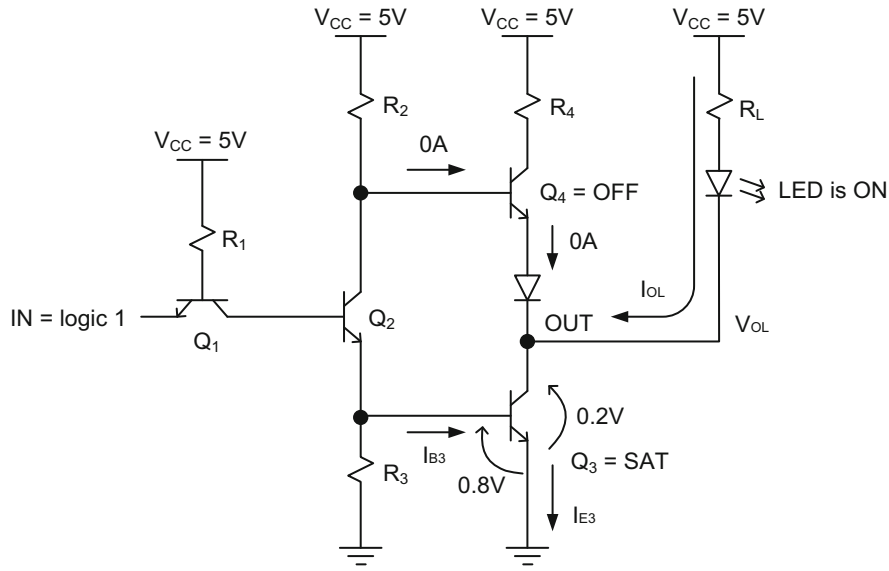


Fig. 4.5 TTL inverter driving LED if I_{OL} is much greater than I_{OH}

4.2 TTL Inverter with Open Collector

If the TTL inverter's I_{OL} is much higher than I_{OH}, the output transistor Q_4 may not be necessary at all to operate an LED or some other two-terminal device. This reduces the overall device count in the inverter and forms a much simpler circuit called open-collector inverter as shown in Fig. 4.6. With open-collector configuration, the high logic level also reaches to the full voltage supply value of 5 V instead of staying at 3.5 V.

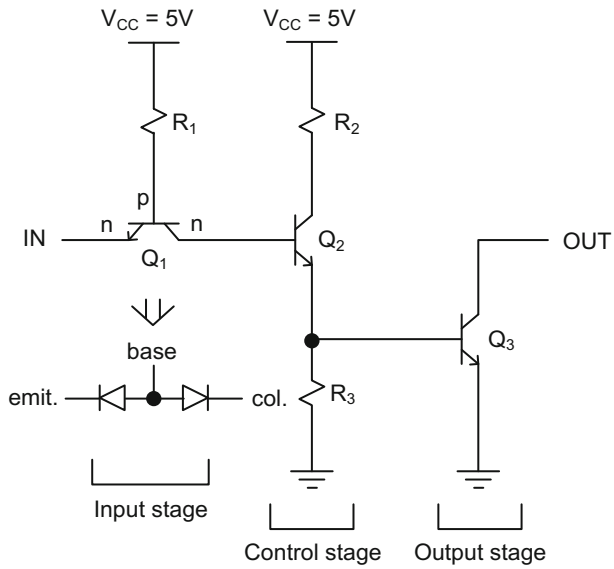


Fig. 4.6 Open-collector TTL inverter

The operation of open-collector inverter is similar to the operation of a common TTL inverter. However, the open collector of Q_3 will always need a pull-up resistor to operate properly.

Figure 4.7 describes the operation of this logic gate with a pull-up resistor when IN is connected to 5 V. The diode corresponding to the emitter-base junction of Q_1 turns off because there is 0 V across this junction. Q_2 goes into the saturation region with a current flowing in its base, I_{B2}. A large portion of Q_2's emitter saturation current, I_{E2}, also flows into the base of Q_3 and causes this transistor to go into saturation provided that Q_3 is biased properly with an external load resistance, R_L. The output voltage becomes V_{OL}, which is in the order of 0.2 V. I_{OL} becomes the collector current of Q_3. R_L is determined in terms of V_{OL} and I_{OL} according to the following equation:

$$R_L = \frac{(V_{CC} - V_{OL})}{I_{OL}} \tag{4.3}$$

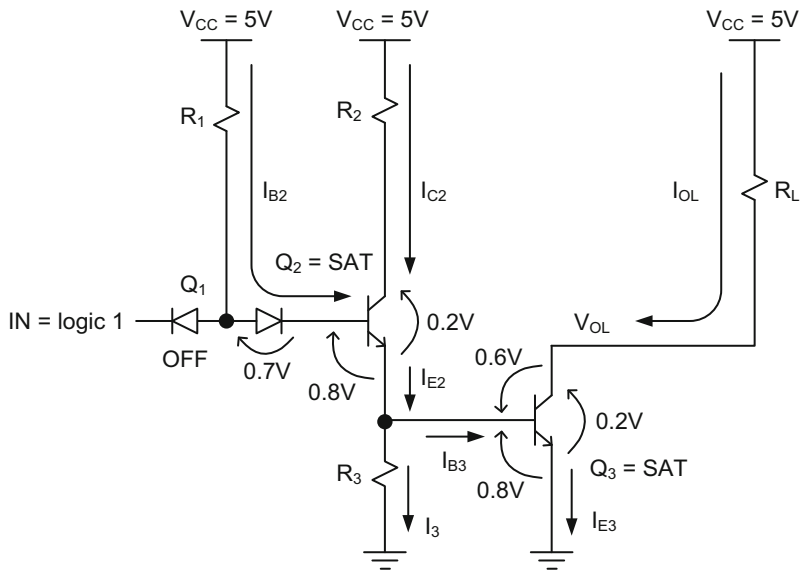


Fig. 4.7 Open-collector TTL inverter driving a CMOS gate when IN = logic 1

When IN = 0 V, the diode corresponding to the emitter-base junction of Q_1 turns on as shown in Fig. 4.8. However, the base of Q_1, now standing at 0.7 V, will not be sufficient to turn on the transistors, Q_2, Q_3 and the diode corresponding to the collector-base of Q_1. The output node is pulled up to V_{CC}. I_{OH} through R_L becomes 0 A.

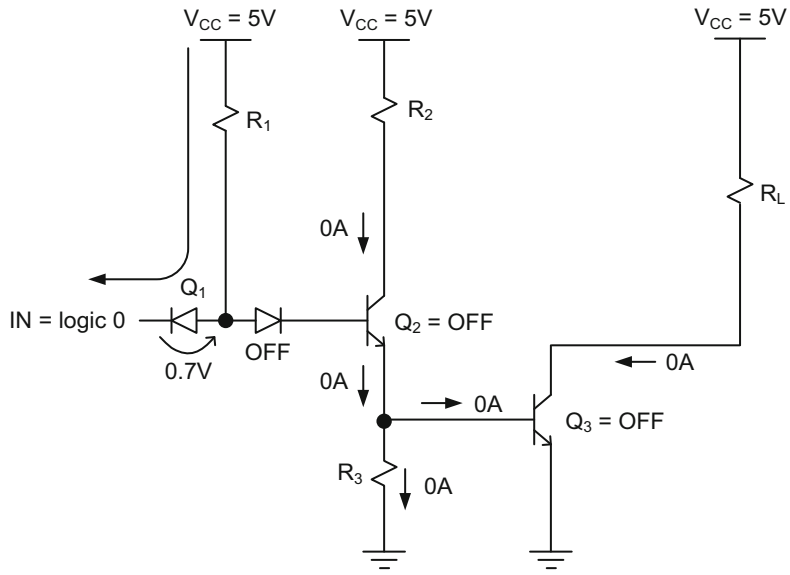


Fig. 4.8 Open-collector TTL inverter driving a CMOS gate when IN = logic 0

Example 4.2 Assume the output of the open-collector inverter in Fig. 4.7 includes an LED in series with R_L. The load resistor now serves two purposes: it limits the current through LED and biases Q_3 when this transistor needs to be driven into saturation. Applying IN = 5 V in Fig. 4.9 causes both Q_2 and Q_3 to be in saturation region which produces OUT = V_{OL}. The resulting I_{OL} turns on the LED.

$$I_{OL} = \frac{(V_{CC} - V_{LED} - V_{OL})}{R_L} \tag{4.4}$$

Then, R_L is calculated as

$$R_L = \frac{(V_{CC} - V_{LED} - V_{OL})}{I_{LED}} \tag{4.5}$$

where $I_{LED} = I_{OL}$.

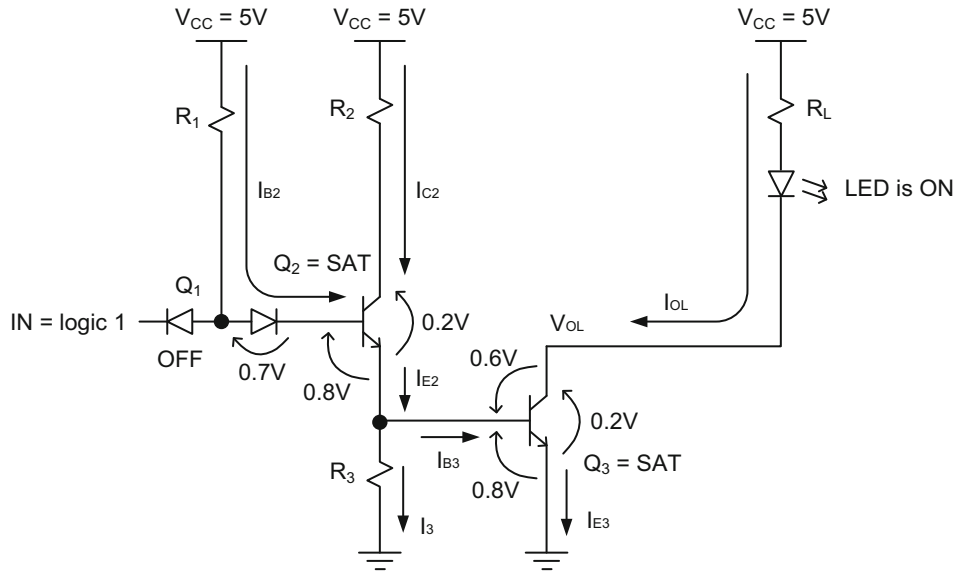


Fig. 4.9 Open-collector TTL inverter driving an LED when IN = logic 1

When IN = 0 V is applied to the open-collector TTL inverter input, both Q_2 and Q_3 turn off, resulting no current flow through the LED as shown in Fig. 4.10. The LED turns off.

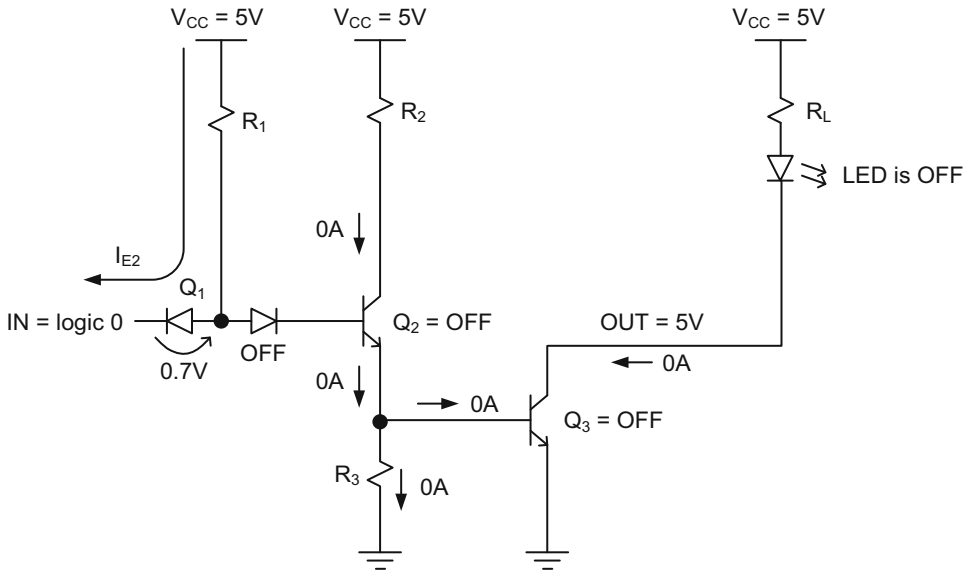


Fig. 4.10 Open-collector TTL inverter driving an LED when IN = logic 0

4.3 Two-Input TTL Nand Logic Gate

Two-input TTL NAND gate is shown in Fig. 4.11. In this figure, Q_1 produces two emitter ports each of which is connected to separate external inputs, IN_1 and IN_2.

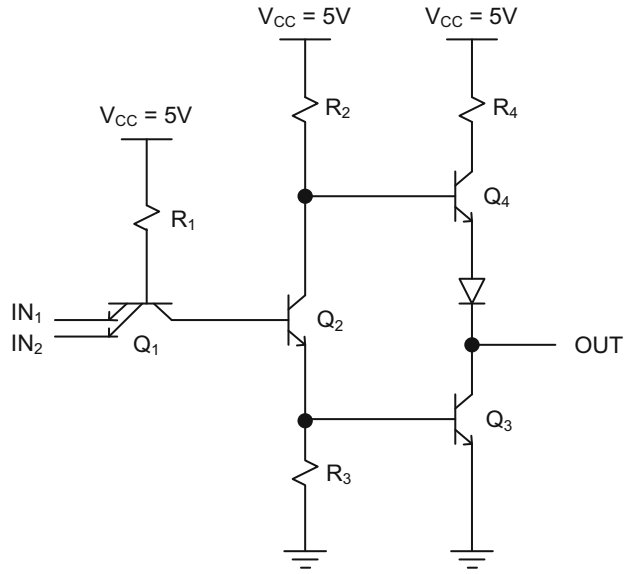


Fig. 4.11 Two-input TTL NAND gate

Figure 4.12 shows both inputs of the two-input TTL NAND gate connected to 0 V. In this figure, Q_1 has been transformed into three discrete diodes, D_1, D_2 and D_3, to make the circuit analysis simpler. When $IN_1 = IN_2 = 0$ V, both D_1 and D_3 turn on. However, the voltage drop across either diode will not be sufficient to turn on D_2, Q_2 and Q_3 as discussed earlier. Q_4 is driven into saturation and supplies I_{OH} to an output load. The output of the NAND gate transitions to logic 1.

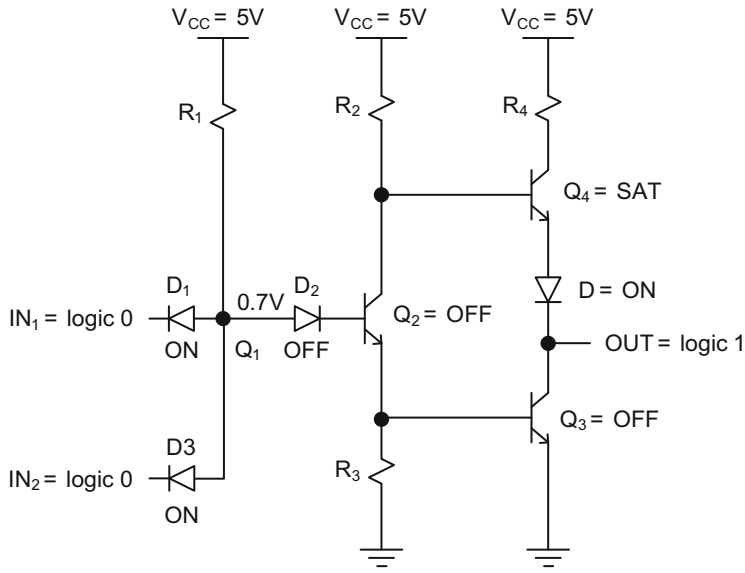


Fig. 4.12 Two-input TTL NAND gate when $IN_1 = IN_2 =$ logic 0

When one of the inputs of the NAND gate is connected to ground while the other tied to logic 1, only D_3 turns on. Both Q_2 and Q_3 turn off as shown in Fig. 4.13. As a result, Q_4 is driven into saturation and the output transitions to logic 1.

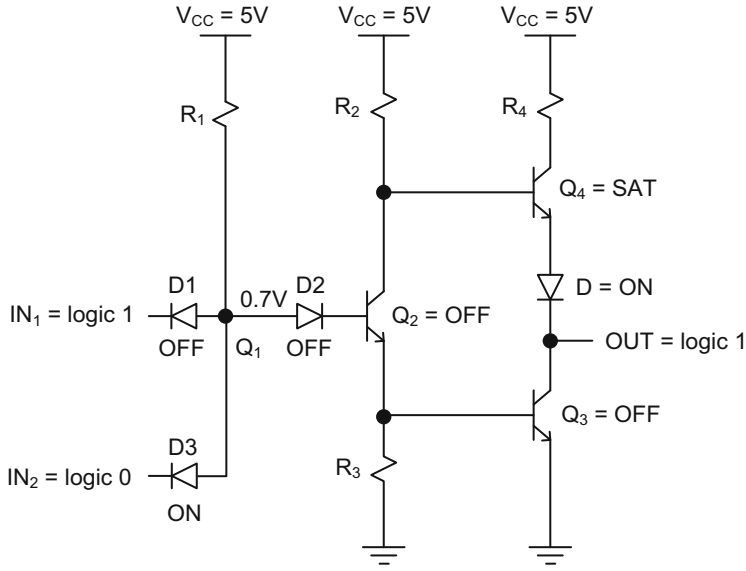


Fig. 4.13 Two-input TTL NAND gate when one of the inputs is at logic 0 ($IN_2 =$ logic 0)

When both inputs of the NAND gate are tied to logic 1, both D_1 and D_3 turn off as shown in Fig. 4.14. The current through R_1 saturates Q_2, and Q_2's emitter current saturates Q_3. The sum of voltage drops across the collector-emitter junction of Q_2 and collector-base junction of Q_3 now reaches about 0.8 V. However, this voltage becomes insufficient to turn on Q_4 and the output diode. As a result, the output terminal is pulled low to about 0.2 V and sinks any current from an external load.

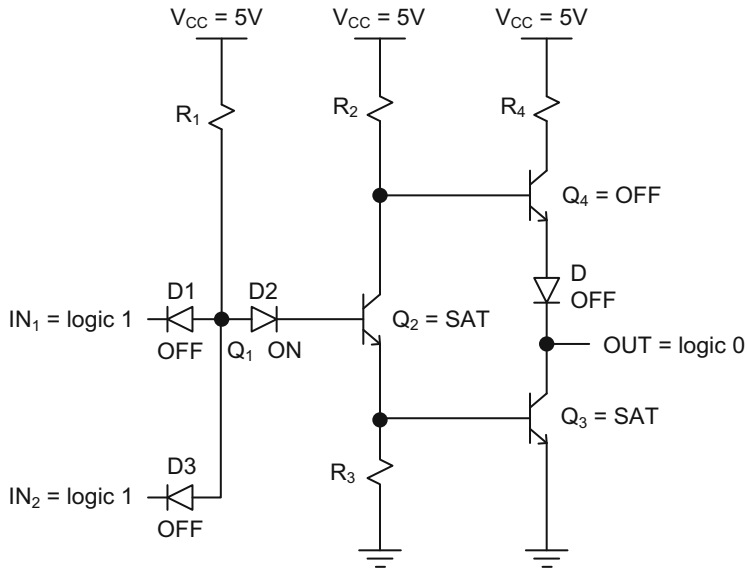


Fig. 4.14 Two-input TTL NAND gate when $IN_1 = IN_2 =$ logic 1

4.4 Two-Input TTL NOR Logic Gate

Two-input TTL NOR gate is shown in Fig. 4.15. This circuit contains two extra transistors, Q_{11} and Q_{12}, at the input, and another two, Q_{21} and Q_{22}, at the control stage, to produce the NOR behavior.

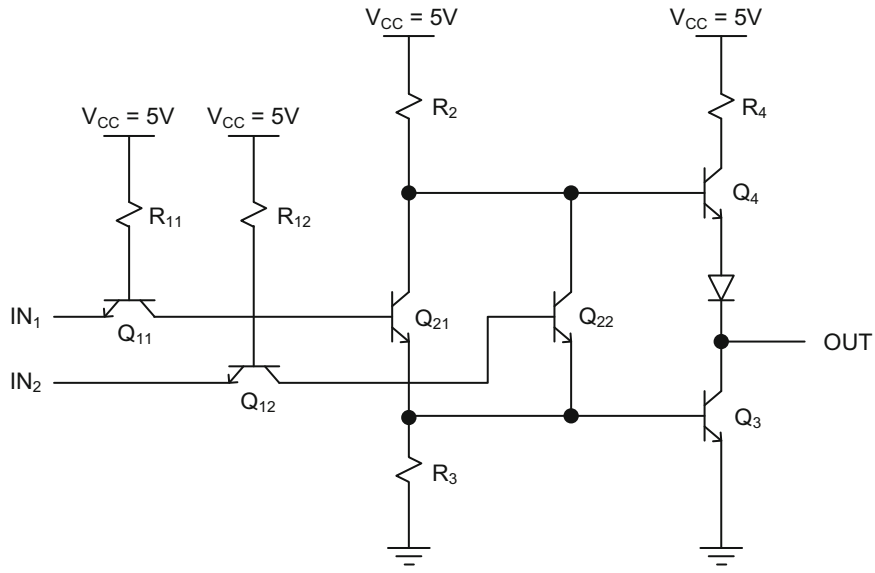


Fig. 4.15 Two-input TTL NOR gate

When both IN_1 and IN_2 are grounded, the diodes, D_1 and D_3 corresponding to the emitter-base junctions of Q_{11} and Q_{12}, turn on as shown in Fig. 4.16. The voltage drop across either of these diodes will not be sufficient to turn on D_2, D_4, Q_{21}, Q_{22} and Q_3. The transistor, Q_4, goes into saturation because a large current is supplied to the base of this transistor through R_2. As a result, the emitter current of Q_4 produces a source current to an external load, and the output of the gate is pulled up to logic 1.

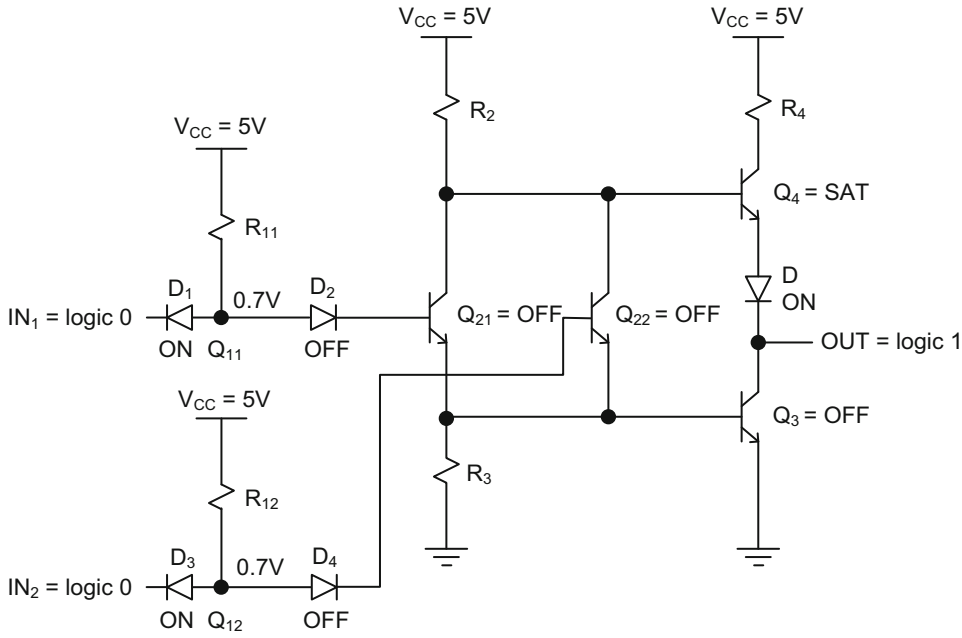


Fig. 4.16 Two-input TTL NOR gate when $IN_1 = IN_2 =$ logic 0

When IN_1 is tied to logic 1 and IN_2 at logic 0 (or vice versa), the diode, D_1 corresponding to the emitter-base of Q_{11}, turns off because there is 0 V across it as shown in Fig. 4.17. Q_{21} goes into saturation because a large current is supplied to the base of this transistor through R_{11} but Q_{22} stays off. A large portion of Q_{21}'s emitter saturation current flows into the base of Q_3 and saturates this transistor. In the mean time, the output diode D and Q_4 turn off, leaving Q_3 in charge of sinking all current from an external load and pulling the output terminal to logic 0.

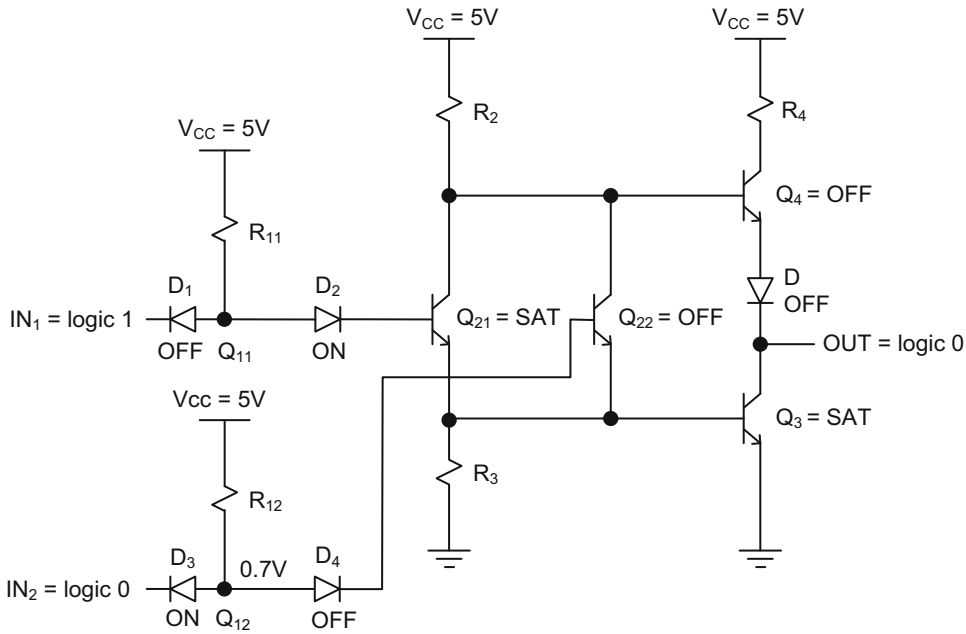


Fig. 4.17 Two-input TTL NOR gate when one of the inputs is at logic 0 (IN_2 = logic 0)

When IN_1 and IN_2 are at logic 1, the diodes, D_1 and D_3 corresponding to the emitter-base junctions of Q_{11} and Q_{12}, turn off as shown in Fig. 4.18. However, both Q_{21} and Q_{22} go into saturation because of large currents supplied to the base of these transistors through R_{11} and R_{12}, respectively. The sum of emitter saturation currents from Q_{21} and Q_{22} drive Q_3 into saturation and lower the output voltage to logic 0. Now, Q_3 is able to sink any current from an external load.

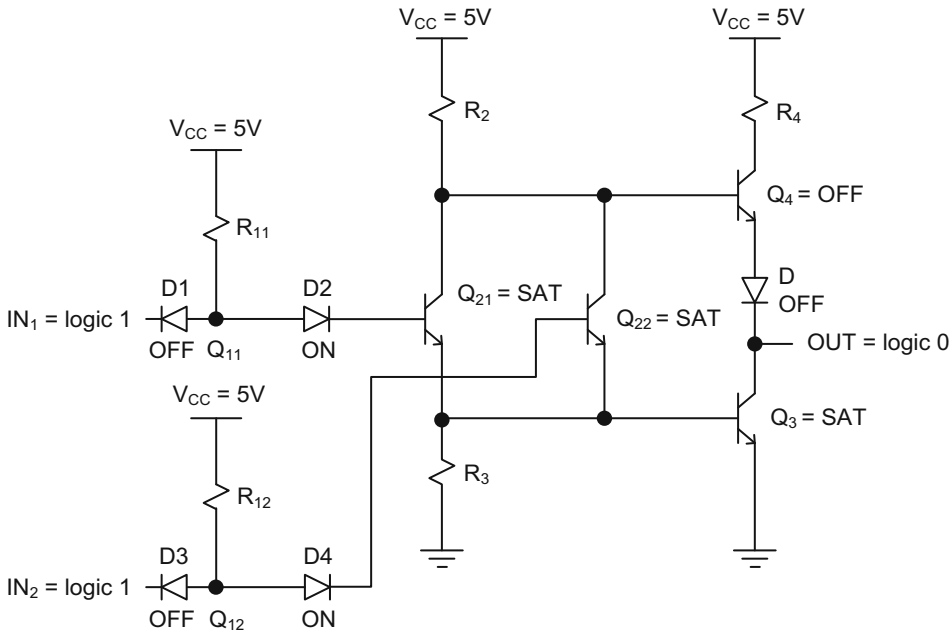


Fig. 4.18 Two-input TTL NOR gate when $IN_1 = IN_2 =$ logic 1

4.5 Input Current and Voltage Measurements of a Logic Gate

It is imperative to know the typical values of input and output terminal currents and voltages of a logic gate in order to eliminate potential electrical problems when interconnecting the gate with other gates to implement a logic block. This especially applies to logic gates fabricated using different technologies, i.e. a TTL gate interfacing a CMOS gate or vice versa.

Figure 4.19 shows the schematic to measure the input terminal current, I_{IL}, and voltage, V_{IL}, when the input is lowered. The potentiometer connected at the input constantly adjusts the value of V_{IL} while the resistor, R_{PROT}, limits the magnitude of I_{IL}. According to this figure, the minimum and maximum values of V_{IL} become equal to R_{PROT} I_{IL} and $(R_{POT} + R_{PROT})$ I_{IL}, respectively where R_{POT} is the maximum potentiometer value.

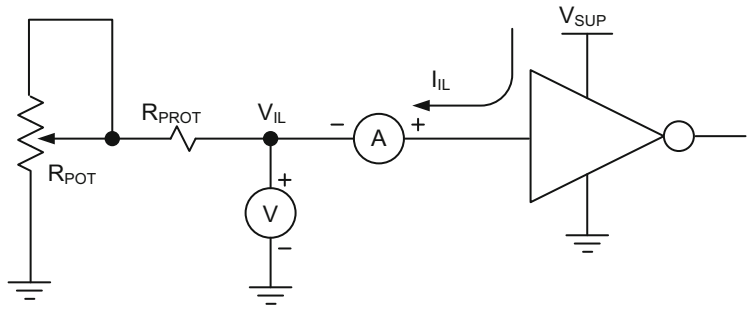


Fig. 4.19 Input current (I_{IL}) and voltage (V_{IL}) measurements when the input voltage is low

Figure 4.20 shows the setup to measure the input current, I_{IH}, and the voltage, V_{IH}, when the input voltage is high. The potentiometer constantly adjusts the value of V_{IH} while R_{PROT} limits the magnitude of I_{IH}. The minimum and maximum values of V_{IH} become equal to $V_{SUP} - (R_{POT} + R_{PROT})\ I_{IH}$ and $V_{SUP} - R_{PROT}\ I_{IH}$, respectively.

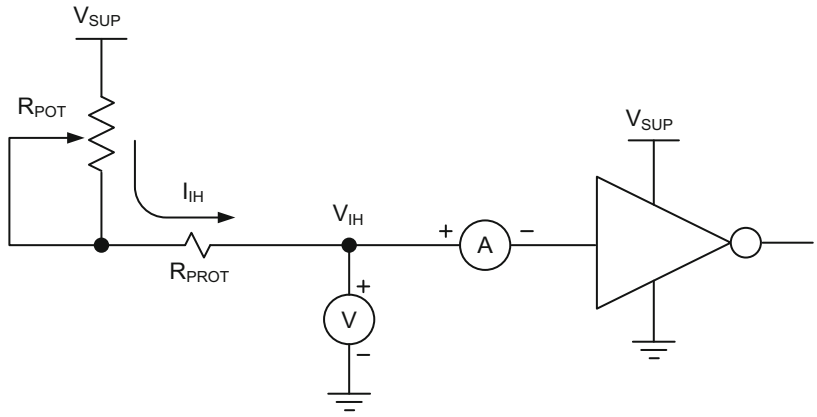


Fig. 4.20 Input current (I_{IH}) and voltage (V_{IH}) measurements when the input voltage is high

4.6 Output Current and Voltage Measurements of a Logic Gate

Current and voltage measurements can also be applied to the output terminals of a logic gate. Figure 4.21 shows the setup to measure the output current, I_{OL}, and the output voltage, V_{OL}, when the output is low. Here, R_{PROT} limits the amount of I_{OL} while the potentiometer adjusts the value of V_{OL}. According to this figure, the minimum and maximum V_{OL} can be calculated as $V_{SUP} - (R_{POT} + R_{PROT})\ I_{OL}$ and $V_{SUP} - R_{PROT}\ I_{OL}$, respectively.

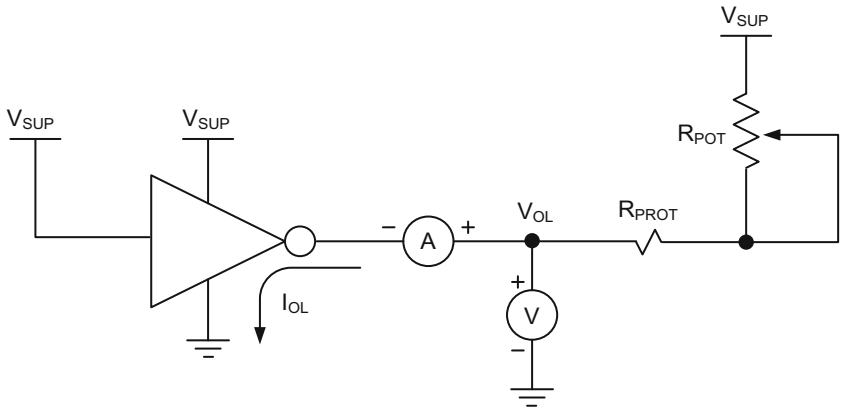


Fig. 4.21 Output current (I_{OL}) and voltage (V_{OL}) measurements when the output voltage is low

The setup in Fig. 4.22 is used if the output terminal current, I_{OH}, and the output terminal voltage, V_{OH}, need to be measured when the output is high. Here, R_{PROT} limits the amount of I_{OH} while the potentiometer constantly adjusts the value of V_{OH}. According to this figure, the minimum and maximum values of V_{OH} can be calculated as R_{PROT} I_{OH} and (R_{POT} + R_{PROT}) I_{OH}, respectively.

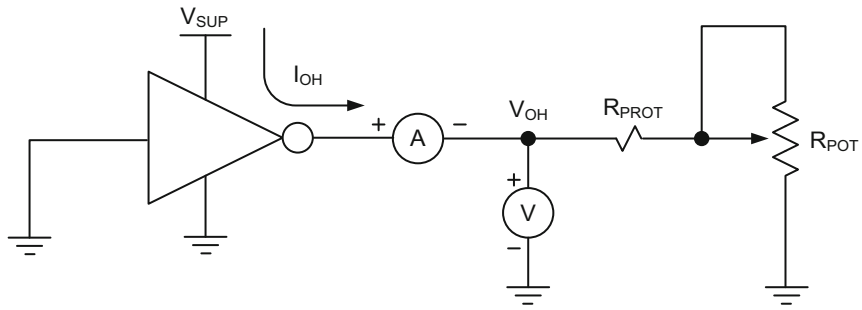


Fig. 4.22 Output current (I_{OH}) and voltage (V_{OH}) measurements when the output voltage is high

It is very possible to interface an old TTL logic gate with a state-of-the art CMOS logic gate. Logic level adjustment is a critical when interfacing tasks take place between two different logic families. This is mainly because power supply voltages used in each logic family may be different or each logic family may require different input and output logic levels. When interfacing becomes unavoidable, TTL and CMOS gates can be connected either using a passive device such as a resistor or an active device such as a bipolar transistor.

4.7 TTL-CMOS Interface with a Pull-up Resistor

When a TTL gate drives a CMOS gate, an external pull-up resistor, R_{PU}, must be added to the interface to be able to switch the CMOS gate.

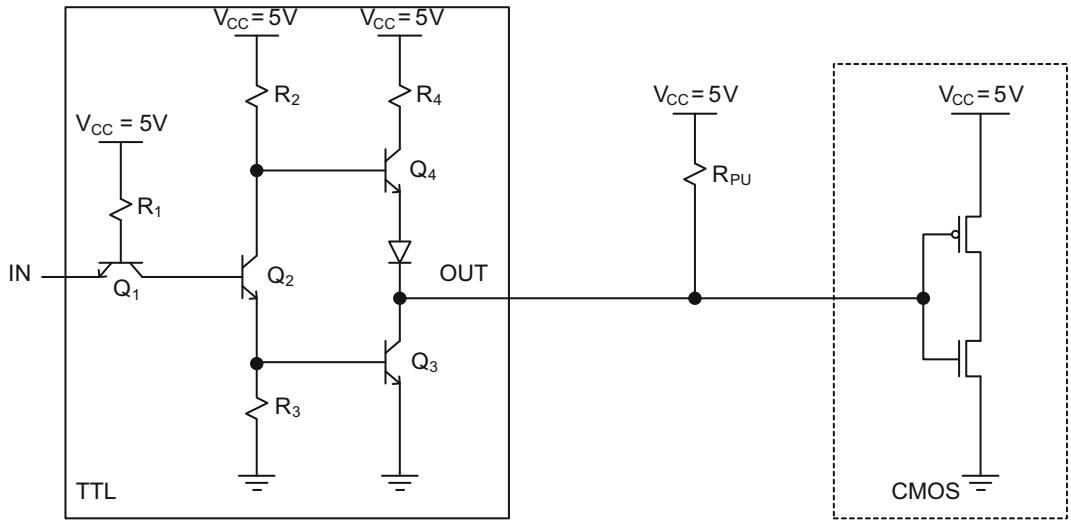


Fig. 4.23 A common TTL gate driving a CMOS gate with a pull-up resistor, R_{PU}

Figure 4.23 shows the interface where the TTL inverter input, IN, is at logic 1, and its output produces OUT = 0.2 V. TTL does not have any problem to switch the state of the CMOS inverter at this voltage level. The combination of a transient discharge current from the input of the CMOS inverter and a static current through the pull-up resistor, I_{PU}, determines the maximum sink current value, I_{OL}, of the TTL inverter as shown in Fig. 4.24. The I_{OL} of the TTL inverter is fetched from the manufacturer's datasheet to calculate R_{PU}. Neglecting I_{DIS}, I_{OL} becomes:

$$I_{OL} \approx I_{PU} = \frac{(5 - V_{OL})}{R_{PU}} = \frac{(5 - 0.2)}{R_{PU}} \tag{4.6}$$

Thus,

$$R_{PU} \approx \frac{4.8}{I_{OL}} \tag{4.7}$$

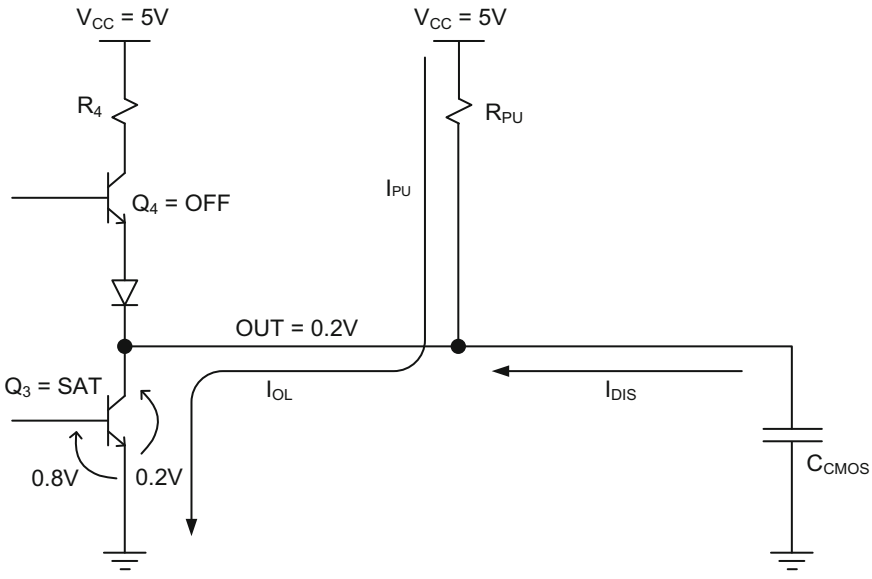


Fig. 4.24 A common TTL gate driving a CMOS gate with R_{PU} when TTL input is at logic 1

The CMOS switching becomes an issue when the TTL input is at logic 0 as shown in Fig. 4.25. In this case, the TTL output can produce a voltage in the neighborhood of 3.4–3.5 V. This voltage is more than enough to drive another common TTL gate. However, it may not be sufficient to drive a CMOS gate operating with a 5 V voltage supply. In general, CMOS gates require inputs well above their gate threshold voltage to be able to change the state of their output. Therefore, Q_4 will contribute delivering current to the input capacitance of the CMOS gate up until OUT reaches at 3.4 V. But, charging the input capacitance of the CMOS gate beyond 3.4 V is performed solely by the current through the pull-up resistor, I_{PU}, until the voltage across the capacitor eventually reaches 5 V.

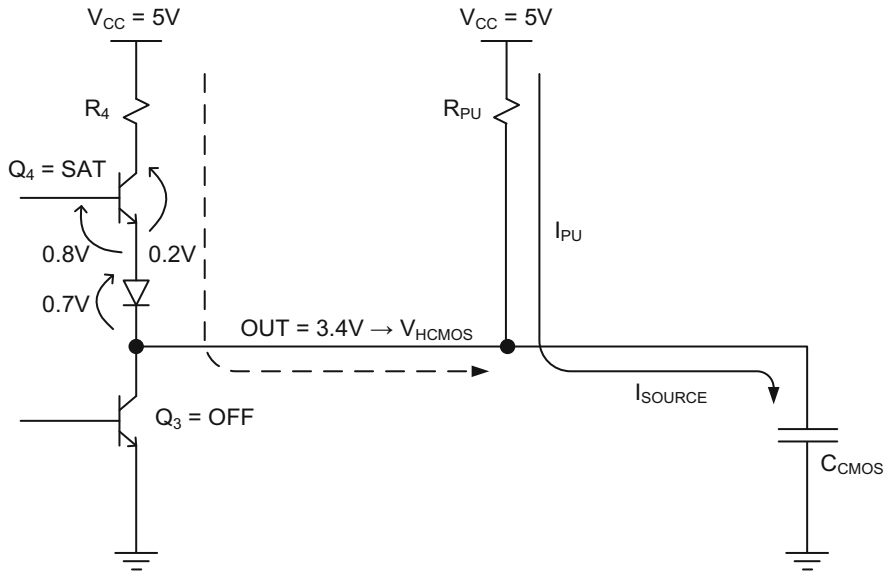


Fig. 4.25 A common TTL gate driving a CMOS gate with R_{PU} when TTL input is at logic 0

Example 4.3 Assume that a TTL inverter operates with V_{CC} = 5 V and needs to drive several CMOS inverters, all operating with V_{DD} = 5 V. Design a passive interface so the TTL inverter has the capability to drive multiple CMOS inverters.

The DC specifications for both parts are given in Fig. 4.26. According to this table, the TTL inverter cannot drive CMOS inverter(s) because the typical V_{OHTTL} = 3.4 V is less than the minimum value of V_{IHCMOS} = 4 V. Therefore, a pull-up resistor must be included between the gates as a passive interface. The low level voltages are compatible since V_{OLTTL} = 0.25 V is below the maximum V_{ILCMOS} = 1 V.

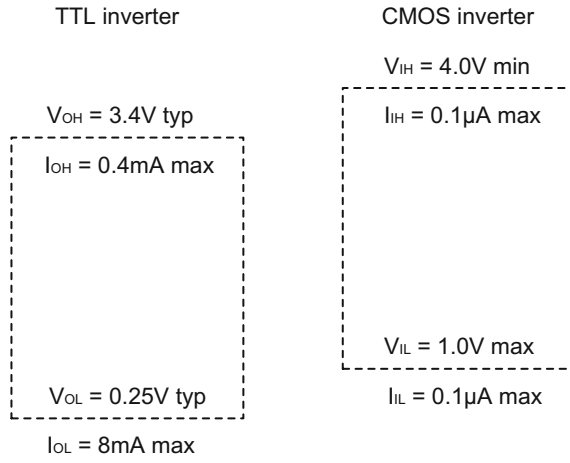


Fig. 4.26 DC parameter diagram for the TTL and CMOS inverters

When the output of the TTL inverter is at logic 0, one can calculate the minimum value of R_{PU} using Eq. 4.8.

$$R_{PU} = \frac{(5 - V_{OLTTL})}{I_{OLTTL}} = \frac{(5 - 0.25)}{8mA} = 593\,\Omega \tag{4.8}$$

R_{PU} can be increased as high as 1 KΩ. However, this produces a static current of I_{OLTTL} of 4.75 mA while the remaining current, 8 mA – 4.75 mA = 3.25 mA, is reserved to accommodate transient discharge currents from CMOS inverter input capacitor(s).

When the TTL inverter output switches to logic 1 (only about 3.4 V), the additional current to charge input capacitance of CMOS inverter(s) from 3.4 to 5 V will be through R_{PU}. This passive charge path creates a time constant of $\tau = R_{PU}\,C_{CMOS}$ where C_{CMOS} is the total input capacitance of CMOS inverter(s). Using smaller R_{PU} values decreases this transient period at the expense of more power consumption.

Another important consideration in the interface design is the output current capability of the TTL inverter. One can compute both the high and low fan-out values, N_H and N_L, as follows:

$$N_H = I_{OHTTL}/I_{IHCMOS} = 0.4\,mA/0.1\,\mu A = 4000$$

and

$$N_L = I_{OLTTL}/I_{ILCMOS} = 8\,mA/0.1\,\mu A = 80{,}000$$

According to this calculation, the TTL inverter can support up to 4000 CMOS inverters at its output.

4.8 TTL-CMOS Interface with a Bipolar Transistor

When a TTL gate drives a CMOS gate, an external active device, such as an NPN bipolar transistor shown in Fig. 4.27, can be used to adjust the required input voltage levels for the CMOS gate. However, using an active device, such as an NPN transistor in the interface, also introduces an extra layer of inversion between the TTL and the CMOS gates, requiring design modifications in the original design for correct logic functionality.

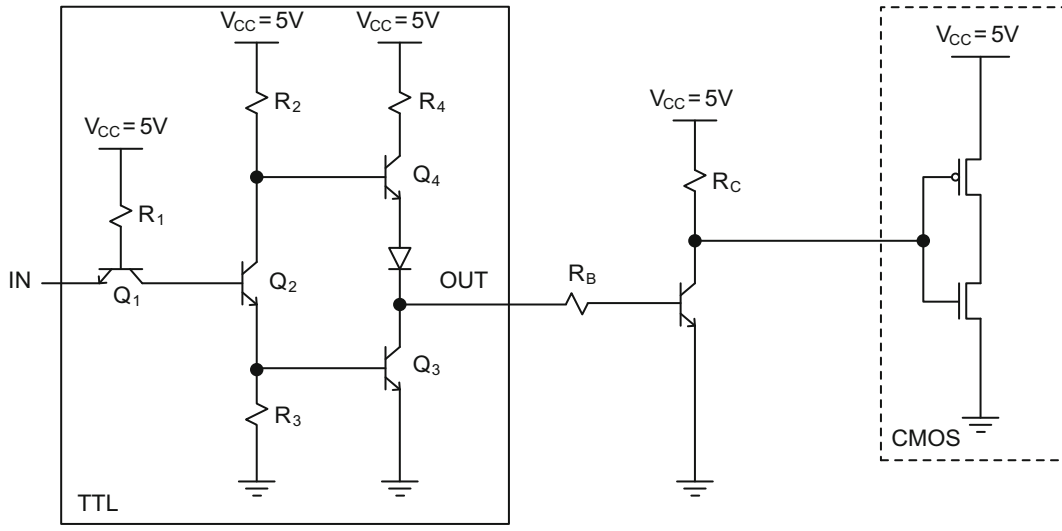


Fig. 4.27 A common TTL gate driving a CMOS gate with an NPN bipolar transistor

When IN = 5 V is applied to the TTL input, OUT becomes 0.2 V, which turns off the NPN transistor at the TTL-CMOS interface. The supply current, I_{CHAR}, through R_C charges the input capacitor of the CMOS gate to 5 V as shown in Fig. 4.28.

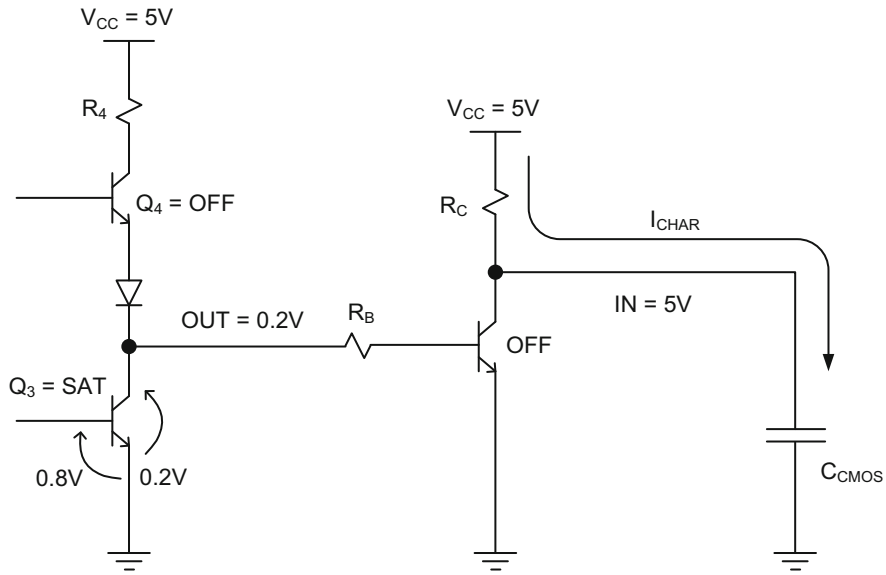


Fig. 4.28 A TTL gate driving a CMOS gate with an NPN when TTL input is at logic 1

Figure 4.29 examines the case when IN = 0 V at the TTL inverter's input. The TTL output becomes about 3.4 V, which is more than enough to saturate the NPN transistor at the interface.

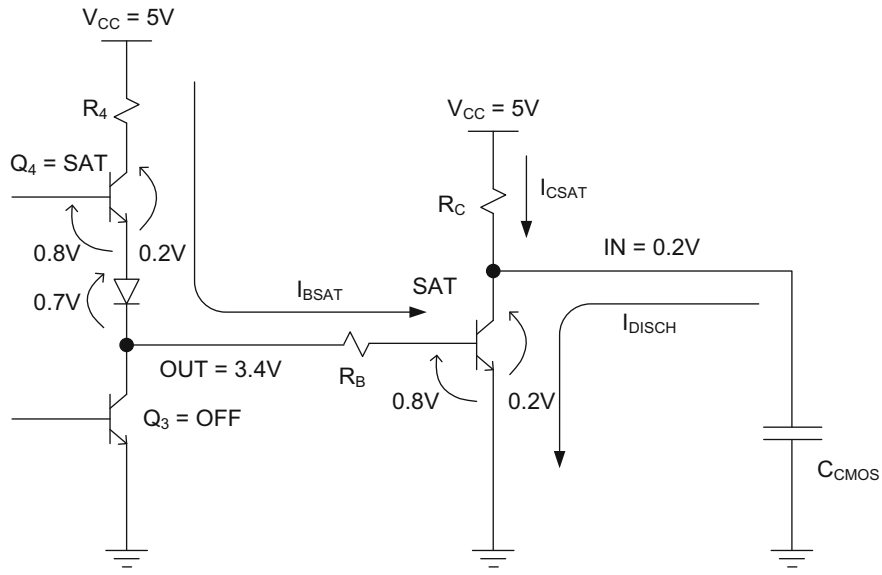


Fig. 4.29 A TTL gate driving a CMOS gate with an NPN when TTL input is at logic 0

Therefore, we have:

$$I_{BSAT} = I_{OH} = \frac{(OUT - 0.8)}{R_B} \tag{4.9}$$

or,

$$R_B = \frac{(OUT - 0.8)}{I_{OH}} \tag{4.10}$$

Replacing OUT with V_{OH} yields the value for R_B. Thus,

$$R_B = \frac{(V_{OH} - 0.8)}{I_{OH}} \tag{4.11}$$

Also,

$$I_{CSAT} = \frac{(V_{CC} - 0.2)}{R_C} = \frac{(5 - 0.2)}{R_C} = \frac{4.8}{R_C} \tag{4.12}$$

or

$$R_C = \frac{4.8}{I_{CSAT}} \tag{4.13}$$

In order to find I_{CSAT} in Eq. 4.13, we need to locate the I_B-curve that corresponds to $I_{OH} = I_{BSAT}$ in the I-V characteristics in Fig. 4.30 as the step no. 1.

However, we know that

$$I_{BACT} \approx \frac{I_{BSAT}}{10} \tag{4.14}$$

Therefore, in step no. 2 we locate the I_B-curve that corresponds to I_{BACT} in Fig. 4.30. In step no. 3, we draw a load line that intersects the I_{BACT}-curve at $V_{CE} = V_{CEMAX}/2$. This intersection is the quiescent point, Q_{ACT}, for the transistor operating in the middle of active region, and produces I_{CACT}. In step no. 4, we rotate the active-region load line counter-clockwise around V_{CEMAX} until the new load line intersects the I_{BSAT}-curve at I_{CACT}. The new quiescent point, Q_{SAT}, switches transistor operation from active region to saturation region. The value of I_{CSAT} can now be used in Eq. 4.13.

Note that the multiplier, 10, used to define the ratio between I_{BSAT} and I_{BACT} in Eq. 4.14 is a conservative number and creates high static power consumption when the NPN transistor is on at the interface. Multipliers in the order of 2 or 3 can be more realistic to achieve lower the power consumption.

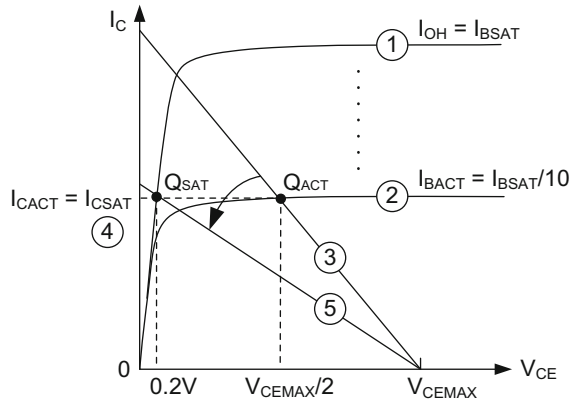


Fig. 4.30 Load line rotation of the bipolar circuit at the interface

Example 4.4 Assume that a high-voltage TTL device operating with a power supply voltage of $V_{CC} = 30$ V needs to drive a CMOS gate(s) with a supply voltage of $V_{DD} = 3$ V as shown in Fig. 4.31.

The nominal high and low output logic levels of the TTL device are $V_{OH} = 20$ V and $V_{OL} = 0$ V, respectively. The TTL device can generate up to $I_{OH} = 100$ mA source and $I_{OL} = 100$ mA sink currents for an external load. The CMOS gate, on the other hand, needs to have a minimum $V_{IH} = 2$ V and a maximum of V_{IL} of 1 V to operate. However, the nominal CMOS input voltage levels are $V_{IH} = 3$ V and $V_{IL} = 0$ V at which the CMOS gate draws approximately $I_{IH} = I_{IL} = 1$ μA as shown in this figure.

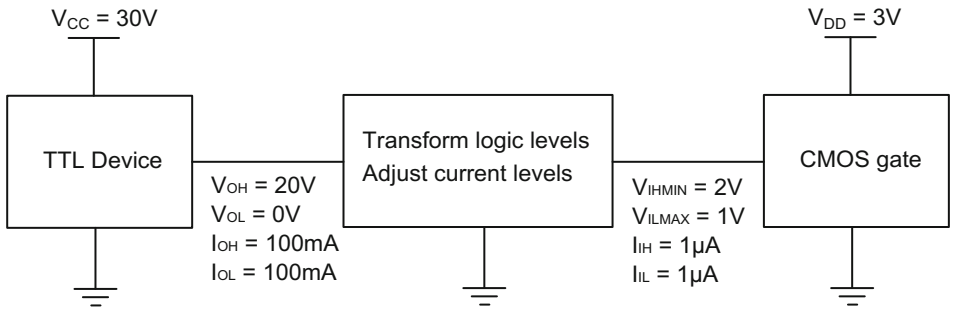


Fig. 4.31 Block diagram of a high voltage TTL device driving CMOS gate(s)

How can one design an interface between the TTL device and the CMOS gate using (a) a passive network and (b) an active NPN bipolar transistor that can transform the voltage levels?

The first task is to use passive elements, such as resistors, at the interface. When the TTL device produces $V_{OH} = 20$ V, the CMOS gate can only accommodate a maximum of $V_{IH} = 3$ V. If we use a passive pull-up resistor at the interface for logic translation, the TTL high output voltage appears directly at the input of the CMOS gate and burn the device. Therefore, the only other choice is to use a step-down resistor network composed of R_1 and R_2 as shown in Fig. 4.32.

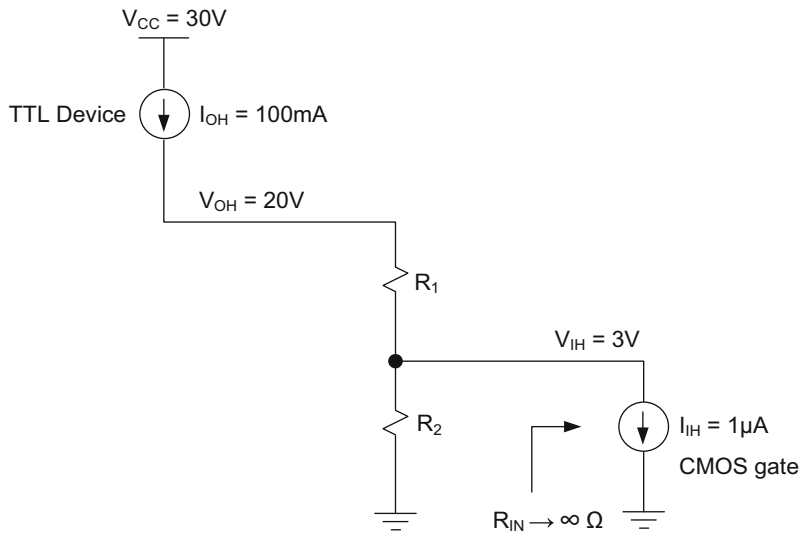


Fig. 4.32 Passive interface design when TTL device produces high output

Therefore,

$V_{OH} = (R_1 + R_2)\ I_{OH}$ since the input impedance of the CMOS gate approaches infinity. Substituting the values of V_{OH} and I_{OH} yields:

$$20\,\text{V} = (\text{R}_1 + \text{R}_2)100\,\text{mA}$$

or

$$\text{R}_1 + \text{R}_2 = 200\,\Omega \tag{4.15}$$

However,

$$\text{V}_{\text{IH}} = \text{R}_2\text{I}_{\text{OH}} = 3\,\text{V} \tag{4.16}$$

or

$$\text{R}_2 = 30\,\Omega \tag{4.17}$$

Thus,

$$\text{R}_1 = 200{-}30 = 170\,\Omega \tag{4.18}$$

Figure 4.33 shows the opposite case when the TTL output becomes V_{OL} = 0 V, and sinks 100 mA current emanating from the interface. However, this case does not provide additional information in calculating anything else but identifying the transient properties of the interface composed of I_{OL} and the total input capacitance of CMOS gate(s), leading to the calculation of TTL-fanout.

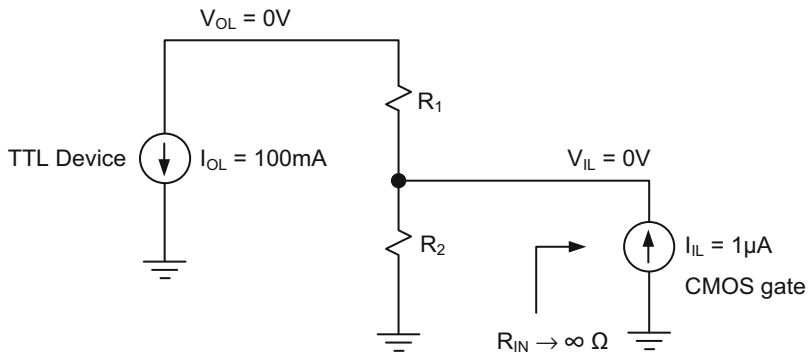


Fig. 4.33 Passive interface design when TTL device produces low output

The result of using resistive network creates a static power consumption of I_{OH} V_{OH} = 2 W, which is quite high to be able to use resistors.

The next design suggests using a NPN bipolar transistor at the interface to adjust the current and voltage levels. However, the inclusion of this device also inverts the TTL output and requires redesigning the logic functionality.

When TTL output produces V_{OH} = 20 V and I_{OH} = 100 mA as shown in the equivalent circuit in Fig. 4.34, the bipolar transistor at the interface goes into saturation. I_{BSAT} becomes equal to I_{OH}.

Thus,

$$V_{OH} = R_B I_{BSAT} + V_{BESAT} = R_B I_{OH} + V_{BESAT} \tag{4.19}$$

$20 - 0.8 = R_B\ 100\ \text{mA}$

$$R_B = \frac{19.2}{100\,\text{mA}} = 192\,\Omega \tag{4.20}$$

Similarly,

$$V_{SUP} = R_C I_A + V_{CESAT} \tag{4.21}$$

$$I_A \approx I_{CSAT} = \frac{(3 - 0.2)}{R_C} = \frac{2.8}{R_C} \tag{4.22}$$

However, to keep the bipolar transistor in saturation one needs:

$$I_{BSAT} \gg I_{BACT} \tag{4.23}$$

A conservative approach is to make I_{BSAT} 10 times higher than I_{BACT}. However, the use of smaller multipliers, such as 2 or 3, is possible depending on the transistor output I-V characteristics as discussed earlier. Thus,

$$I_{BSAT} \approx 10 I_{BCAT} = 10 \frac{I_{CACT}}{\beta} \tag{4.24}$$

Substituting the values for $I_{BSAT} = 100$ mA, and $I_{CACT} \approx I_{CSAT}$, and Eq. 4.22 into Eq. 4.24 yields:

$$100\,\text{mA} \approx \frac{10}{\beta}\left(\frac{2.8}{R_C}\right) \tag{4.25}$$

For $\beta = 100$

$$R_C = \frac{10}{100}\left(\frac{2.8}{100\,\text{mA}}\right) = 2.8\,\Omega \tag{4.26}$$

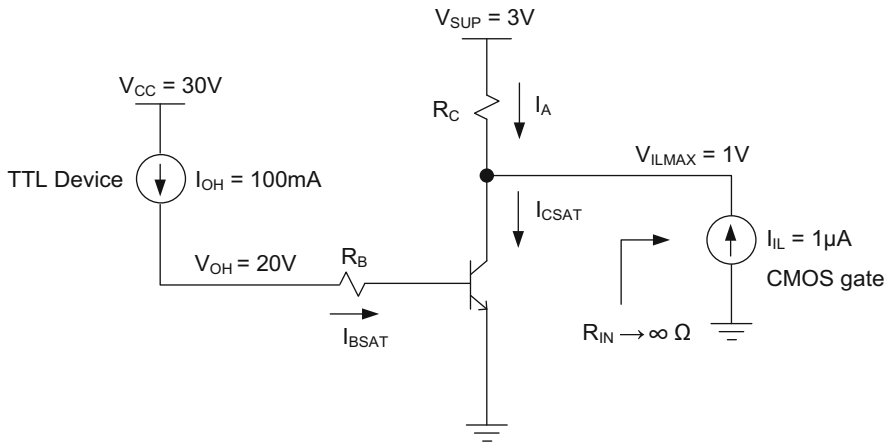


Fig. 4.34 Active interface design when TTL device produces high output

Figure 4.35 illustrates the case where the TTL device output produces V_{OL} = 0 V and I_{OL} = 100 mA, which turns off the bipolar transistor. No further design data can be obtained from this case.

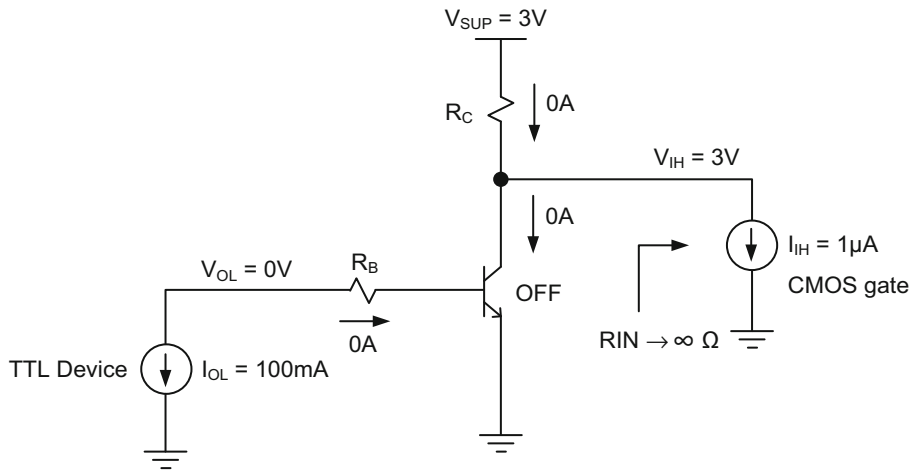


Fig. 4.35 Active interface design when TTL device produces low output

4.9 CMOS-TTL Interface with a Pull-Down Resistor

When a CMOS gate drives a TTL gate, the high logic output of the CMOS gate does not create an issue for the input circuitry of the TTL gate. The problem arises only when the output of the CMOS gate needs to lower the input of the TTL gate towards logic 0, and in

the process, it needs to drain a large input current from the TTL gate. An external pull-down resistor, R_{PD}, helps sinking the large TTL input current and eventually causes the TTL gate to switch its state as shown in Fig. 4.36.

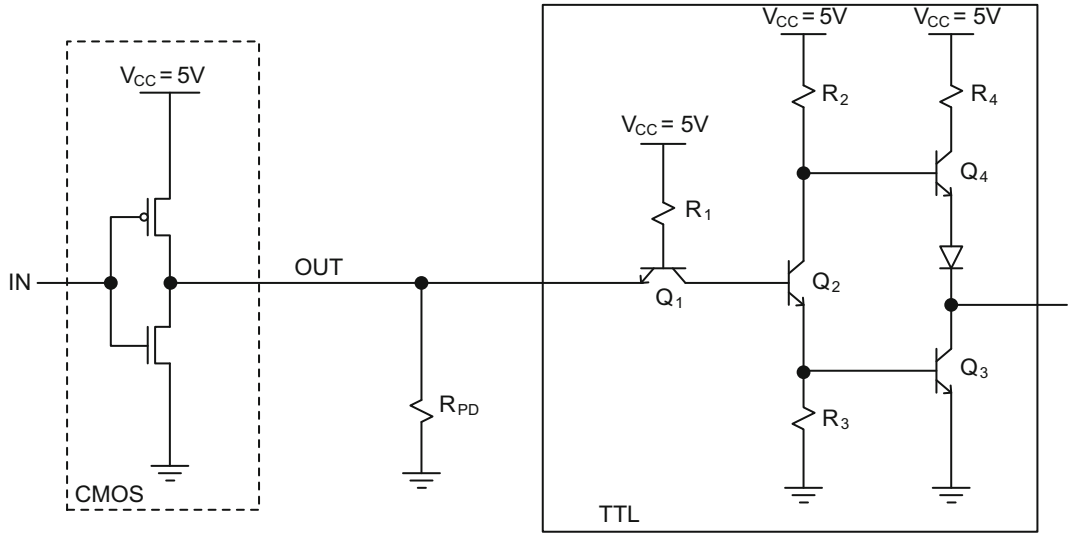


Fig. 4.36 CMOS inverter driving a TTL gate with a passive pull-down resistor

When the CMOS input voltage is 5 V, the NMOS transistor turns on with an equivalent resistance of R_N as shown in Fig. 4.37. The diode corresponding to the emitter-base junction of Q_1 turns on. In case the output current sinking capability of the CMOS gate is much smaller than the input current generated by the TTL gate, the pull-down resistor, R_{PD}, creates an extra drainage channel for the TTL input current as shown in Fig. 4.37. R_{PD} is determined as follows:

$$R_{PD} = \frac{V_{ILTTL}}{(I_{ILTTL} - I_{OLCMOS})} \tag{4.27}$$

Here, V_{ILTTL} and I_{ILTTL} are the low input voltage and the low input current of the TTL gate, respectively. I_{OLCMOS} is the low output current of the CMOS gate.

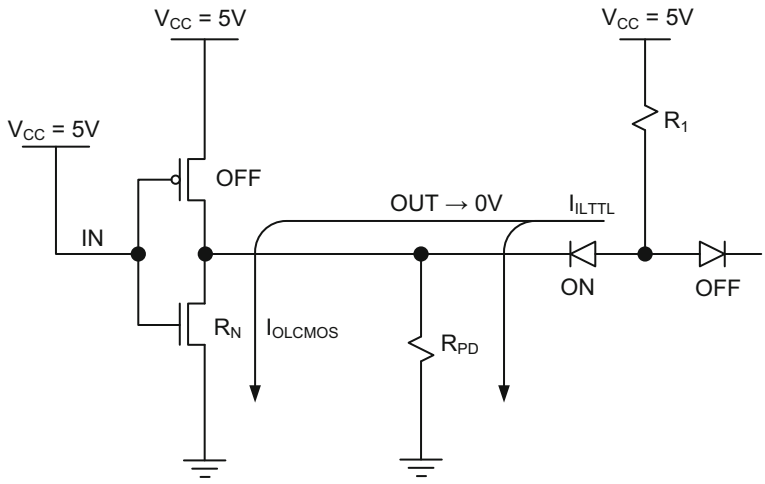


Fig. 4.37 CMOS inverter driving a TTL gate with R_{PD} when CMOS input is at 5 V

When the CMOS input voltage is 0 V, the PMOS transistor of the CMOS gate turns on and exhibits an equivalent resistance, R_P, as shown in Fig. 4.38. Since the diode corresponding to the emitter-base junction of Q_1 turns off, the output voltage becomes:

$$\text{OUT} = \frac{R_{PD}}{R_P + R_{PD}} V_{CC} \tag{4.28}$$

OUT approaches to V_{CC} = 5 V as long as $R_{PD} \gg R_P$.

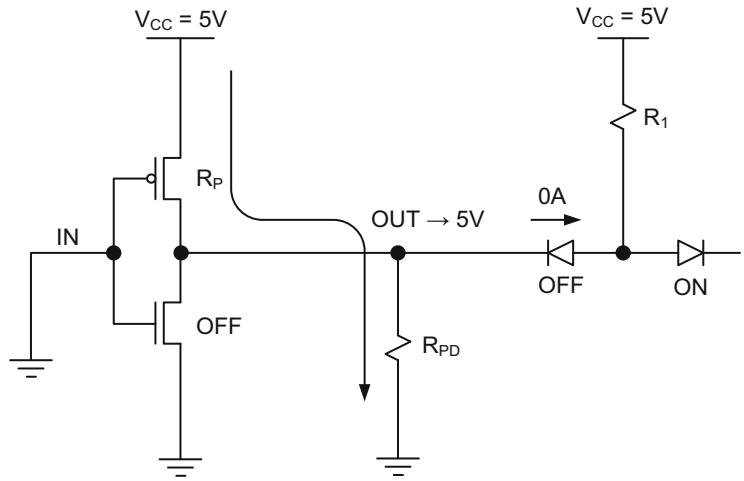


Fig. 4.38 CMOS inverter driving a TTL gate with R_{PD} when CMOS input is at 0 V

4.10 CMOS-TTL Interface with a Bipolar Transistor

When a CMOS gate drives a TTL gate, especially with a different supply voltage, it may be prudent to use an NPN transistor at the interface in order to translate the output voltage levels of the CMOS gate for the input voltage levels of the TTL gate as shown in Fig. 4.39. However, the bipolar circuit also creates a logic inversion as indicated previously.

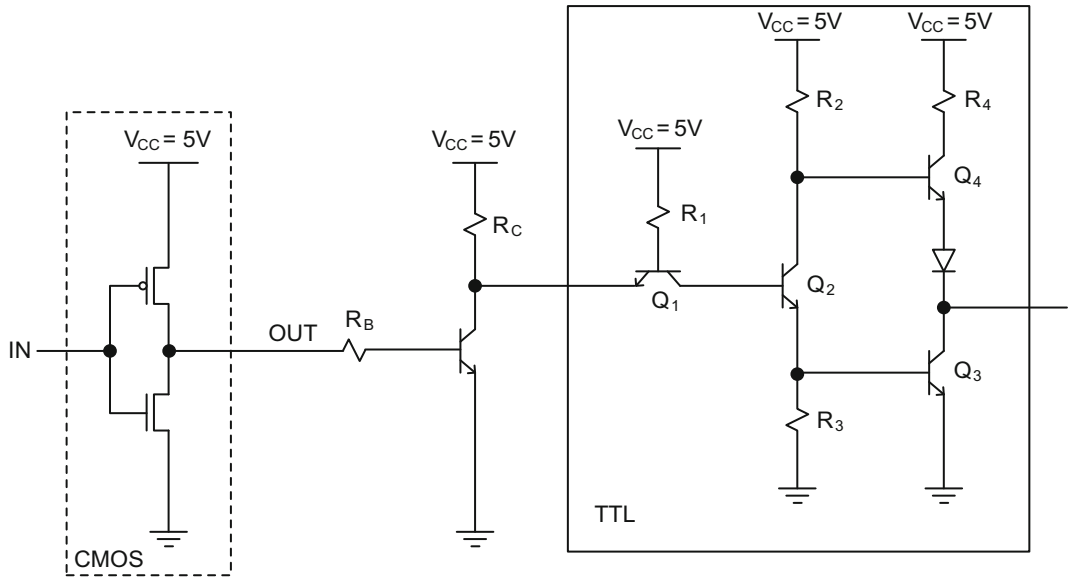


Fig. 4.39 CMOS inverter driving a TTL gate with an NPN bipolar transistor

Figure 4.40 shows when IN = 0 V is applied to the input of the CMOS inverter. Since the output of the CMOS inverter reaches 5 V, the NPN transistor at the interface saturates. Therefore, one must satisfy $I_{BSAT} \gg I_{BACT}$ for this transistor to enter into the saturation region.

Using a conservative multiplication factor of 10, $I_{BSAT} \approx 10 I_{BACT}$.

Thus,

$$I_{BSAT} \approx 10 \frac{I_{CACT}}{\beta} \tag{4.29}$$

However,

$$I_{BSAT} = I_{OHCMOS} \tag{4.30}$$

and

$$I_{CSAT} = I_A + I_{ILTTL} = \frac{(V_{CC} - V_{ILTTL})}{R_C} + I_{ILTTL} \approx I_{CACT} \tag{4.31}$$

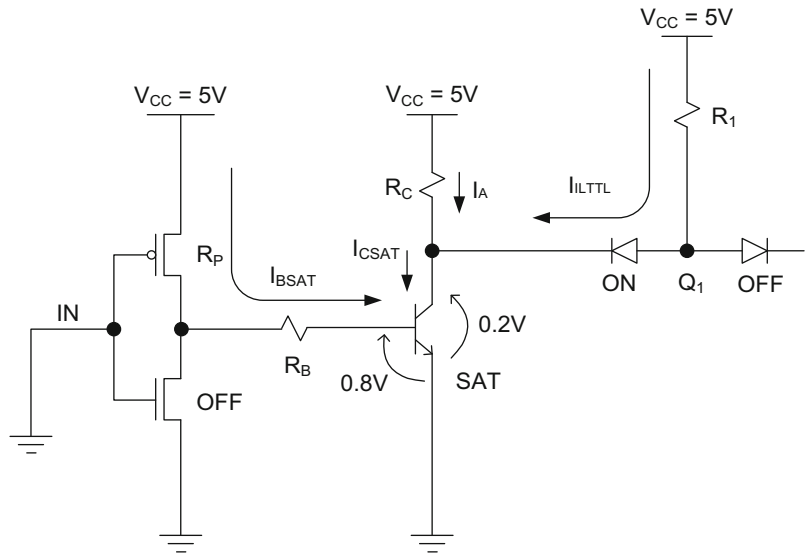


Fig. 4.40 CMOS inverter driving a TTL gate with a bipolar transistor when IN = 0 V

Here, I_{OHCMOS} is the high output current of the CMOS gate, and V_{ILTTL} and I_{ILTTL} are the low input voltage and input current of the TTL gate, respectively.

Substituting the values of I_{BSAT} in Eq. 4.30 and $I_{CSAT} \approx I_{CACT}$ in Eq. 4.31 in Eq. 4.29 yields:

$$I_{OHCMOS} = \frac{10}{\beta}\left(\frac{V_{CC} - V_{ILTTL} + R_C I_{ILTTL}}{R_C}\right) \tag{4.32}$$

Reorganizing the terms in Eq. 4.32 yields:

$$R_C = \frac{10(V_{CC} - V_{ILTTL})}{(\beta I_{OHCMOS} - 10 I_{ILTTL})} \tag{4.33}$$

R_B is selected as follows:

$$V_{OHCMOS} = R_B I_{BSAT} + 0.8 = R_B I_{OHCMOS} + 0.8 \tag{4.34}$$

Here, V_{OHCMOS} is the high output voltage of the CMOS gate. Then,

$$R_B = \frac{(V_{OHCMOS} - 0.8)}{I_{OHCMOS}} \tag{4.35}$$

When IN = 5 V, the output voltage of the CMOS gate becomes equal to V_{OLCMOS} as shown in Fig. 4.41. However, this voltage is not sufficient to turn on the interfacial bipolar transistor. Therefore, the NPN transistor's collector reaches 5 V and turns off the diode corresponding to the emitter-base junction of Q_1 in the TTL gate.

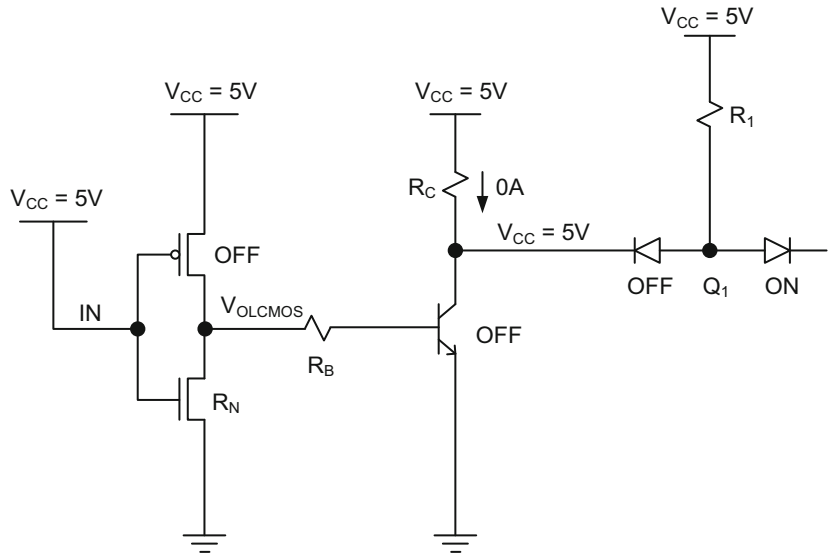


Fig. 4.41 CMOS inverter driving a TTL gate with a bipolar transistor when IN = 5 V

Review Questions

1. Determine R_1, R_2, R_3 and R_4 resistors in a TTL inverter with the following I/O characteristics. Use $\beta = 100$ for all four NPN transistors. Assume $V_{CC} = 5$ V.

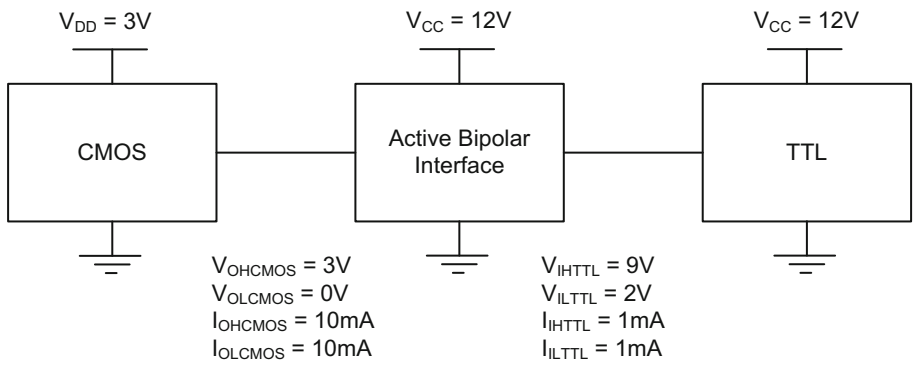
$V_{IL} = 0.2\,V \quad V_{OL} = 0.2\,V$
$V_{IH} = 3.5\,V \quad V_{OH} = 3.5\,V$
$I_{IL} = 1\,mA \quad I_{OL} = 10\,mA$
$I_{IH} = 0\,mA \quad I_{OH} = 10\,mA$

2. Determine R_1, R_2 and R_3 resistors in an open collector TTL inverter with the following I/O characteristics. Use $\beta = 100$ for all four NPN transistors. Assume $V_{CC} = 20$ V.

$V_{IL} = 0.2\,V \quad V_{OL} = 0.2\,V$
$V_{IH} = 20\,V \quad V_{OH} = 20\,V$
$I_{IL} = 1\,mA \quad I_{OL} = 10\,mA$
$I_{IH} = 0\,mA \quad I_{OH} = 0\,mA$

3. Implement out = A ⊕ B in a TTL logic gate using discrete gates. Try to implement the same logic function in an integrated form using a single gate.

4. A CMOS inverter with 3 V power supply needs to be interfaced with a TTL inverter with 12 V power supply as shown below. The interface is an active interface composed of an NPN transistor and resistors operating with 12 V power supply. The NPN bipolar transistor has a current gain of $\beta = 100$, and it goes into saturation if $I_{BSAT} \approx 10I_{BACT}$. The output current and voltage ratings of the CMOS inverter and input current and voltage ratings of the TTL inverter are shown below.
Find the resistor values connected to the base and the collector of the NPN transistor in this active interface. Apply both high (3 V) and low logic values (0 V) at the input of the CMOS gate, and check the voltage levels at the interface.



5. A bipolar circuit with an emitter resistance, R_E, below is used to feed two CMOS inputs. TTL_{OUT} port has the following characteristics:

$V_{OH} = 3.5\,V$
$V_{OL} = 0.2\,V$
$I_{OH} = 20\,mA$
$I_{OL} = 20\,mA$

Determine the resistors R_B, R_C and R_E. What are the current and voltage levels at $CMOS_{IN1}$ and $CMOS_{IN2}$ ports? According to your calculations, can $CMOS_{IN2}$ port be used to change the state of a CMOS gate?