18

Pulse-Width Modulated Rectifiers

To obtain low ac line current THD, the passive techniques described in the previous chapter rely on low-frequency transformers and/or reactive elements. The large size and weight of these elements are objectionable in many applications. This chapter covers active techniques that employ converters having switching frequencies much greater than the ac line frequency. The reactive elements and transformers of these converters are small, because their sizes depend on the converter switching frequency rather than the ac line frequency.

Instead of making do with conventional diode rectifier circuits, and dealing after-the-fact with the resulting low-frequency harmonics, let us consider now how to build a rectifier that behaves as ideally as possible, without generation of line current harmonics. In this chapter, the properties of the *ideal rectifier* are explored, and a model is described. The ideal rectifier presents an effective resistive load to the ac power line; hence, if the supplied ac voltage is sinusoidal, then the current drawn by the rectifier is also sinusoidal and is in phase with the voltage. Converters that approximate the properties of the ideal rectifier are sometimes called *power factor corrected*, because their input power factor is essentially unity [1].

The boost converter, as well as a variety of other converters, can be controlled such that a near-ideal rectifier system is obtained. This is accomplished by control of a high-frequency switching converter, such that the ac line current waveform follows the applied ac line voltage. Both single-phase and three-phase rectifiers can be constructed using PWM techniques. A typical dc power supply system that is powered by the single-phase ac utility contains three major power-processing elements. First, a high-frequency converter with a wide-bandwidth input-current controller functions as a near-ideal rectifier. Second, an energy-storage capacitor smooths the pulsating power at the rectifier output, and a low-bandwidth controller causes the average input power to follow the power drawn by the load. Finally, a dc–dc converter provides a well-regulated dc voltage to the load. In this chapter, single-phase rectifier systems are discussed, expressions for rms currents are derived, and various converter approaches are compared.

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The techniques developed in earlier chapters for modeling and analysis of dc-dc converters are extended in this chapter to treat the analysis, modeling, and control of low-harmonic rectifiers. The CCM models of Chapter 3 are used to compute the average losses and efficiency of CCM PWM converters operating as rectifiers. The results yield insight that is useful in power stage design. Several converter control schemes are known, including peak current programming, average current control, critical conduction mode control, and nonlinear carrier control. Ac modeling of the rectifier control system is also covered.

18.1 PROPERTIES OF THE IDEAL RECTIFIER

It is desired that the ideal single-phase rectifier present a resistive load to the ac system. The ac line current and voltage will then have the same waveshape and will be in phase. Unity power factor rectification is the result. Thus, the rectifier input current $i_{ac}(t)$ should be proportional to the applied input voltage $v_{ac}(t)$:

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e} \tag{18.1}$$

where R_e is the constant of proportionality. An equivalent circuit for the ac port of an ideal rectifier is therefore an effective resistance R_e, as shown in Fig. 18.1(a). R_e is also known as the *emulated resistance*. It should be noted that the presence of R_e does not imply the generation of heat: the power apparently

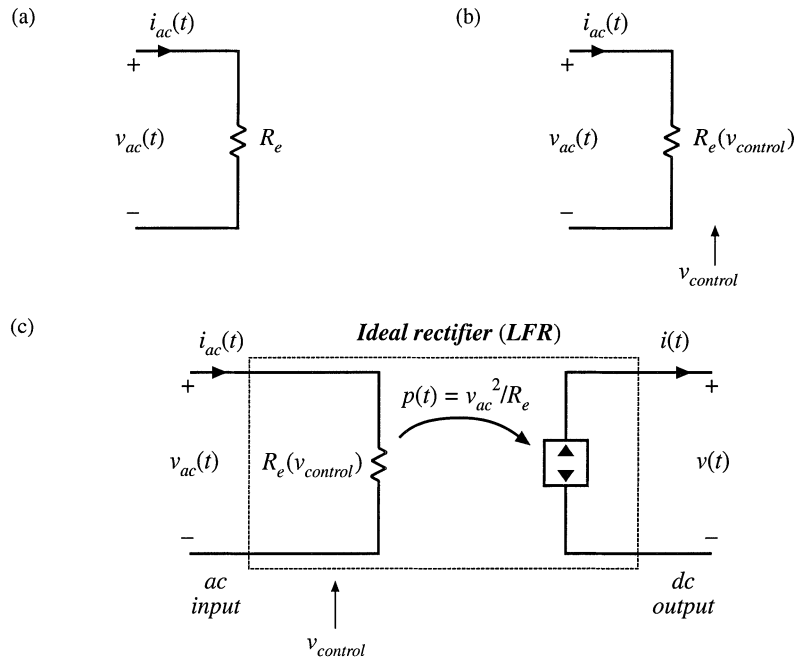

Fig. 18.1 Development of the ideal rectifier equivalent circuit model: (a) input port resistor emulation; (b) the value of the emulated resistance, and hence the power throughput, is controllable; (c) output port power source characteristic, and complete model.

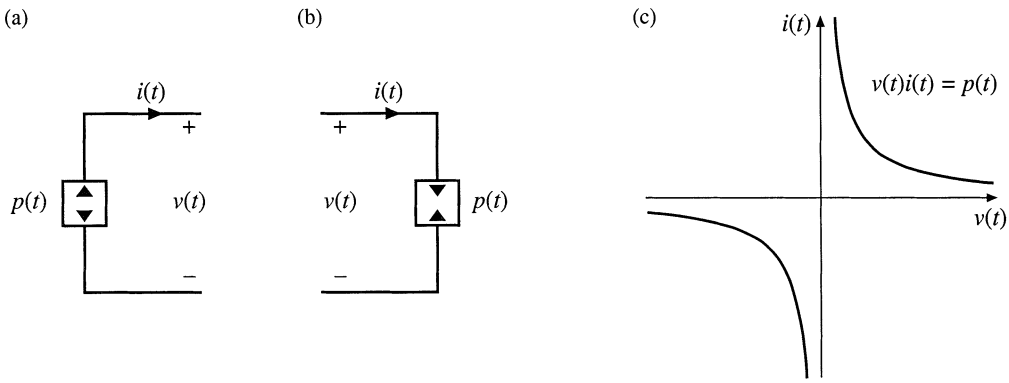

Fig. 18.2 The dependent power source: (a) power source schematic symbol, (b) power sink schematic symbol, (c) *i–v* characteristic.

"consumed" by R_e is actually transferred to the rectifier dc output port. R_e simply models how the ideal rectifier loads the ac power system.

Output regulation is accomplished by variation of the effective resistance R_e, and hence the value of R_e must depend on a control signal $v_{control}(t)$ as in Fig. 18.1(b). This allows variation of the rectifier power throughput, since the average power consumed by R_e is

$$P_{av} = \frac{V_{ac,rms}^2}{R_e(v_{control})} \tag{18.2}$$

Note that changing R_e results in a time-varying system, with generation of harmonics. To avoid generation of significant amounts of harmonics and degradation of the power factor, variations in R_e and in the control input must be slow with respect to the ac line frequency.

To the extent that the rectifier is lossless and contains negligible internal energy storage, the instantaneous power flowing into R_e must appear at the rectifier output port. Note that the instantaneous power throughput

$$p(t) = \frac{v_{ac}^2(t)}{R_e\big(v_{control}(t)\big)} \tag{18.3}$$

is dependent only on $v_{ac}(t)$ and the control input $v_{control}(t)$, and is independent of the characteristics of the load connected to the output port. Hence, the output port must behave as a source of constant power, obeying the relationship

$$v(t)i(t) = p(t) = \frac{v_{ac}^2(t)}{R_e} \tag{18.4}$$

The *dependent power source* symbol of Fig. 18.2(a) is used to denote such an output characteristic. As illustrated in Fig. 18.1(c), the output port is modeled by a power source that is dependent on the instantaneous power flowing into R_e.

Thus, a two-port model for the ideal unity-power-factor single-phase rectifier is as shown in Fig. 18.1(c) [2–4]. The two port model is also called a *loss-free resistor* (LFR) because (1) its input port obeys Ohm's law, and (2) power entering the input port is transferred directly to the output port without loss of

energy. The defining equations of the LFR are:

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e\left(v_{control}\right)} \tag{18.5}$$

$$v(t)i(t) = p(t) \tag{18.6}$$

$$p(t) = \frac{v_{ac}^2(t)}{R_e\left(v_{control}(t)\right)} \tag{18.7}$$

When the LFR output port is connected to a resistive load of value R, the dc output rms voltages and currents V_{rms} and I_{rms} are related to the ac input rms voltages and currents $V_{ac,rms}$ and $I_{ac,rms}$ as follows:

$$\frac{V_{rms}}{V_{ac,rms}} = \sqrt{\frac{R}{R_e}} \tag{18.8}$$

$$\frac{I_{ac,rms}}{I_{rms}} = \sqrt{\frac{R}{R_e}} \tag{18.9}$$

The properties of the power source and loss-free resistor network are discussed in Chapter 11. Regardless of the specific converter implementation, any single-phase rectifier having near-ideal properties can be modeled using the LFR two-port model.

18.2 REALIZATION OF A NEAR-IDEAL RECTIFIER

Feedback can be employed to cause a converter that exhibits controlled dc transformer characteristics to obey the LFR equations. In the single-phase case, the simplest and least expensive approach employs a full-wave diode rectifier network, cascaded by a dc–dc converter, as in Fig. 18.3. The dc–dc converter is represented by an ideal dc transformer, as discussed in Chapter 3. A control network varies the duty cycle, as necessary to cause the converter input current $i_g(t)$ to be proportional to the applied input volt-

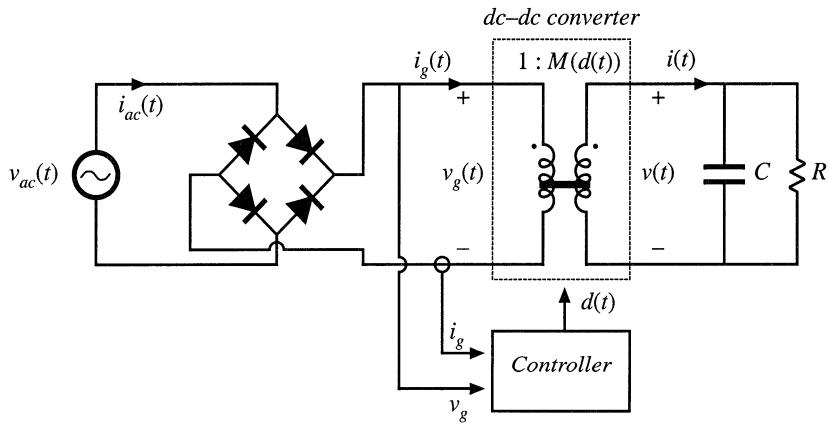

Fig. 18.3 Synthesis of an ideal rectifier by varying the duty cycle of a PWM dc–dc converter.

age $v_g(t)$ as in Eq. (18.1). The effective turns ratio of the ideal transformer then varies with time. Ideal waveforms are illustrated in Fig. 18.4. If the applied input voltage $v_{ac}(t)$ is sinusoidal,

$$v_{ac}(t) = V_M \sin(\omega t) \tag{18.10}$$

then the rectified voltage $v_g(t)$ is

$$v_g(t) = V_M \left|\sin(\omega t)\right| \tag{18.11}$$

It is desired that the converter output voltage be a constant dc value $v(t) = V$. The converter conversion ratio must therefore be

$$M\big(d(t)\big) = \frac{v(t)}{v_g(t)} = \frac{V}{V_M \left|\sin(\omega t)\right|} \tag{18.12}$$

This expression neglects the converter dynamics. As can be seen from Fig. 18.4, the controller must cause the conversion ratio to vary between infinity (at the ac line voltage zero crossings) and some minimum value M_{min} (at the peaks of the ac line voltage waveform). M_{min} is given by

$$M_{min} = \frac{V}{V_M} \tag{18.13}$$

Any converter topology whose ideal conversion ratio can be varied between these limits can be employed in this application.

To the extent that the dc–dc converter is ideal (i.e., if the losses can be neglected and there is negligible low-frequency energy storage), the instantaneous input and output powers are equal. Hence, the output current $i(t)$ in Fig. 18.3 is given by

$$i(t) = \frac{v_g(t) i_g(t)}{V} = \frac{v_g^2(t)}{V R_e} \tag{18.14}$$

Substitution of Eq. (18.11) into Eq. (18.14) then leads to

$$\begin{aligned} i(t) &= \frac{V_M^2}{V R_e} \sin^2(\omega t) \\ &= \frac{V_M^2}{2 V R_e} \big(1 - \cos(2\omega t)\big) \end{aligned} \tag{18.15}$$

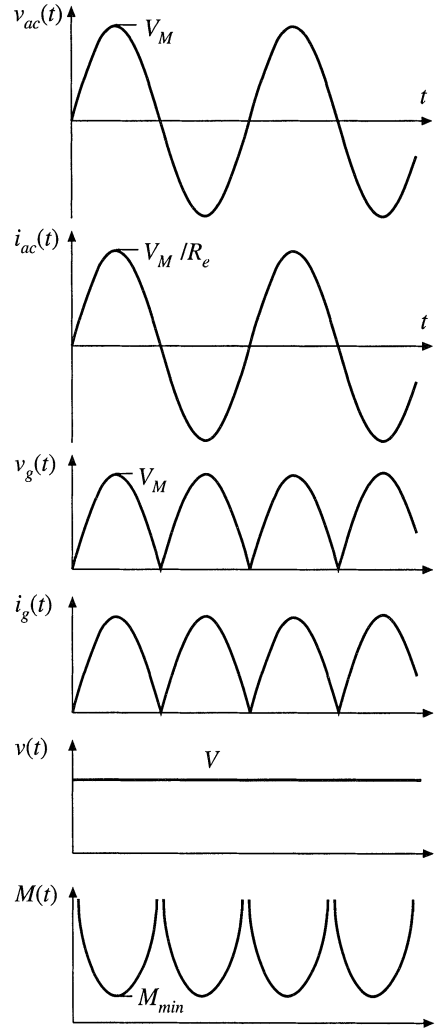

Fig. 18.4 Waveforms of the rectifier system of Fig. 18.3.

Hence, the converter output current contains a dc component and a component at the second harmonic of the ac line frequency. One of the functions of capacitor C in Fig. 18.3 is to filter out the second harmonic component of $i(t)$, so that the load current (flowing through resistor R) is essentially equal to the dc component

$$I = \langle i(t) \rangle_{T_L} = \frac{V_M^2}{2VR_e} \tag{18.16}$$

where T_L is the period of the applied ac line voltage.

The average power is

$$P = \frac{V_M^2}{2R_e} \tag{18.17}$$

The above equations are generally valid for PWM converters used as single-phase low-harmonic rectifiers.

18.2.1 CCM Boost Converter

A system based on the CCM boost converter is illustrated in Fig. 18.5 [1,5,6]. Ideally, the boost converter can produce any conversion ratio between one and infinity. Hence, the boost converter is capable of producing the $M(d(t))$ given by Eq. (18.12), provided that $V \geq V_M$. Further, the boost converter can produce very low THD, with better transistor utilization than other approaches.

If the boost converter operates in continuous conduction mode, and if the inductor is small enough that its influence on the low-frequency components of the converter waveforms is negligible, then the duty ratio should follow $M(d(t)) = 1/(1 - d(t))$. This implies that the duty ratio should follow the function

$$d(t) = 1 - \frac{v_g(t)}{V} \tag{18.18}$$

This expression is true only in the continuous conduction mode. The boost converter operates in the continuous conduction mode provided that the inductor current ripple

$$\Delta i_g(t) = \frac{v_g(t)d(t)T_s}{2L} \tag{18.19}$$

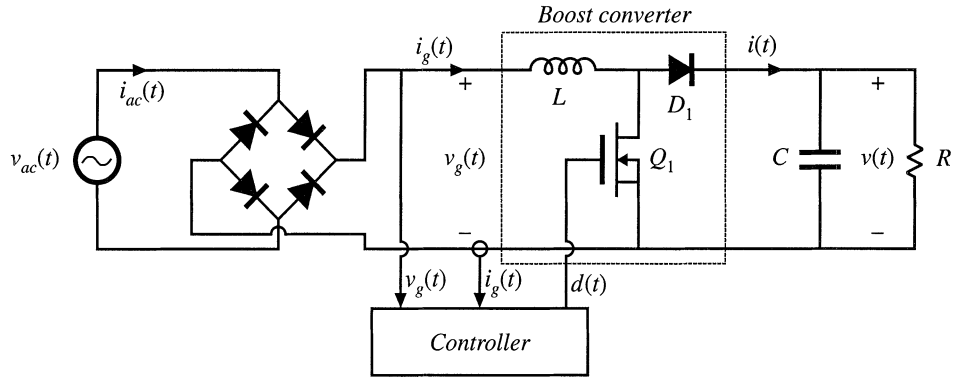

Fig. 18.5 Rectifier system based on the boost converter.

is greater than the average inductor current, or

$$\left\langle i_g(t)\right\rangle_{T_s} = \frac{v_g(t)}{R_e} \tag{18.20}$$

Hence, the converter operates in CCM when

$$\left\langle i_g(t)\right\rangle_{T_s} > \Delta i_g(t) \;\Rightarrow\; d(t) < \frac{2L}{R_e T_s} \tag{18.21}$$

Substitution of Eq. (18.18) into (18.21) and solution for R_e leads to

$$R_e < \frac{2L}{T_s\left(1 - \dfrac{v_g(t)}{V}\right)} \quad \text{for CCM} \tag{18.22}$$

Since $v_g(t)$ varies according to Eq. (18.11), Eq. (18.22) may be satisfied at some points on the ac line cycle, and not at others. Since $0 \le v_g(t) \le V_M$, we can conclude that the converter operates in CCM over the entire ac line cycle when

$$R_e < \frac{2L}{T_s} \tag{18.23}$$

Equations (18.18) and (18.22) then hold for all t. The converter always operates in DCM when

$$R_e > \frac{2L}{T_s\left(1 - \dfrac{V_M}{V}\right)} \tag{18.24}$$

For R_e between these limits, the converter operates in DCM when $v_g(t)$ is near zero, and in CCM when $v_g(t)$ approaches V_M.

The static input characteristics of the open-loop boost converter are sketched in Fig. 18.6. The input current $i_g(t)$ is plotted vs. input voltage $v_g(t)$, for various duty cycles $d(t)$. In CCM, the input characteristics of the boost converter are described by

$$\frac{v_g(t)}{V} = 1 - d(t) \qquad \text{in CCM} \tag{18.25}$$

To obtain a general plot, we can normalize the input current and input voltage as follows:

$$m_g(t) = \frac{v_g(t)}{V} \tag{18.26}$$

$$j_g(t) = \frac{2L}{VT_s} i_g(t) \tag{18.27}$$

Equation (18.25) then becomes

$$m_g(t) = 1 - d(t) \tag{18.28}$$

This equation is independent of the input current $i_g(t)$, and hence is represented by vertical lines in Fig.

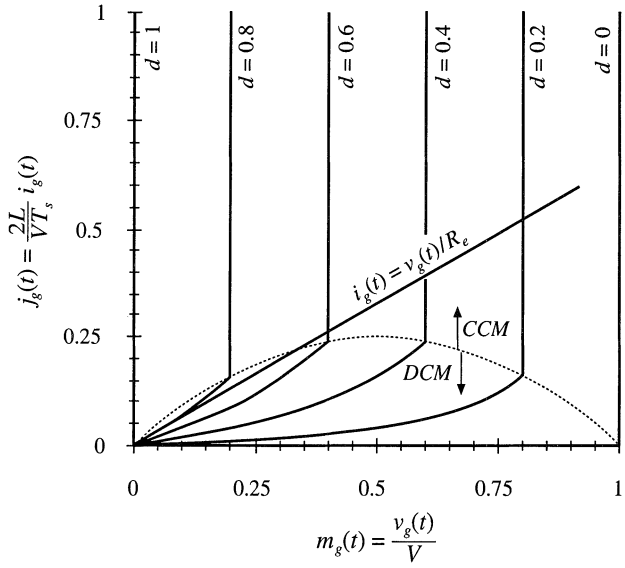

Fig. 18.6 Static input characteristics of the boost converter. A typical linear resistive input characteristic is superimposed.

18.6.

To derive the boost input characteristic for DCM operation, we can solve the steady-state equivalent circuit model of Fig. 11.12(b) (reproduced in Fig. 18.7). *Beware*: the natural DCM effective resistance of Chapter 11, $R_e = 2L/d^2T_s$, does not necessarily coincide with the emulated resistance $R_e = v_g/i_g$ of Eq. (18.1). In this chapter, the quantity R_e is defined according to Eq. (18.1). Solution of Fig. 18.7 for the input current $i_g(t)$ leads to:

$$i_g(t) = \frac{v_g(t)}{\left(\frac{2L}{d^2T_s}\right)} + \frac{p(t)}{V - v_g(t)} \tag{18.29}$$

The instantaneous power consumed by the effective resistor in the model of Fig. 18.7 is

$$p(t) = \frac{v_g^2(t)}{\left(\frac{2L}{d^2T_s}\right)} \tag{18.30}$$

Substitution of Eq. (18.30) into Eq. (18.29) and simplification leads to

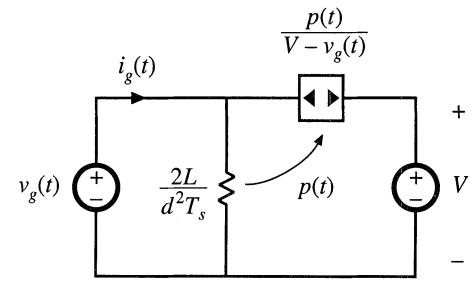

Fig. 18.7 Averaged equivalent circuit model of the boost converter operating in DCM, derived in Chapter 11.

$$\frac{2L}{VT_s} i_g(t) \left(1 - \frac{v_g(t)}{V}\right) = d^2(t) \frac{v_g(t)}{V} \qquad \text{in DCM} \qquad (18.31)$$

Normalization of this equation according to Eqs. (18.26) and (18.27) yields

$$j_g(t)\left(1 - m_g(t)\right) = d^2 m_g(t) \qquad (18.32)$$

This equation describes the curved (DCM) portions of the Fig. 18.6 input characteristics, for low $i_g(t)$.

To express the CCM/DCM mode boundary as a function of $v_g(t)$ and $i_g(t)$, Eqs. (18.1) and (18.22) can be combined, leading to

$$\frac{2L}{VT_s} i_g(t) > \left(\frac{v_g(t)}{V}\right)\left(1 - \frac{v_g(t)}{V}\right) \qquad \text{for CCM} \qquad (18.33)$$

Normalization of this equation, according to Eqs. (18.26) and (18.27), results in

$$j_g(t) > m_g(t)\left(1 - m_g(t)\right) \qquad \text{for CCM} \qquad (18.34)$$

This equation describes a parabola having roots at $m_g = 0$ and $m_g = 1$, with the maximum value $j_g = 0.25$ at $m_g = 0.5$. The mode boundary equation is plotted as a dashed line in Fig. 18.6

The complete input characteristics for the boost converter were plotted in Fig. 18.6 using Eqs. (18.28), (18.32), and (18.34). Figure 18.6 also illustrates the desired linear resistive input characteristic, Eq. (18.1). For the value of R_e illustrated, the converter operates in DCM for $v_g(t)$ near zero, and in CCM for $v_g(t)$ near V_M. The intersections of boost input characteristics with the desired linear input characteristic illustrate how the controller must choose the duty cycle at various values of $v_g(t)$.

Other converters capable of producing the $M(d(t))$ of Eq. (18.12) include the buck-boost, SEPIC, and Ćuk converters. The boost, SEPIC, and Ćuk converters share the desirable property of non-pulsating input current, and hence require minimal input EMI filtering. The SEPIC produces a non inverted output voltage. Isolated versions of these converters (see Chapter 6) are also sometimes employed [7–9]. Schemes involving the parallel resonant converter, as well as several types of quasi-resonant converters, are also documented in the literature [10–13].

The open-loop boost converter, when operated in discontinuous conduction mode, is also sometimes used as an approximation of an ideal rectifier. The DCM effective resistance $2L/d^2(t)T_s$ of Fig. 18.7 is then taken as an approximation of the desired emulated resistance of Eq. (18.1). The model differs from that of the ideal rectifier model of Fig. 18.1(c) in that the power source is connected between the input and output terminals. As a result, harmonics are present in the input current waveform. For example, if $v_g(t)$ is a rectified sinusoid, then the current through the effective resistance $2L/d^2(t)T_s$ will also be a rectified sinusoid. However, the input current $\langle i_g(t)\rangle_{T_s}$ is now equal to the sum of the current through R_e and the current flowing through the power source element. Since the power source is a nonlinear element, $\langle i_g(t)\rangle_{T_s}$ contains harmonics. For large C, the output voltage is essentially constant. The input current waveform is then given by Eq. (18.31). If V is sufficiently large, then the term $(1 - v_g(t)/V)$ is approximately equal to one, and the harmonics in $\langle i_g(t)\rangle_{T_s}$ are small. The zero crossings of $v_g(t)$, $p(t)$, and $\langle i_g(t)\rangle_{T_s}$ coincide. So although the DCM boost converter generates some current harmonics, it is nonetheless possible to construct a low harmonic rectifier that meets harmonic limits. Again, this approach has the disadvantages of the increased peak currents of DCM, and the need for additional filtering of the high-frequency pulsating input currents. Computer simulation of a DCM boost rectifier is described in Appendix B, Section B.2.3.

A similar approach is to operate the boost converter at the boundary between the continuous and discontinuous conduction modes. This approach is known as "critical conduction mode" operation. It eliminates the distortion mechanism described above, but requires variable switching-frequency control. This approach is quite popular at low power levels, and is described further in Section 18.3.3.

Other converters not capable of producing the $M(d(t))$ of Eq. (18.12), such as the buck converter, are sometimes employed as the dc–dc converter of Fig. 18.3. Distortion of the ac line current waveform must then occur. Nonetheless, at low power levels it may be possible to meet the applicable ac line current harmonic standards using such an approach.

18.2.2 DCM Flyback Converter

In Chapter 11, the loss-free resistor network is used to model converters operating in discontinuous conduction mode. This suggests that DCM converters can also be used as near-ideal rectifiers. Indeed, the buck-boost, flyback, SEPIC, and Ćuk converters, when operated in discontinuous conduction mode without additional control, inherently behave as natural loss-free resistors. The DCM effective resistance R_e, found in Chapter 11 to be equal to $2L/D^2T_s$, then coincides with the rectifier emulated resistance of Eq. (18.1). At low power levels, this can be an effective and low-cost approach. Inrush current limiting is also inherent in this approach, and isolation and scaling via a turns ratio are provided by the transformer. Disadvantages are the increased peak currents of DCM, and the need for additional filtering of the high-frequency pulsating input currents.

A simple low-harmonic rectifier system based on the transformer-isolated flyback converter is illustrated in Fig. 18.8 [2]. The ac line voltage is connected through an input EMI filter to a bridge rectifier and a flyback converter. The flyback converter is operated at constant switching frequency f_s and constant duty cycle D. The converter is designed such that it operates in the discontinuous conduction mode under all conditions. The input EMI filter smooths the pulsating input current waveform, so that $i_{ac}(t)$ is approximately sinusoidal.

The flyback converter is replaced by its averaged equivalent circuit in Fig. 18.9. As discussed in Chapter 11, the terminal waveforms of the flyback converter have been averaged over the switching period T_s, resulting in the loss-free resistor model. This model illustrates how the DCM flyback converter presents a resistive load to the ac input. It also illustrates how the power flow can be controlled, by varia-

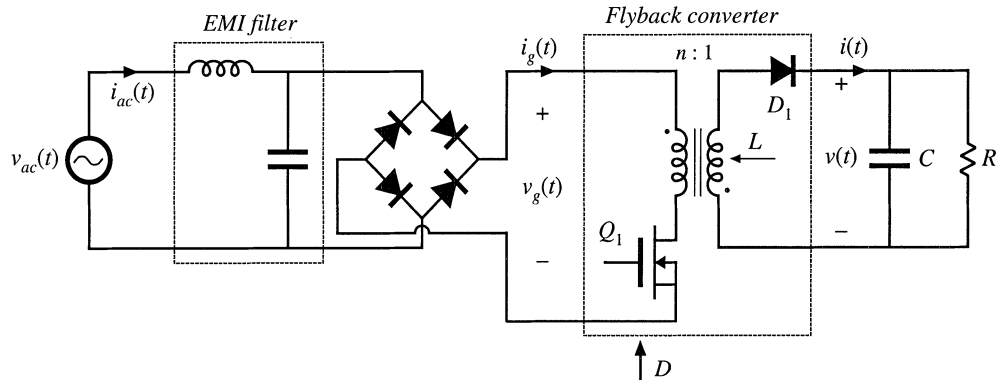

Fig. 18.8 Low-harmonic rectifier system incorporating a flyback converter that operates in the discontinuous conduction mode.

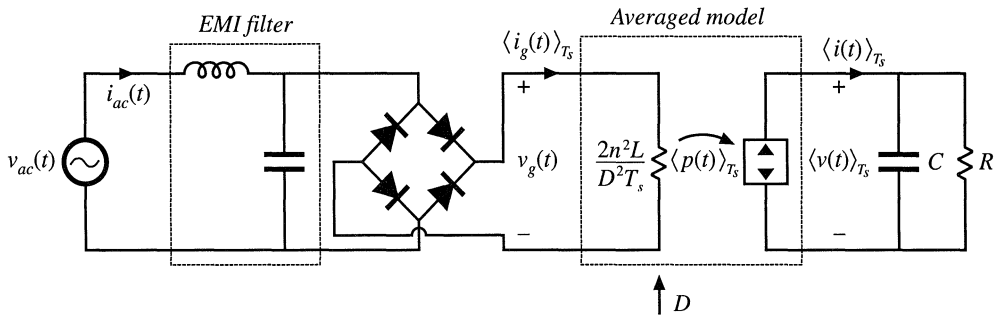

Fig. 18.9 Averaged equivalent circuit that models the system of Fig. 18.8.

tion of D to control the value of the emulated resistance R_e.

To design this converter, one must select the value of inductance to be sufficiently small, such that the converter operates in DCM at all points on the ac sine wave, at maximum load. If we denote the lengths of the transistor conduction interval, diode conduction interval, and discontinuous interval as DT_s, d_2T_s, and d_3T_s, respectively, then the converter operates in DCM provided that d_3 is greater than zero. This implies that

$$d_2(t) < 1 - D \tag{18.35}$$

By volt-second balance on the transformer magnetizing inductance, we can express $d_2(t)$ as

$$d_2(t) = D\frac{v_g(t)}{nV} \tag{18.36}$$

Substitution of Eq. (18.36) into Eq. (18.35) and solution for D yields

$$D < \frac{1}{\left(1 + \frac{v_g(t)}{nV}\right)} \tag{18.37}$$

During a given switching period, the converter will operate in DCM provided that the above inequality is satisfied. The worst case occurs when the rectified sinusoid $v_g(t)$ is equal to its peak value V_M. The inequality then becomes

$$D < \frac{1}{\left(1 + \frac{V_M}{nV}\right)} \tag{18.38}$$

If Eq. (18.38) is satisfied, then the converter operates in DCM at all points on the ac line sinusoid.

In steady state, the dc output voltage is given by Eq. (18.8). Upon substitution of the expression for R_e and solution for D, this equation becomes

$$D = \frac{2nV}{V_M}\sqrt{\frac{L}{RT_s}} \tag{18.39}$$

Insertion of this relationship into Eq. (18.38), and solution for L, yields

$$L < L_{crit} = \frac{RT_s}{4\left(1 + \frac{nV}{V_M}\right)^2} \tag{18.40}$$

For variations in load R and peak ac input voltage V_M, the worst case will occur at minimum R (maximum power) and minimum V_M. Hence, the designer should choose L to satisfy

$$L < L_{crit\text{-}min} = \frac{R_{min}T_s}{4\left(1 + \frac{nV}{V_{M\text{-}min}}\right)^2} \tag{18.41}$$

If this equation is violated, then at maximum load power and minimum input voltage amplitude, the convert will operate in CCM near the peak of the ac sinewave. This will lead to an input current waveform having substantial distortion.

18.3 CONTROL OF THE CURRENT WAVEFORM

A wide variety of approaches are known for active control of the input current waveform to attain input resistor emulation [14–33]. Average current control [17,18], input voltage feedforward [17], current-programmed control [19–22], hysteretic control and critical conduction mode control [23–27], and nonlinear carrier control [28–30] are briefly surveyed here. Other approaches include sliding-mode control [31], charge control [32], and ASDTIC control [33].

18.3.1 Average Current Control

Average current control is a popular method of implementing control of the input current waveform in a low-harmonic rectifier. This approach works in both continuous and discontinuous conduction modes, and can produce high-quality current waveforms over a wide range of input voltages and load powers. The problems of crossover distortion, found in some competing schemes such as current programmed control, are largely avoided. Several popular integrated circuits are available that implement average current control.

Figure 18.10 illustrates average current control of the input current waveform $\langle i_g(t)\rangle_{T_s}$ in a boost converter. The input current $i_g(t)$ flows through a shunt resistor. The voltage across this shunt resistor is amplified by an op amp circuit. This op amp circuit contains a low-pass filter characteristic that attenuates the high-frequency switching harmonics. The output voltage $v_a(t)$ of the op amp circuit is proportional to the low-frequency average value of $i_g(t)$:

$$v_a(t) = R_s\left\langle i_g(t)\right\rangle_{T_s} \tag{18.42}$$

This signal is compared to the reference voltage $v_r(t)$, to produce an error signal that drives the compensator network and pulse-width modulator as illustrated. If the feedback loop is well designed, then the error signal is small:

$$v_a(t) \approx v_r(t) \tag{18.43}$$

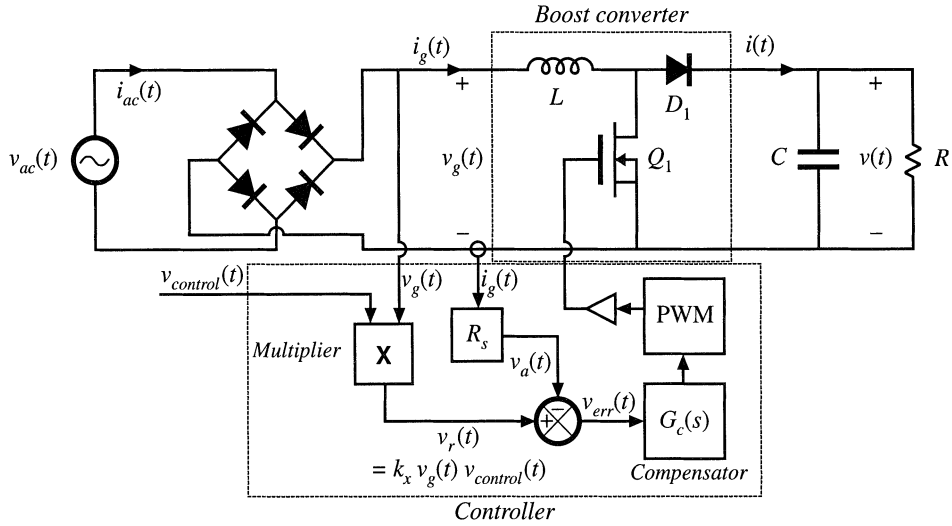

Fig. 18.11 Average current control of a boost converter, to obtain a low-harmonic rectifier.

The average current controller causes the sensed current $i_g(t)$ to follow the reference waveform $v_r(t)$.

To cause the input current to be proportional to the input voltage, the reference voltage $v_r(t)$ is derived from the sensed input voltage waveform, as in Fig. 18.11. The current reference signal $v_r(t)$ is derived from the sensed input voltage $v_g(t)$, and hence has a sinusoidal waveshape. Hence, the average current controller causes the average input current $i_g(t)$ to be proportional to the input voltage $v_g(t)$. The multiplier illustrated in Fig. 18.11 allows adjustment of the constant of proportionality, so that the magnitude of the emulated resistance can be controlled via a control signal $v_{control}(t)$. Let us assume that the multiplier terminal equations are

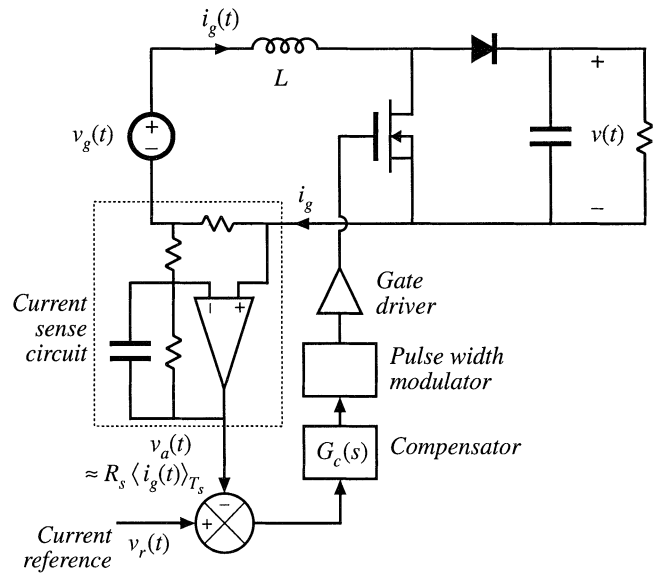

Fig. 18.10 Average current control of the input current in a boost converter.

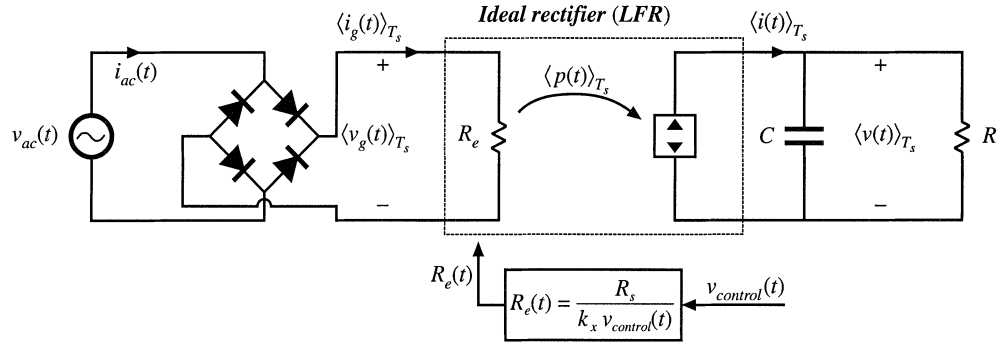

Fig. 18.12 Model of the system of Fig. 18.5, based on the loss-free resistor model of Fig. 18.1(c), which predicts the low-frequency system waveforms. This model assumes that the feedback loop of Fig. 18.5 operates ideally.

$$v_r(t) = k_x v_g(t) v_{control}(t) \tag{18.44}$$

Then the emulated resistance is

$$R_e = \frac{v_g(t)}{i_g(t)} = \frac{\left(\frac{v_r(t)}{k_x v_{control}(t)}\right)}{\left(\frac{v_a(t)}{R_s}\right)} \tag{18.45}$$

Here, Eqs. (18.44) and (18.42) have been used to eliminate v_g and i_g. Substitution of Eq. (18.43) leads to the result

$$R_e\left(v_{control}(t)\right) = \frac{R_s}{k_x v_{control}(t)} \tag{18.46}$$

Hence, if the feedback loop is well designed, then the system of Fig. 18.11 can be represented by the LFR model as in Fig. 18.12. The average current controller scheme of Fig. 18.11 and the model of Fig. 18.12 are independent of the dc–dc converter topology, and can be applied to systems containing CCM boost, buck-boost, Ćuk, SEPIC, and other topologies.

Average power flow and the output voltage are regulated by variation of the emulated resistance R_e, in average current control as well as in most other schemes. This is usually accomplished by use of a multiplier in the input voltage sensing path, as shown in Fig. 18.13. This control loop continually adjusts R_e to maintain balance of the average rectifier power $P_{av} = V_{g,rms}^2 / R_e$ and the load power P_{load}, such that the following relation is obeyed:

$$P_{av} = \frac{V_{g,rms}^2}{R_e} = P_{load} \tag{18.47}$$

Average current control works quite well. Its only disadvantages are the need to sense the average input current, rather than the transistor current, and the need for a multiplier in the controller circuit.

Most average current control implementations include provisions for feedforward of the input voltage amplitude. This allows disturbances in the ac input voltage amplitude to be canceled out by the

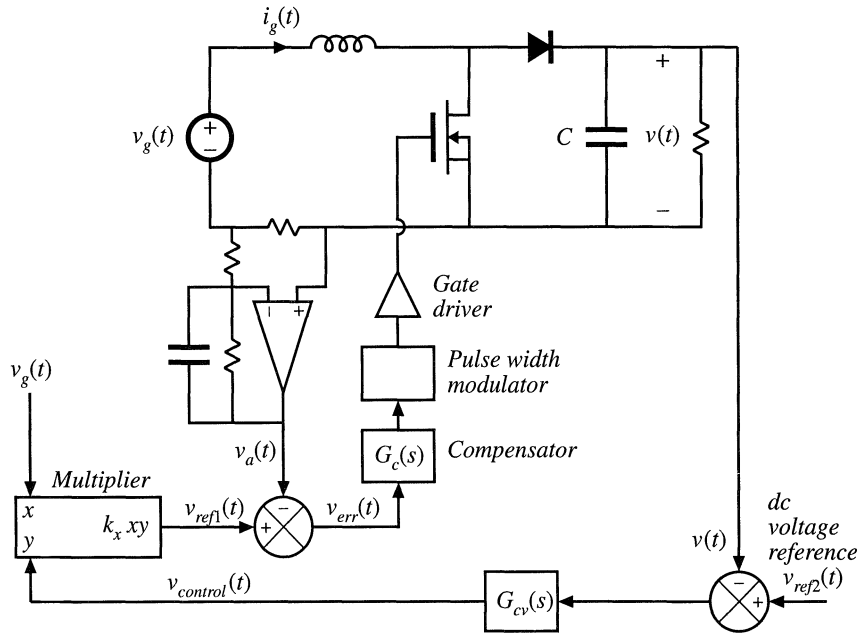

Fig. 18.13 Average current control incorporating a multiplier for regulation of the output voltage.

controller, such that the dc output voltage is unaffected.

Combination of Eqs. (18.44), (18.46), and (18.47), and solution for $v_{ref1}(t)$ leads to

$$v_{ref1}(t) = \frac{P_{av} v_g(t) R_s}{V_{g,rms}^2} \tag{18.48}$$

This equation shows how the reference voltage should be varied to maintain a given rectifier average power throughput P_{av}. Apparently, it is necessary to divide by the square of the rms input voltage amplitude. A controller that implements Eq. (18.48) is illustrated in Fig. 18.14. The multiplier block of Fig. 18.13 has been generalized to perform the function $k_v xy/z^2$. It is somewhat complicated to compute the rms value of a general ac waveform; however, the ac input voltage $v_g(t)$ normally is sinusoidal with negligible harmonics. Hence, the peak value of $v_g(t)$ is directly proportional to its rms value, and we can use the peak value V_M in place of $V_{g,rms}$. So the controller of Fig. 18.14 produces the reference voltage

$$v_{ref1}(t) = \frac{k_v v_{control}(t) v_g(t)}{V_M^2} \tag{18.49}$$

Comparison of Eqs. (18.48) and (18.49) leads to the conclusion that

$$P_{av} = \frac{k_v v_{control}(t)}{2R_s} \tag{18.50}$$

So the average power throughput is directly controlled by $v_{control}(t)$, and is independent of the input voltage $v_g(t)$.

Feedforward can cause the rectifier dc output voltage to be less sensitive to variations in the ac

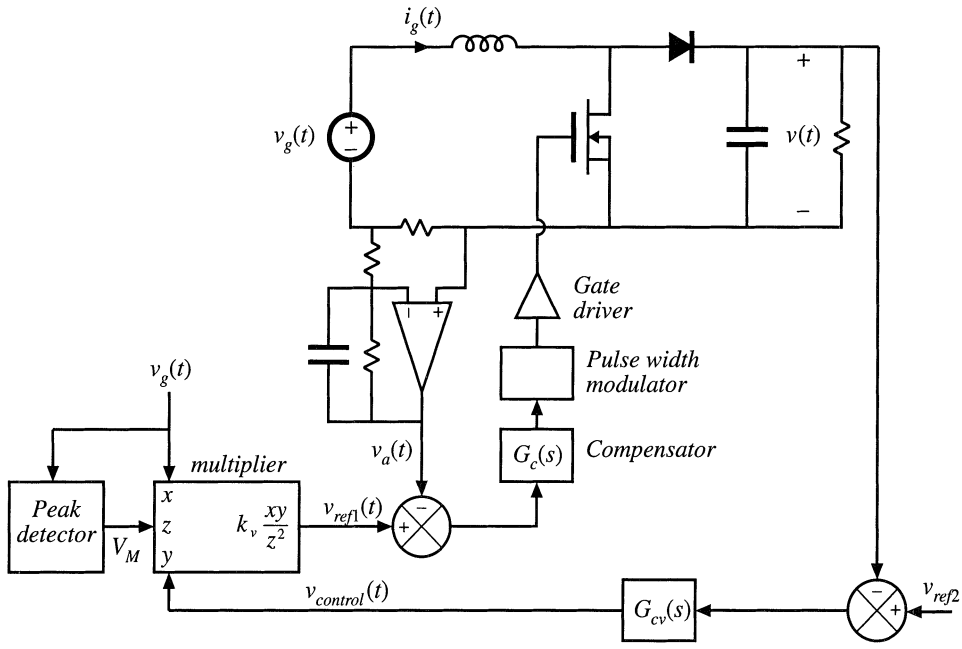

Fig. 18.14 Average current control incorporating input voltage feedforward.

line voltage. A disadvantage is the ac line current distortion introduced by variations in the voltage produced by the peak detector.

To aid in the design of the inner feedback loop that controls the ac line current waveshape, a converter model is needed that describes how the converter average input current depends on the duty cycle. We would prefer to apply the averaged small-signal modeling techniques of Chapter 7 here. The problem is that the variations in the duty cycle $d(t)$, as well as in the ac input voltage $v_g(t)$ and current $i_g(t)$, are not small. As a result, in general the small-signal assumptions are violated, and we are faced with the design of a control system that exhibits significant nonlinear time-varying behavior.

When the rectifier operates near periodic steady state, the output voltage $v(t)$ of a well-designed system exhibits small variations. So we can write

$$\langle v(t) \rangle_{T_s} = V + \hat{v}(t) \tag{18.51}$$

with

$$|\hat{v}(t)| \ll |V| \tag{18.52}$$

In other words, the small-signal assumption continues to be valid with respect to the rectifier output voltage. In the case of the boost converter, this allows us to linearize the converter input characteristics.

Following the approach of Chapter 7, we can express the average inductor voltage of the boost converter as

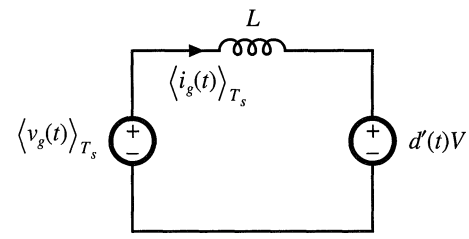

Fig. 18.15 Linearized model describing the boost converter input characteristics, corresponding to Eq. (18.55)

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t) \langle v(t) \rangle_{T_s} \tag{18.53}$$

This equation contains the nonlinear term $d'(t) \langle v(t) \rangle_{T_s}$. Substitution of Eq. (18.51) into (18.53) yields

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t) V - d'(t) \hat{v}(t) \tag{18.54}$$

When Eq. (18.52) is satisfied, then the nonlinear term $- d'(t)\hat{v}(t)$ is much smaller in magnitude than the linear term $- d'(t)V$. Therefore, we can discard the nonlinear term to obtain

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t) V \tag{18.55}$$

This linear differential equation is valid even though $i_g(t)$, $v_g(t)$, and $d(t)$ contain large variations.

An equivalent circuit corresponding to Eq. (18.55) is given in Fig. 18.15. The averaged control-to-input-current transfer function is found by setting the independent inputs other than $d(t)$ to zero, and then solving for i_g; the model predicts that this transfer function is

$$\frac{i_g(s)}{d(s)} = \frac{V}{sL} \tag{18.56}$$

where $i_g(s)$ is the Laplace transform of $\langle i_g(t) \rangle_{T_s}$. So the input characteristics of the boost rectifier can be linearized, even though the ac input variations are not small.

Unfortunately, Eq. (18.52) is not sufficient to linearize the equations describing the input characteristics of the buck-boost, SEPIC, Ćuk, and most other single-phase rectifiers. The control system design engineer must then deal with a truly nonlinear time-varying dynamical system.

One approach that is sometimes suggested employs the *quasi-static approximation* [34,35]. It is assumed that the ac line variations are much slower than the rectifier system dynamics, such that the rectifier always operates near equilibrium. The quiescent operating point changes slowly along the input sinusoid; an equilibrium analysis can be performed to find expressions for the slowly-varying "equilibrium" duty ratio and converter voltages and currents. The small-signal dc–dc converter transfer functions derived in Chapters 7 and 8 are evaluated using this time-varying operating point. The converter poles, zeroes, and gains are found to vary along the ac input sinusoid. An average current controller is designed using these time-varying transfer functions, such that the current loop gain has a positive phase margin at all operating points.

We expect that the quasi-static approximation should be valid if the rectifier system dynamics are sufficiently fast, and it is reasonable to anticipate that high-frequency PWM converters have dynam-

ics that are much faster than the ac line frequency. The problem is that no good condition on system parameters, which can justify the approximation, is known for the basic converter topologies. There is room for additional research in this area.

It is well-understood in the field of control systems that, when the rectifier system dynamics are not sufficiently fast, the quasi-static approximation yields neither sufficient nor necessary conditions for stability of the resulting design. Time-varying "loop gains" that always have a positive phase margin may nonetheless be unstable, and a negative phase margin does not always imply instability. Such phenomena are sometimes observed in rectifier systems. Even worse, it is difficult to justify the use of the Laplace transform on rectifiers described by time-varying differential equations, unless the quasi-static approximation can be validated.

18.3.2 Current Programmed Control

Another well-known approach to attaining input resistor emulation is the use of current-programmed control. As illustrated in Fig. 18.16, the programmed current $i_c(t)$ is made proportional to the ac input voltage. This causes the average inductor current, and hence also $\langle i_g(t) \rangle_{T_s}$, to approximately follow $v_g(t)$. As in average current control, a multiplier is used to adjust the emulated resistance and average power flow; the control signal $v_{control}(t)$ is typically used to stabilize the dc output voltage magnitude. Several rectifier control ICs are commercially available, which implement current-programmed control.

As discussed in Chapter 12, several mechanisms cause the average inductor current and hence also $\langle i_g(t) \rangle_{T_s}$ to differ from the programmed $i_c(t)$. These mechanisms introduce crossover distortion and line current harmonics. An artificial ramp having sufficiently large slope m_a is necessary to stabilize the

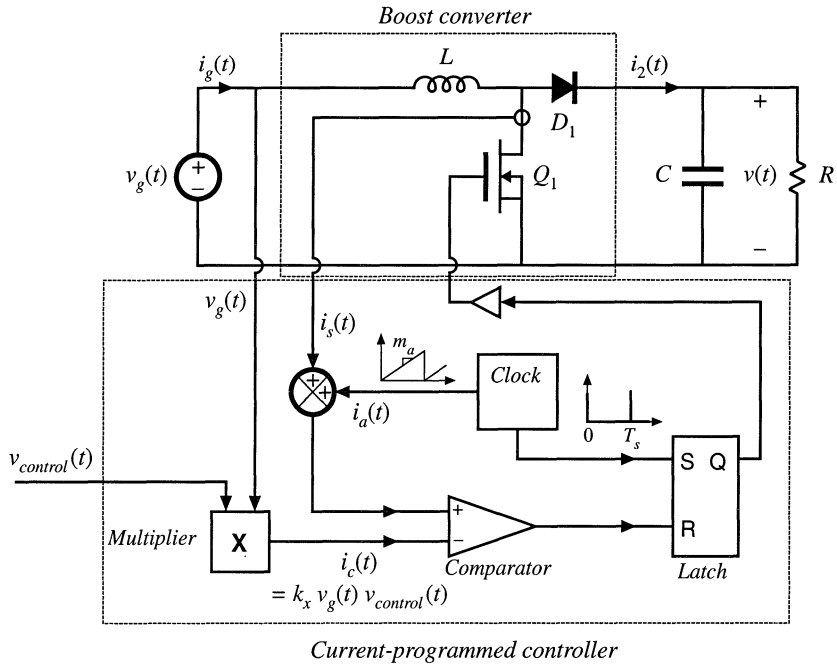

Fig. 18.16 Current-programmed control of a boost rectifier.

current-programmed boost converter when it operates in CCM with $d(t) > 0.5$. The addition of this ramp causes $\langle i_g(t) \rangle_{T_s}$ to differ from $i_c(t)$. Additional deviation is introduced by the inductor current ripple. Both mechanisms are most pronounced when the inductor current is small, near the zero-crossings of the ac line waveforms.

The static input characteristics, that is, the average input current vs. the input voltage, of the current-programmed boost converter are given by

$$\langle i_g(t) \rangle_{T_s} = \begin{cases} v_g(t) \dfrac{L i_c^2(t) f_s V}{2\left(V - v_g(t)\right)\left(v_g(t) + m_a L\right)^2} & \text{in DCM} \\ i_c(t) - \left(1 - \dfrac{v_g(t)}{V}\right)\left(m_a + \dfrac{v_g(t)}{2L}\right) T_s & \text{in CCM} \end{cases} \tag{18.57}$$

The converter operates in the continuous conduction mode when

$$\langle i_g(t) \rangle_{T_s} > \frac{T_s V}{2L} \frac{v_g(t)}{V} \left(1 - \frac{v_g(t)}{V}\right) \tag{18.58}$$

In terms of the control current $i_c(t)$, the condition for operation in CCM can be expressed

$$i_c(t) > \frac{T_s V}{L} \left(\frac{m_a L}{V} + \frac{v_g(t)}{V}\right)\left(1 - \frac{v_g(t)}{V}\right) \tag{18.59}$$

In the conventional current-programmed rectifier control scheme, the control current $i_c(t)$ is simply proportional to the ac input voltage:

$$i_c(t) = \frac{v_g(t)}{R_e} \tag{18.60}$$

where R_e is the emulated resistance that would be obtained if the average input current exactly followed the reference current $i_c(t)$. The static input characteristics given by Eqs. (18.57) to (18.60) are plotted in Fig. 18.17. The average input current $\langle i_g(t) \rangle_{T_s}$ is plotted as a function of the applied input voltage $v_g(t)$, for several values of emulated resistance R_e. The region near the CCM–DCM boundary is shown. The curves are plotted for a fixed artificial ramp having slope

$$m_a = \frac{V}{2L} \tag{18.61}$$

This is the minimum value of artificial ramp that stabilizes the boost current-programmed controller at all static operating points. Decreasing m_a below this value leads to instability at operating points in the continuous conduction mode at low $v_g(t)/V$.

To obtain resistor emulation, it is desired that the static input characteristics be linear and pass through the origin. It can be seen from Fig. 18.17 that this is not the case: the curves are reasonably linear in the continuous conduction mode, but exhibit significant curvature as the CCM–DCM boundary is approached. The resulting average current waveforms are summarized in Fig. 18.8.

To minimize the line current THD, it is apparent that the converter should be designed to operate deeply in the continuous conduction mode for most of the ac line cycle. This is accomplished with emulated resistances R_e that are much smaller than $R_{base} = 2L/T_s$. In addition, the artificial ramp slope m_a

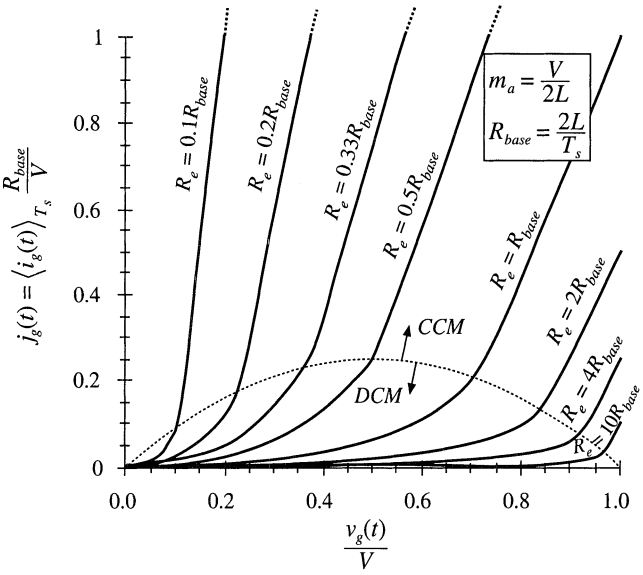

Fig. 18.17 Static input characteristics of a current-programmed boost converter, with minimum stabilizing artificial ramp of Eq. (18.61).

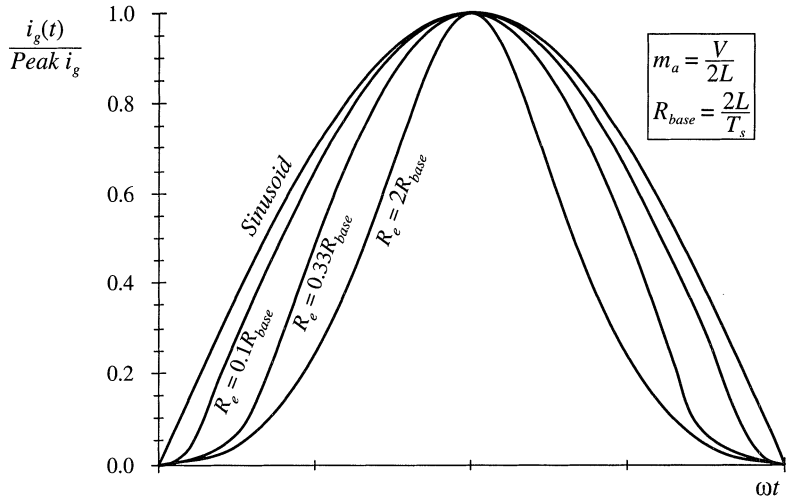

Fig. 18.18 Input current waveshapes predicted by the static input characteristics of Fig. 18.17, compared with a pure sinusoid. Curves are plotted for the case $V_M = 0.8V$, with minimum stabilizing artificial ramp.

should be no greater than otherwise necessary. In practice, THD of 5% to 10% can easily be obtained in rectifiers that function over a narrow range of rms input voltages and load currents. However, low THD cannot be obtained at all operating points in universal-input rectifiers; THD of 20% to 50% may be observed at maximum ac input voltage. This problem can be solved by biasing the current reference waveform. Design of current-programmed rectifiers is discussed in [19–22], and some strategies for solving this problem are addressed in [19].

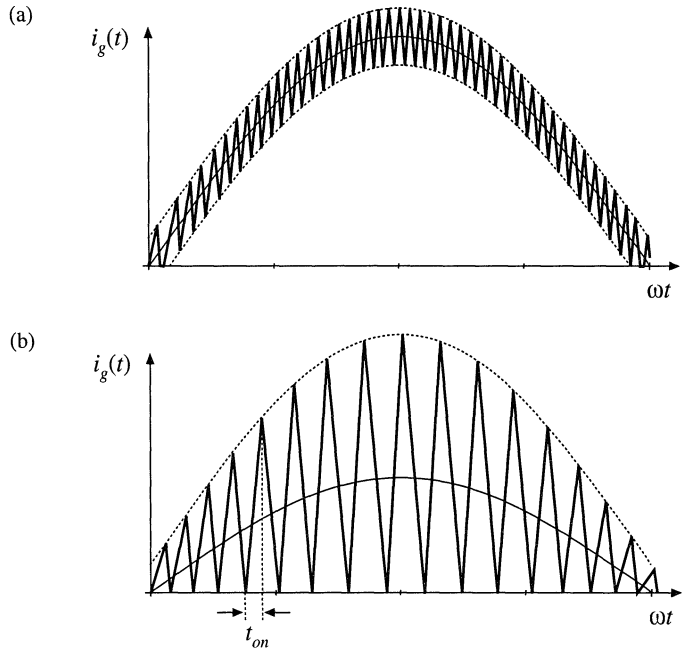

Fig. 18.19 Input current waveforms of two boost converters with hysteretic control: (a) ± 10% regulation band, (b) critical conduction mode operation (± 100% regulation band).

18.3.3 Critical Conduction Mode and Hysteretic Control

Another control scheme sometimes used in low-harmonic rectifiers, as well as in dc–dc converters and dc–ac inverters, is hysteretic control. Rather than operating at a fixed switching frequency and duty cycle, the hysteretic controller switches the transistor on and off as necessary to maintain a waveform within given limits. A special case of hysteretic control, called *critical conduction mode* control, is implemented in several commercially-available ICs, and is popular for low-harmonic rectifiers rated below several hundred Watts [23–25].

An example is the sinusoid of Fig. 18.19(a), in which the boost converter input current is controlled to follow a sinusoidal reference with a ± 10% tolerance. The inductor current increases when the transistor is on, and decreases when the transistor is off. So this hysteretic controller switches the transistor on whenever the input current falls below 90% of the reference input. The controller switches the transistor off whenever the input current exceeds 110% of the reference. Hysteretic controllers tend to have simple implementations. However, they have the disadvantages of variable switching frequency and reduced noise immunity.

Another example of hysteretic control is the waveform of Fig. 18.19(b). The lower limit is chosen to be zero, while the upper limit is twice the reference input. This controller operates the boost converter at the boundary between the continuous and discontinuous conduction modes. An alternative control scheme that generates the same waveform simply operates the transistor with constant on-time: the transistor is switched on when the inductor current reaches zero, and is switched off after a fixed

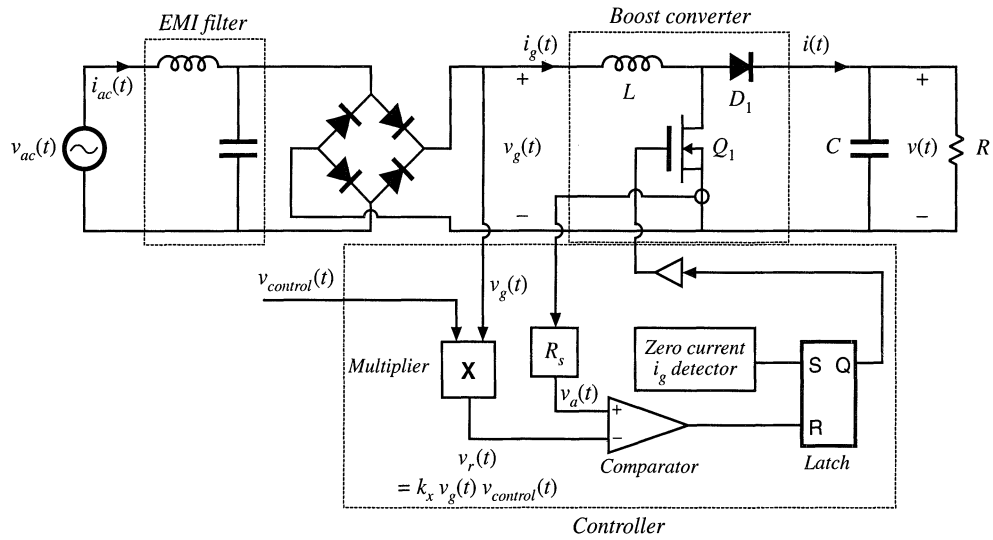

Fig. 18.20 A typical implementation of critical conduction mode control.

interval of length t_{on}. The resulting inductor current waveform will have a peak value that depends directly on the applied input voltage, and whose average value is one-half of its peak. With either control approach, the converter naturally exhibits loss-free-resistor or ideal rectifier behavior. The emulated resistance is

$$R_e = \frac{2L}{t_{on}} \tag{18.62}$$

This scheme has the advantage of small inductor size and low-cost control ICs. Disadvantages are increased peak currents, variable switching frequency, and the need for additional input EMI filtering.

A typical critical conduction mode controller is illustrated in Fig. 18.20. A zero-current detector senses when the inductor current is zero; this is typically accomplished by monitoring the voltage across the inductor. The zero-current detector sets a latch, turning on the transistor and initiating the switching period. The transistor current is also monitored, and is compared to a sinusoidal reference $v_r(t)$ that is proportional to the applied input voltage $v_g(t)$. When the sensed current is equal to the reference, the latch is reset and the transistor is turned off.

Since the switching frequency can vary, possibly over a wide range, it is important to carefully design the converter power stage. For a given power P, the required transistor on-time t_{on} can be found by combining Eqs. (18.17) and (18.62), and solving for t_{on}:

$$t_{on} = \frac{4LP}{V_M^2} \tag{18.63}$$

Application of the principle of volt-second balance to inductor L of Fig. 18.20 leads to the following equation:

$$v_g t_{on} + \left(v_g - V\right) t_{off} = 0 \tag{18.64}$$

Hence, the transistor off-time is given by

$$t_{off} = t_{on} \frac{v_g}{\left(V - v_g\right)} \tag{18.65}$$

The switching period T_s is equal to

$$T_s = t_{off} + t_{on} \tag{18.66}$$

Substitution of Eqs. (18.63) and (18.65) into Eq. (18.66) yields

$$T_s = \frac{4LP}{V_M^2} \frac{1}{\left(1 - \frac{v_g(t)}{V}\right)} \tag{18.67}$$

The following expression for switching frequency is found by substitution of Eq. (18.11) into Eq. (18.67):

$$f_s = \frac{1}{T_s} = \frac{V_M^2}{4LP}\left(1 - \frac{V_M}{V}\left|\sin(\omega t)\right|\right) \tag{18.68}$$

The maximum switching frequency occurs when $\sin(\omega t)$ equals zero:

$$\max f_s = \frac{V_M^2}{4LP} \tag{18.69}$$

The minimum switching frequency occurs at the peak of the sine wave:

$$\min f_s = \frac{V_M^2}{4LP}\left(1 - \frac{V_M}{V}\right) \tag{18.70}$$

Equations (18.69) and (18.70) can be used to select the value of the inductance L and the output voltage V, so that the switching frequency varies over an acceptable range.

18.3.4 Nonlinear Carrier Control

The nonlinear-carrier controller (NLC) is capable of attaining input resistor emulation in boost and other converters that operate in the continuous conduction mode. Implementation of the controller is quite simple, with no need for sensing of the input voltage or input current. There is also no need for a current loop error amplifier. The boost nonlinear-carrier charge controller is inherently stable and is free from the stability problems that require addition of an artificial ramp in current programmed controllers.

A CCM boost rectifier system with nonlinear-carrier charge control is illustrated in Fig. 18.21, and waveforms are given in Fig. 18.22. The reasoning behind this approach is as follows. It is desirable to control the transistor switch current $i_s(t)$. This pulsating current is much easier to sense than the continuous converter input current—a simple current transformer can be used, as in Fig. 18.21. Further, it is desirable to control the integral of this current, or the charge, for two reasons: (1) integration of the waveform leads to improved noise immunity, and (2) the integral of the waveform is directly related to its average value,

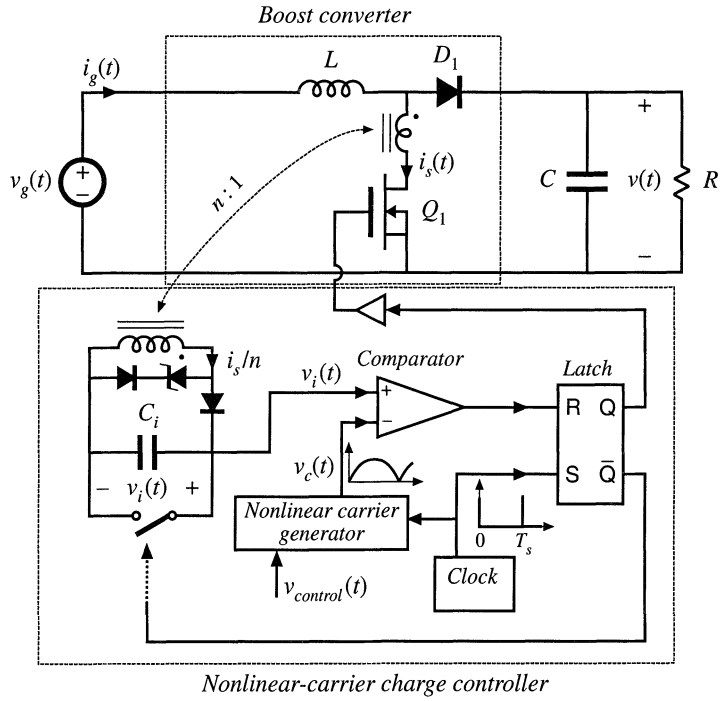

Fig. 18.21 Nonlinear-carrier charge control of a boost converter.

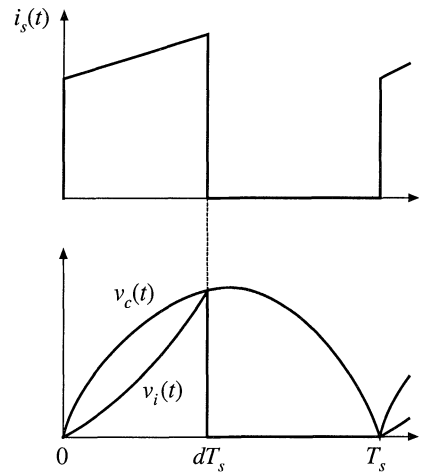

Fig. 18.22 Transistor current $i_s(t)$, parabolic carrier voltage $v_c(t)$, and integrator voltage $v_i(t)$ waveforms for the NLC-controlled boost rectifier of Fig. 18.21.

$$\langle i_s(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} i_s(\tau)d\tau \tag{18.71}$$

In a fixed-frequency system, T_s is constant, and the integral over one switching period is proportional to the average value. Hence the average switch current can be controlled to be proportional to a reference signal by simply switching the transistor off when the integral of the switch current is equal to the reference. In the controller of Fig. 18.21, the switch current $i_s(t)$ is scaled by the transformer turns ratio n, and then integrated by capacitor C_i, such that

$$v_i(t) = \frac{1}{C_i}\int_0^{dT_s} \frac{i_s(\tau)}{n}\,d\tau \qquad \text{for } 0 < t < dT_s \tag{18.72}$$

The integrator voltage $v_i(t)$ is reset to zero at the end of each switching period, and the integration process begins anew at the beginning of the next switching period. So at the instant that the transistor is switched off, the voltage $v_i(dT_s)$ is proportional to the average switch current:

$$v_i(dT_s) = \frac{\langle i_s\rangle_{T_s}}{nC_i f_s} \qquad \text{for interval } 0 < t < T_s \tag{18.73}$$

How should the average switch current be controlled? To obtain input resistor emulation, it is desired that

$$\langle i_g(t)\rangle_{T_s} = \frac{\langle v_g(t)\rangle_{T_s}}{R_e(v_{control})} \tag{18.74}$$

It is further desired to avoid sensing either $i_g(t)$ or $v_g(t)$. As with other schemes, we will sense the dc output voltage $\langle v(t)\rangle_{T_s}$, to construct a low-bandwidth feedback loop that balances the average input and output powers. So let us determine the relationship between $\langle i_s(t)\rangle_{T_s}$ and $\langle v(t)\rangle_{T_s}$ implied by Eq. (18.74). If we assume that the boost converter operates in the continuous conduction mode, then we can write

$$\langle i_s(t)\rangle_{T_s} = d(t)\,\langle i_g(t)\rangle_{T_s} \tag{18.75}$$

and

$$\langle v_g(t)\rangle_{T_s} = d'(t)\,\langle v(t)\rangle_{T_s} \tag{18.76}$$

Substitution of Eqs. (18.75) and (18.76) into Eq. (18.74) leads to

$$\langle i_s(t)\rangle_{T_s} = d(t)\big(1 - d(t)\big)\frac{\langle v(t)\rangle_{T_s}}{R_e(v_{control})} \tag{18.77}$$

The controller of Fig. 18.21 implements this equation.

The nonlinear carrier generator of Fig. 18.21 produces the parabolic waveform $v_c(t)$, given by

$$v_c(t) = v_{control}\left(\frac{t}{T_s}\right)\left(1 - \frac{t}{T_s}\right) \qquad \text{for } 0 \le t \le T_s$$
$$v_c(t + T_s) = v_c(t) \tag{18.78}$$

This waveform is illustrated in Fig. 18.22. Note that Eq. (18.78) resembles Eq. (18.77), with $d(t)$ replaced by (t/T_s). The controller switches the transistor off at time $t = dT_s$ when the integrator voltage $v_i(t)$ is equal to the carrier waveform $v_c(t)$. Hence, it is true that

$$v_i(dT_s) = v_c(dT_s) = v_{control}(t)\, d(t)\left(1 - d(t)\right) \tag{18.79}$$

Substitution of Eq. (18.73) yields

$$\frac{\langle i_s(t)\rangle_{T_s}}{nC_i f_s} = v_{control}(t)\, d(t)\left(1 - d(t)\right) \tag{18.80}$$

This is of the same form as Eq. (18.77). Comparison of Eqs. (18.77) and (18.80) reveals that the emulated resistance R_e is given by

$$R_e(v_{control}) = d(t)\left(1 - d(t)\right)\frac{\langle v(t)\rangle_{T_s}}{\langle i_s(t)\rangle_{T_s}} = \frac{\langle v(t)\rangle_{T_s}}{nC_i f_s v_{control}(t)} \tag{18.81}$$

If the dc output voltage and the control voltage have negligible ac variation, then R_e is essentially constant, and the ac line current will exhibit low harmonic distortion. So neither the input voltage nor the input current need be sensed, and input resistor emulation can be obtained in CCM boost converters by sensing only the switch current.

A simple way to generate the parabolic carrier waveform uses two integrators, as illustrated in Fig. 18.23. The slowly varying control voltage $v_{control}(t)$ is integrated, to obtain a ramp waveform $v_r(t)$ whose peak amplitude is proportional to $v_{control}(t)$. The dc component of this waveform is removed, and then integrated again. The output of the second integrator is the parabolic carrier $v_c(t)$, illustrated in Fig. 18.22 and given by Eq. (18.78). Both integrators are reset to zero before the end of each switching period

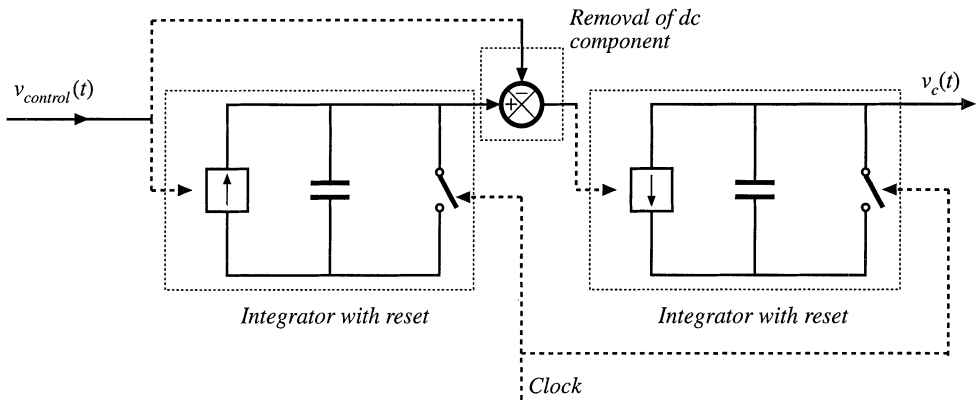

Fig. 18.23 Generation of parabolic carrier waveform by double integration.

by the clock generator. The amplitude of the parabolic carrier, and hence also the emulated resistance, can be controlled by variation of $v_{control}(t)$.

Equations (18.75) and (18.76) are valid only when the converter operates in the continuous conduction mode. In consequence, the ac line current waveform is distorted when the converter operates in DCM. Since this occurs near the zero crossings of the ac line voltage, crossover distortion is generated. Nonetheless, the harmonic distortion is less severe than in current-programmed schemes, and it is feasible to construct universal-input rectifiers that employ the NLC control approach. Total harmonic distortion is analyzed and plotted in [28].

Nonlinear carrier control can be applied to current-programmed boost rectifiers, as well as to other rectifiers based on the buck-boost, SEPIC, Ćuk, or other topologies, with either integral charge control or peak-current-programmed control [28,29]. In these cases, a different carrier waveform must be employed. A nonlinear-carrier controller in which the ac input voltage $v_g(t)$ is sensed, rather than the switch current $i_s(t)$, is described in [30].

18.4 SINGLE-PHASE CONVERTER SYSTEMS INCORPORATING IDEAL RECTIFIERS

An additional issue that arises in PWM rectifier systems is the control of power drawn from the ac line, the power delivered to the dc load, and the energy stored in a bulk energy storage capacitor.

18.4.1 Energy Storage

It is usually desired that the dc output voltage of a converter system be regulated with high accuracy. In practice, this is easily accomplished using a high-gain wide-bandwidth feedback loop. A well-regulated dc output voltage $v(t) = V$ is then obtained, which has negligible ac variations. For a given constant load characteristic, the load current I and the instantaneous load power $p_{load}(t) = P_{load}$, are also constant:

$$p_{load}(t) = v(t)i(t) = VI \tag{18.82}$$

However, the instantaneous input power $p_{ac}(t)$ of a single-phase ideal rectifier is not constant:

$$p_{ac}(t) = v_g(t)i_g(t) \tag{18.83}$$

If $v_g(t)$ is given by Eq. (18.11), and if $i_g(t)$ follows Eq. (18.1), then the instantaneous input power becomes

$$p_{ac}(t) = \frac{V_M^2}{R_e}\sin^2(\omega t) = \frac{V_M^2}{2R_e}\left(1 - \cos(2\omega t)\right) \tag{18.84}$$

which varies with time. The instantaneous input power is zero at the zero crossings of the ac input voltage. Equations (18.82) and (18.84) are illustrated in Fig. 18.24(a). Note that the desired instantaneous load power $p_{load}(t)$ is not equal to the desired instantaneous rectifier input power $p_{ac}(t)$. Some element within the rectifier system must supply or consume the difference between these two instantaneous powers.

Since the ideal rectifier does not consume or generate power, nor does it contain significant internal energy storage, it is necessary to add to the system a low-frequency energy storage element such

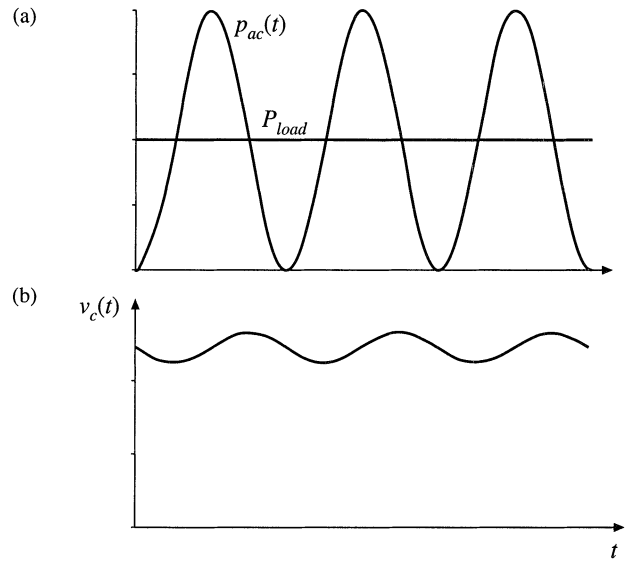

Fig. 18.24 Waveforms of a single-phase ideal rectifier system: (a) pulsating ac input power $p_{ac}(t)$, and constant dc load power P_{load}; (b) energy storage capacitor voltage $v_C(t)$.

as an electrolytic capacitor. The difference between the instantaneous input and load powers flows through this capacitor.

The waveforms of rectifier systems containing reactive elements can be determined by solution of the rectifier energy equation [36,37]. If the energy storage capacitor C is the only system element capable of significant low-frequency energy storage, then the power $p_C(t)$ flowing into the capacitor is equal to the difference between the instantaneous input and output powers:

$$p_C(t) = \frac{dE_C(t)}{dt} = \frac{d\left(\frac{1}{2}Cv_C^2(t)\right)}{dt} = p_{ac}(t) - p_{load}(t) \tag{18.85}$$

where C is the capacitance, $v_C(t)$ is the capacitor voltage, and $E_C(t)$ is the energy stored in the capacitor. Hence as illustrated in Fig. 18.24(b), when $p_{ac}(t) > p_{load}(t)$ then energy flows into the capacitor, and $v_C(t)$ increases. Likewise, $v_C(t)$ decreases when $p_{ac}(t) < p_{load}(t)$. So the capacitor voltage $v_C(t)$ must be allowed to increase and decrease as necessary to store and release the required energy. In steady-state, the average values of $p_{ac}(t)$ and $p_{load}(t)$ must be equal, so that over one ac line cycle there is no net change in capacitor stored energy.

Where can the energy storage capacitor be placed? It is necessary to separate the energy storage capacitor from the regulated dc output, so that the capacitor voltage is allowed to independently vary as illustrated in Fig. 18.24(b). A conventional means of accomplishing this is illustrated in Fig. 18.25. A second dc–dc converter is inserted, between the energy storage capacitor and the regulated dc load. A wide-bandwidth feedback loop controls this converter, to attain a well-regulated dc load voltage. The capacitor voltage $v_C(t)$ is allowed to vary. Thus, this system configuration is capable of (1) wide-bandwidth control of the ac line current waveform, to attain unity power factor, (2) internal low-frequency energy storage, and (3) wide-bandwidth regulation of the dc output voltage. It is also possible to integrate these functions into a single converter, provided that the required low-frequency independence of the input, output, and capacitor voltages is maintained [38].

The energy storage capacitor also allows the system to function in other situations in which the instantaneous input and output powers differ. For example, it is commonly required that the output volt-

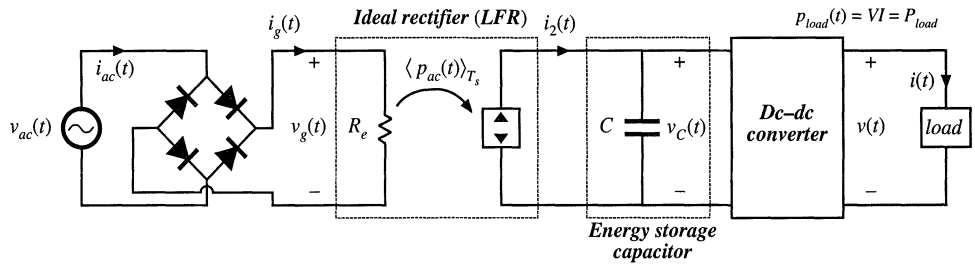

Fig. 18.25 Elements of a single-phase-ac to dc power supply, in which the ac line current and dc load voltage are independently regulated with high bandwidth. An internal independent energy storage capacitor is required.

age remain regulated during ac line voltage failures of short duration. The *hold-up time* is the duration that the output voltage $v(t)$ remains regulated after $v_{ac}(t)$ has become zero. A typical requirement is that the system continue to supply power to the load during one complete missing ac line cycle, that is, for 20 msec in a 50 Hz system. During the hold-up time, the load power is supplied entirely by the energy storage capacitor. The value of capacitance should be chosen such that at the end of the hold-up time, the capacitor voltage $v_C(t)$ exceeds the minimum value that the dc–dc converter requires to produce the desired load voltage.

The energy storage function could be performed by an element other than a capacitor, such as an inductor. However, use of an inductor is a poor choice, because of its high weight and cost. For example, a 100 μF 100 V electrolytic capacitor and a 100 μH 100 A inductor can each store 1 Joule of energy. But the capacitor is considerably smaller, lighter, and less expensive.

A problem introduced by the energy storage capacitor is the large *inrush current* observed during the system turn-on transient. The capacitor voltage $v_C(t)$ is initially zero; substantial amounts of charge and energy are required to raise this voltage to its equilibrium value. The boost converter is not capable of limiting the magnitude of the resulting inrush current: even when $d(t) = 0$, a large current flows through the boost converter diode to the capacitor, as long as the converter output voltage is less than the input voltage. Some additional circuitry is required to limit the inrush current of the boost converter. Converters having a buck–boost type conversion ratio are inherently capable of controlling the inrush current. This advantage comes at the cost of additional switch stress.

It is also possible to design the ideal rectifier to operate correctly when connected to utility power systems anywhere in the world. *Universal input* rectifiers can operate with nominal ac rms voltage magnitudes as low as the 100 V encountered in a portion of Japan, or as high as the 260 V found in western Australia, with ac line frequencies of either 50 Hz or 60 Hz. Regardless of the ac input voltage, the universal-input rectifier produces a constant nominal dc output voltage V_C.

Let us now consider in more detail the low-frequency energy storage process of the system of Fig. 18.25. Let us assume that the dc–dc converter contains a controller having bandwidth much greater than the ac line frequency, such that the load voltage contains negligible low-frequency variations. A low-frequency model of the dc–dc converter is then as illustrated in Fig. 18.26. The dc–dc converter produces constant voltage $v(t) = V$, modeled by a voltage source as shown. This causes the load to draw constant current $i(t) = I$, leading to load power $p_{load}(t) = P_{load}$. To the extent that converter losses can be neglected, the dc–dc converter input port draws power P_{load}, regardless of the value of $v_C(t)$. So the dc–dc converter input port can be modeled as a constant power sink, of value P_{load}.

The model of Fig. 18.26 implies that the difference between the rectifier power $p_{ac}(t)$ and the load power P_{load} flows into the capacitor, as given by Eq. (18.85). The capacitor voltage increases when $p_{ac}(t)$ exceeds P_{load}, and decreases when $p_{ac}(t)$ is less than P_{load}. In steady state, the average values of $p_{ac}(t)$ and P_{load} must be equal. But note that $p_{ac}(t)$ is determined by the magnitudes of $v_{ac}(t)$ and R_e, and

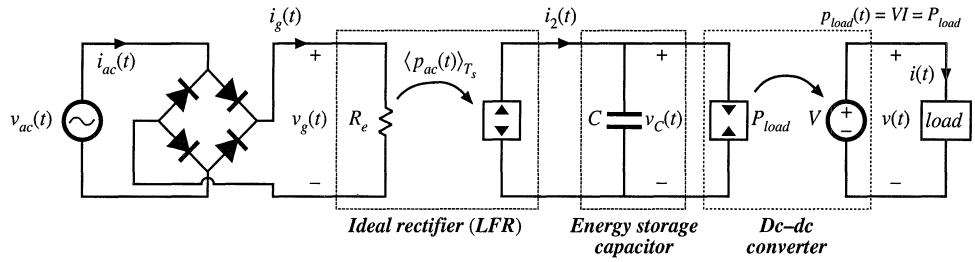

Fig. 18.26 Low-frequency equivalent circuit of the system of Fig. 18.25.

not by the load. The system of Fig. 18.26 contains no mechanism to cause the average rectifier power and load power to be equal. In consequence, it is necessary to add an additional control system that adjusts R_e as necessary, to cause the average rectifier output power and dc–dc converter input power to balance. The conventional way to accomplish this is simply to regulate the dc component of $v_C(t)$.

A complete system containing ideal rectification, energy storage, and wide-bandwidth output voltage regulation is illustrated in Fig. 18.27. This system incorporates the boost converter and controller of Fig. 18.5, as well as a generic dc–dc converter with output voltage feedback. In addition, the system contains a low-bandwidth feedback loop, which regulates the dc component of the energy-storage capacitor voltage to be equal to a reference voltage v_{ref2}. This is accomplished by slow variations of $v_{control}(t)$ and R_e. This controller should have sufficiently small loop gain at the even harmonics of the ac line frequency, so that variations in R_e are much slower than the ac line frequency.

Increasing the bandwidth of the energy storage capacitor voltage controller can lead to significant ac line current harmonics. When this controller has wide bandwidth and high gain, then it varies $R_e(t)$ quickly, distorting the ac line current waveform. In the extreme limit of perfect regulation of the

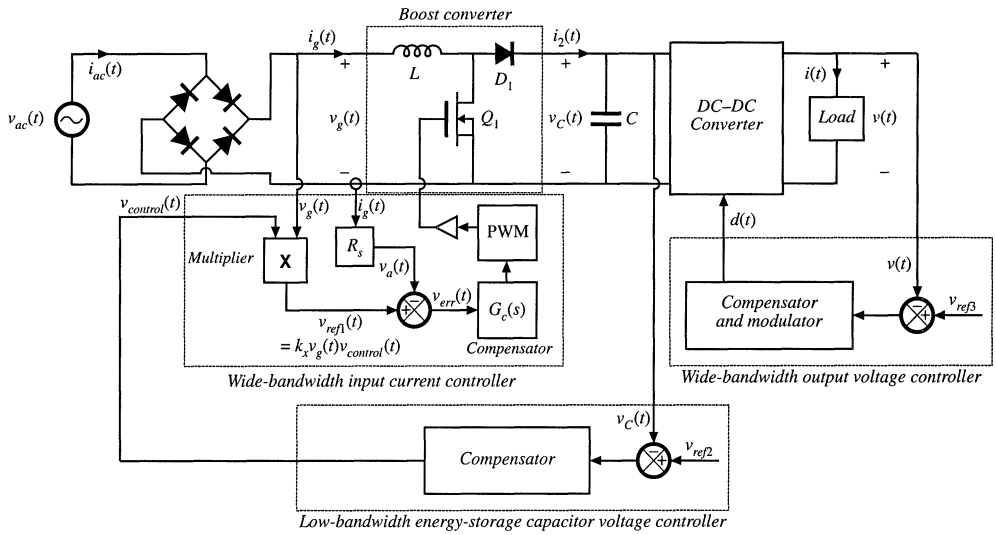

Fig. 18.27 A complete dc power supply system incorporating a near-ideal single-phase boost rectifier system, energy storage capacitor, and dc-dc converter. Wide-bandwidth feedback loops regulate the ac line current waveform and the dc load voltage, and a slow feedback loop regulates the energy storage capacitor voltage.

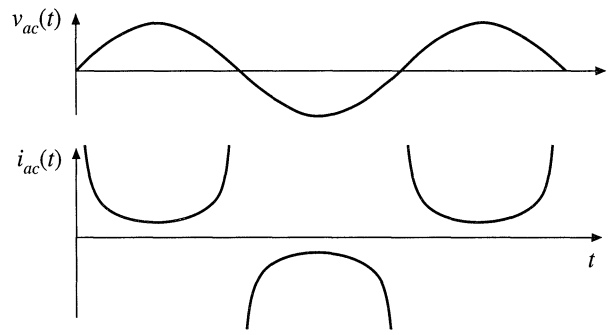

Fig. 18.28 Ac line current waveform of the single-phase ideal rectifier with output voltage feedback, when it supplies constant instantaneous power to a dc load. The THD tends to infinity, and the power factor tends to zero.

energy storage capacitor voltage $v_C(t) = V_C$, then the capacitor stored energy is constant, and the instantaneous input ac line power $p_{ac}(t)$ and load power $p_{load}(t)$ are equal. The controller prevents the energy-storage capacitor from performing its low-frequency energy storage function. The ac line current then becomes

$$i_{ac}(t) = \frac{p_{ac}(t)}{v_{ac}(t)} = \frac{p_{load}(t)}{v_{ac}(t)} = \frac{P_{load}}{V_M \sin(\omega t)} \tag{18.86}$$

This waveform is sketched in Fig. 18.28. In this idealized limiting case, the ac line current tends to infinity at the zero crossings of the ac line voltage waveform, such that the instantaneous input power is constant. It can be shown that the THD of this current waveform is infinite, and its distortion factor and power factor are zero. So the bandwidth of this controller should be limited.

The energy storage capacitor voltage ripple can be found by integration of Eq. (18.85). Under steady-state conditions, where the average value of $p_{ac}(t) = P_{load}$, integration of Eq. (18.85) yields

$$E_C(t) = \tfrac{1}{2} C v_C^2(t) = E_C(0) + \int_0^t \left(-P_{load} \cos(2\omega t)\right) dt \tag{18.87}$$

where ω is the ac line frequency. Evaluation of the integral leads to

$$E_C(t) = E_C(0) - \frac{P_{load} \sin(2\omega t)}{2\omega} \tag{18.88}$$

Therefore, the capacitor voltage waveform is

$$v_C(t) = \sqrt{\frac{2E_C(t)}{C}} = \sqrt{v_C^2(0) - \frac{P_{load}}{\omega C} \sin(2\omega t)} \tag{18.89}$$

It can be verified that the rms value of this waveform is $V_{C,rms} = v_C(0)$. Hence, Eq. (18.89) can be written

$$v_C(t) = V_{C,rms} \sqrt{1 - \frac{P_{load}}{\omega C V_{C,rms}^2} \sin(2\omega t)} \tag{18.90}$$

This waveform is sketched in Fig. 18.24(b). The minimum and maximum values of the capacitor voltage occur when $\sin(2\omega t)$ is equal to 1 and –1, respectively. Therefore, the peak-to-peak capacitor voltage rip-

ple is

$$2\Delta v_C = V_{C,rms}\left[\sqrt{1+\frac{P_{load}}{\omega C V_{C,rms}^2}}-\sqrt{1-\frac{P_{load}}{\omega C V_{C,rms}^2}}\right]\approx\frac{P_{load}}{\omega C V_{C,rms}} \tag{18.91}$$

The approximation is valid for $P_{load}/(\omega C V_{C,rms}^2)$ sufficiently less than one, a condition that is satisfied whenever the ac voltage ripple is sufficiently less than $V_{C,rms}$.

18.4.2 Modeling the Outer Low-Bandwidth Control System

As discussed above, the outer low-bandwidth controller, which varies the emulated resistance as necessary to balance the average ac input and dc load powers, is common to all near-ideal rectifier systems. For design of this controller, the rectifier can be modeled using the loss-free resistor (LFR) model. Perturbation and linearization of the LFR leads to a small-signal equivalent circuit that predicts the relevant small-signal transfer functions. Such a model is derived in this section [2,39,40].

It is desirable to stabilize the rectifier output voltage against variations in load power, ac line voltage, and component characteristics. Hence, a voltage feedback loop is necessary. As discussed in Section 18.4.1, this loop cannot attempt to remove the capacitor voltage ripple that occurs at the second harmonic of the ac line frequency, 2ω, since doing so would require that $R_e(t)$ change significantly at the second harmonic frequency. This would introduce significant distortion, phase shift, and power factor degradation into the ac line current waveform. In consequence this loop must have sufficiently small gain at frequency 2ω, and hence its bandwidth must be low. Therefore, for the purposes of designing the low-bandwidth outer control loop, it is unnecessary to model the system high-frequency behavior. It can be assumed that any inner wide-bandwidth controller operates ideally at low frequencies, such that the ideal rectifier model of Fig. 18.29(a) adequately represents the low-frequency system behavior.

A small-signal model is derived here that correctly predicts the control-to-output transfer function and output impedance of any rectifier system that can be modeled as a loss-free resistor. The model neglects the complicating effects of high-frequency switching ripple, and is valid for control variations at frequencies sufficiently less than the ac line frequency. Both resistive and dc-dc converter/regulator loads are treated.

The steps in the derivation of the small-signal ac model are summarized in Fig. 18.29. Figure 18.29(a) is the basic ideal rectifier model, in which the converter high frequency switching ripple is removed via averaging over the switching period T_s, but waveform frequency components slower than the switching frequency are correctly modeled, including the 2ω second-harmonic and dc components of output voltage. It is difficult to use this model in design of the feedback loop because it is highly nonlinear and time-varying.

If the ac input voltage $v_g(t)$ is

$$v_g(t) = \sqrt{2}\, v_{g,rms}\left|\sin(\omega t)\right| \tag{18.92}$$

then the model of Fig. 18.29(a) predicts that the instantaneous output power $\langle p(t)\rangle_{T_s}$ is

$$\langle p(t)\rangle_{T_s} = \frac{\langle v_g(t)\rangle_{T_s}^2}{R_e(v_{control}(t))} = \frac{v_{g,rms}^2}{R_e(v_{control}(t))}\left(1-\cos(2\omega t)\right) \tag{18.93}$$

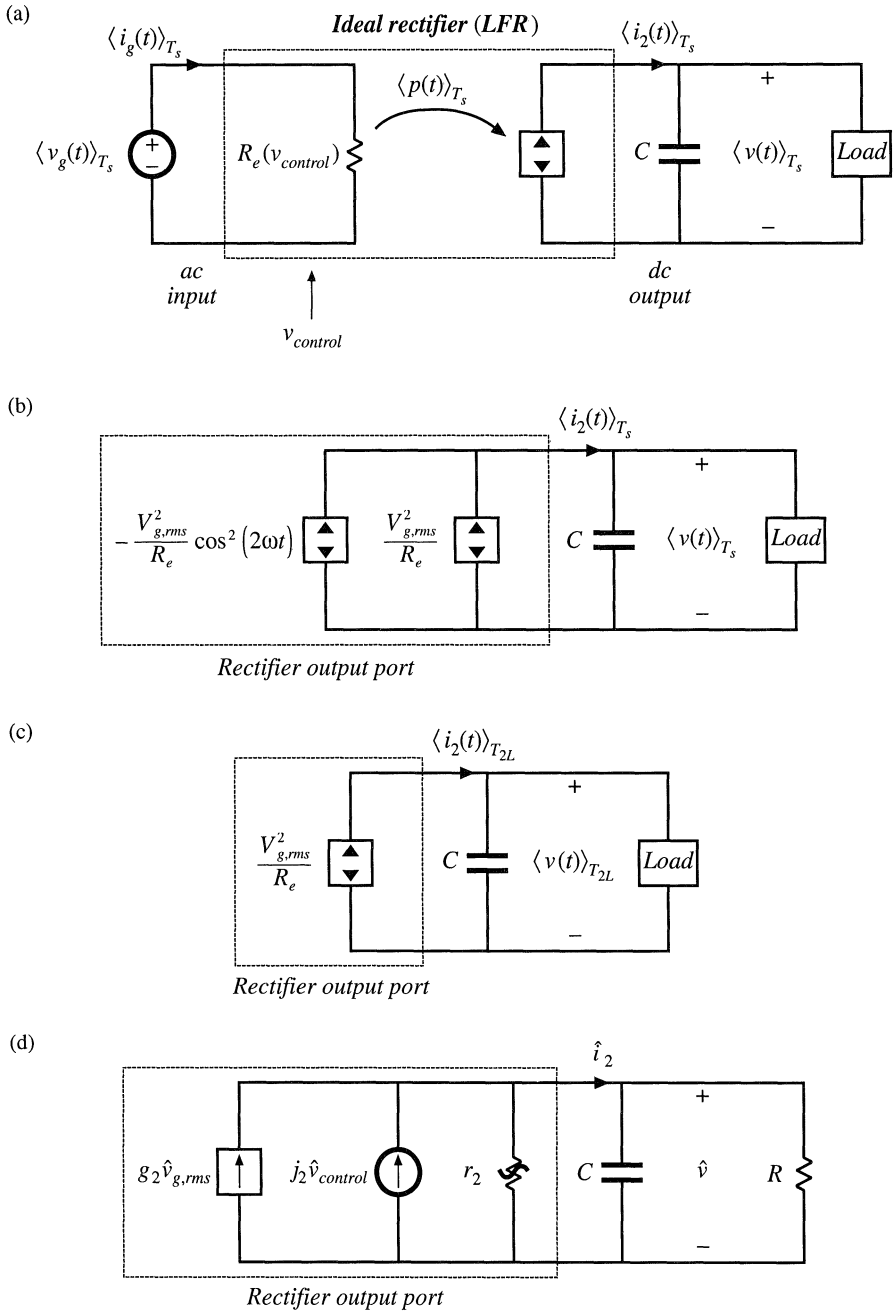

Fig. 18.29 Steps in the derivation of low-frequency small-signal rectifier model: (a) large-signal LFR model, averaged over one switching period T_s; (b) separation of power source into its constant and time-varying components; (c) removal of second-harmonic components by averaging over one-half of the ac line period, T_{2L}; (d) small-signal model obtained by perturbation and linearization of Fig. 18.29(c).

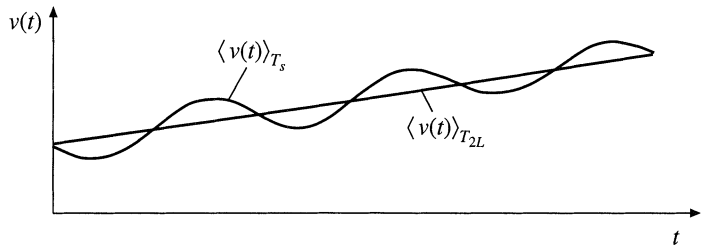

Fig. 18.30 Removal of components of $v(t)$ at the harmonics of the ac line frequency, by averaging over one-half of the ac line period, T_{2L}.

The output power is comprised of a constant term $v_{g,rms}^2/R_e$, and a term that varies at the second harmonic of the ac line frequency. These two terms are explicitly identified in Fig. 18.29(b).

The second-harmonic variation in $\langle p(t)\rangle_{T_s}$ leads to time-varying system equations, and slow variations in $v_{control}(t)$ lead to an output voltage spectrum containing components not only at the frequencies present in $v_{control}(t)$, but also at the even harmonics of the ac line frequency and their sidebands, as well as at the switching frequency and its harmonics and sidebands. It is desired to model only the low-frequency components excited by slow variations in $v_{control}(t)$, the load, and the ac line voltage amplitude $v_{g,rms}$. The even harmonics of the ac line frequency can be removed by averaging over one-half of the ac line period

$$T_{2L} = \frac{1}{2}\frac{2\pi}{\omega} = \frac{\pi}{\omega} \tag{18.94}$$

Hence, we average over the switching period T_s to remove the switching harmonics, and then average again over one-half of the ac line period T_{2L} to remove the even harmonics of the ac line frequency. The resulting model is valid for frequencies sufficiently less than the ac line frequency ω. Averaging of the rectifier output voltage is illustrated in Fig. 18.30: averaging over T_{2L} removes the ac line frequency harmonics, leaving the underlying low-frequency variations. By averaging the model of Fig. 18.29(b) over T_{2L}, we obtain the model of Fig. 18.29(c). This step removes the second-harmonic variation in the power source.

The equivalent circuit of Fig. 18.29(c) is time-invariant, but nonlinear. We can now perturb and linearize as usual, to construct a small-signal ac model that describes how slow variations in $v_{control}(t)$, $v_{g,rms}$, and the load, affect the rectifier output waveforms. Let us assume that the averaged output voltage $\langle v(t)\rangle_{T_{2L}}$, rectifier averaged output current $\langle i_2(t)\rangle_{T_{2L}}$, rms line voltage amplitude $v_{g,rms}$, and control voltage $v_{control}(t)$, can be represented as quiescent values plus small slow variations:

$$\begin{aligned}
\langle v(t)\rangle_{T_{2L}} &= V + \hat{v}(t) \\
\langle i_2(t)\rangle_{T_{2L}} &= I_2 + \hat{i}_2(t) \\
v_{g,rms} &= V_{g,rms} + \hat{v}_{g,rms}(t) \\
v_{control}(t) &= V_{control} + \hat{v}_{control}(t)
\end{aligned} \tag{18.95}$$

with

$$\begin{aligned} V &\gg \left|\hat{v}(t)\right| \\ I_2 &\gg \left|\hat{i}_2(t)\right| \\ V_{g,rms} &\gg \left|\hat{v}_{g,rms}(t)\right| \\ V_{control} &\gg \left|\hat{v}_{control}(t)\right| \end{aligned} \tag{18.96}$$

In the averaged model of Fig. 18.29(c), $\langle i_2(t)\rangle_{T_{2L}}$ is given by

$$\begin{aligned} \left\langle i_2(t)\right\rangle_{T_{2L}} &= \frac{\left\langle p(t)\right\rangle_{T_{2L}}}{\left\langle v(t)\right\rangle_{T_{2L}}} = \frac{v_{g,rms}^2(t)}{R_e(v_{control}(t))\left\langle v(t)\right\rangle_{T_{2L}}} \\ &= f\left(v_{g,rms}(t), \left\langle v(t)\right\rangle_{T_{2L}}, v_{control}(t)\right) \end{aligned} \tag{18.97}$$

This equation resembles DCM buck-boost Eq. (11.45), and linearization proceeds in a similar manner. Expansion of Eq. (18.97) in a three-dimensional Taylor series about the quiescent operating point, and elimination of higher-order nonlinear terms, leads to

$$\hat{i}_2(t) = g_2\hat{v}_{g,rms}(t) + j_2\hat{v}_{control}(t) - \frac{\hat{v}(t)}{r_2} \tag{18.98}$$

where

$$g_2 = \left.\frac{df\left(v_{g,rms}, V, V_{control}\right)}{dv_{g,rms}}\right|_{v_{g,rms}=V_{g,rms}} = \frac{2}{R_e(V_{control})}\frac{V_{g,rms}}{V} \tag{18.99}$$

$$\left(-\frac{1}{r_2}\right) = \left.\frac{df\left(V_{g,rms}, \left\langle v\right\rangle_{T_{2L}}, V_{control}\right)}{d\left\langle v\right\rangle_{T_{2L}}}\right|_{\left\langle v\right\rangle_{T_{2L}}=V} = -\frac{I_2}{V} \tag{18.100}$$

$$j_2 = \left.\frac{df\left(V_{g,rms}, V, v_{control}\right)}{dv_{control}}\right|_{v_{control}=V_{control}} = -\frac{V_{g,rms}^2}{VR_e^2(V_{control})}\left.\frac{dR_e(v_{control})}{dv_{control}}\right|_{v_{control}=V_{control}} \tag{18.101}$$

A small-signal equivalent circuit based on Eq. (18.98) is given in Fig. 18.29(d). Expressions for the parameters g_2, j_2, and r_2 for several controllers are listed in Table 18.1. This model is valid for the conditions of Eq. (18.96), with the additional assumption that the output voltage ripple is sufficiently small. Figure 18.29(d) is useful only for determining the various ac transfer functions; no information regarding dc conditions can be inferred. The ac resistance r_2 is derived from the slope of the average value of the power source output characteristic, evaluated at the quiescent operating point. The other coefficients, j_2 and g_2, are also derived from the slopes of the same characteristic, taken with respect to $v_{control}(t)$ and $v_{g,rms}$ and evaluated at the quiescent operating point. The resistance R is the incremental resistance of the load, evaluated at the quiescent operating point. In the boost converter with hysteretic control, the transistor on-time ton replaces $v_{control}$ as the control input; likewise, the transistor duty cycle d is taken as the

Table 18.1 Small-signal model parameters for several types of rectifier control schemes

Controller type	g_2	j_2	r_2
Average current control with feedforward, Fig. 18.14	0	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
Current-programmed control, Fig. 18.16	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
Nonlinear-carrier charge control of boost rectifier, Fig. 18.21	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{2P_{av}}$
Boost with critical conduction mode control, Fig. 18.20	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
DCM buck-boost, flyback, SEPIC, or Ćuk converters	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{2P_{av}}{VD}$	$\frac{V^2}{P_{av}}$

control input to the DCM buck-boost, flyback, SEPIC, and Ćuk converters. Harmonics are ignored for the current-programmed and NLC controllers; the expressions given in Table 18.1 assume that the converter operates in CCM with negligible harmonics.

The control-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{control}(s)} = j_2 R \| r_2 \frac{1}{1 + sC R \| r_2} \tag{18.102}$$

The line-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{g,rms}(s)} = g_2 R \| r_2 \frac{1}{1 + sC R \| r_2} \tag{18.103}$$

Thus, the small-signal transfer functions of the high quality rectifier contain a single pole, ascribable to the output filter capacitor operating in conjunction with the incremental load resistance R and r_2, the effective output resistance of the power source. Although this model is based on the ideal rectifier, its form is similar to that of the dc–dc DCM buck-boost converter ac model of Chapter 11. This is natural, because the DCM buck-boost converter is itself a natural loss-free resistor. The major difference is that the rms value of the ac input voltage must be used, and that the second harmonic components of r_2, j_2, and g_2 must additionally be removed via averaging. Nonetheless, the equivalent circuit and ac transfer functions are of similar form.

When the rectifier drives a regulated dc–dc converter as in Fig. 18.25, then the dc–dc converter presents a constant power load to the rectifier, as illustrated in Fig. 18.26. In equilibrium, the rectifier and dc–dc converter operate with the same average power P_{av} and the same dc voltage V. The incremental resistance R of the constant power load is negative, and is given by

$$R = -\frac{V^2}{P_{av}} \tag{18.104}$$

which is equal in magnitude but opposite in polarity to the rectifier incremental output resistance r_2, for all controllers except the NLC controller. The parallel combination $r_2 \| R$ then tends to an open circuit, and the control-to-output and line-to-output transfer functions become

$$\frac{\hat{v}(s)}{\hat{v}_{control}(s)} = \frac{j_2}{sC} \tag{18.105}$$

and

$$\frac{\hat{v}(s)}{\hat{v}_{g,rms}(s)} = \frac{g_2}{sC} \tag{18.106}$$

In the case of the NLC controller, the parallel combination $r_2 \| R$ becomes equal to $r_2/2$, and Eqs. (18.102) and (18.103) continue to apply.

18.5 RMS VALUES OF RECTIFIER WAVEFORMS

To correctly specify the power stage elements of a near-ideal rectifier, it is necessary to compute the root-mean-square values of their currents. A typical waveform such as the transistor current of the boost converter (Fig. 18.31) is pulse-width modulated, with both the duty cycle and the peak amplitude varying with the ac input voltage. When the switching frequency is much larger than the ac line frequency, then the rms value can be well-approximated as a double integral. The square of the current is integrated first to find its average over a switching period, and the result is then integrated to find the average over the ac line period.

Computation of the rms and average values of the waveforms of a PWM rectifier can be quite tedious, and this can impede the effective design of the power stage components. In this section, several approximations are developed, which allow relatively simple analytical expressions to be written for the rms and average values of the power stage currents, and which allow comparison of converter approaches [14,41]. The transistor current in the boost rectifier is found to be quite low.

The rms value of the transistor current is defined as

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} i_Q^2(t)\,dt} \tag{18.107}$$

where T_{ac} is the period of the ac line waveform. The integral can be expressed as a sum of integrals over all of the switching periods contained in one ac line period:

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} T_s \sum_{n=1}^{T_{ac}/T_s} \left(\frac{1}{T_s} \int_{(n-1)T_s}^{nT_s} i_Q^2(t)\,dt \right)} \tag{18.108}$$

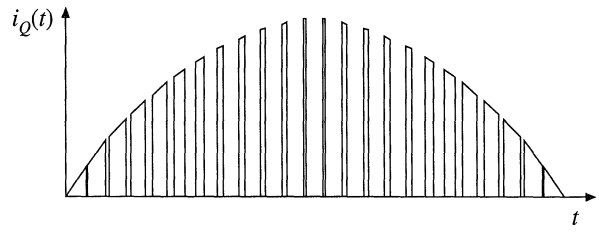

Fig. 18.31 Modulated transistor current waveform, boost rectifier.

where T_s is the switching period. The quantity inside the parentheses is the value of i_Q^2 averaged over the n^{th} switching period. The summation can be approximated by an integral in the case when T_s is much less than T_{ac}. This approximation corresponds to taking the limit as T_s tends to zero, as follows:

$$\begin{aligned} I_{Qrms} &\approx \sqrt{\frac{1}{T_{ac}} \lim_{T_s \to 0} \left[T_s \sum_{n=1}^{T_{ac}/T_s} \left(\frac{1}{T_s} \int_{(n-1)T_s}^{nT_s} i_Q^2(\tau) d\tau \right) \right]} \\ &= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{1}{T_s} \int_t^{t+T_s} i_Q^2(\tau) d\tau dt} \\ &= \sqrt{\left\langle \left\langle i_Q^2(t) \right\rangle_{T_s} \right\rangle_{T_{ac}}} \end{aligned} \tag{18.109}$$

So $i_Q^2(t)$ is first averaged over one switching period. The result is then averaged over the ac line period, and the square root is taken of the result.

18.5.1 Boost Rectifier Example

For the boost rectifier, the transistor current $i_Q(t)$ is equal to the input current when the transistor conducts, and is zero when the transistor is off. Therefore, the average of $i_Q^2(t)$ over one switching period is

$$\begin{aligned} \left\langle i_Q^2 \right\rangle_{T_s} &= \frac{1}{T_s} \int_t^{t+T_s} i_Q^2(t) dt \\ &= d(t) i_{ac}^2(t) \end{aligned} \tag{18.110}$$

If the input voltage is given by

$$v_{ac}(t) = V_M \left| \sin \omega t \right| \tag{18.111}$$

then the input current will be

$$i_{ac}(t) = \frac{V_M}{R_e} \left| \sin \omega t \right| \tag{18.112}$$

where R_e is the emulated resistance. With a constant output voltage V, the transistor duty cycle must obey the relationship

$$\frac{V}{v_{ac}(t)} = \frac{1}{1 - d(t)} \tag{18.113}$$

This assumes that the converter dynamics are fast compared to the ac line frequency. Substitution of Eq. (18.111) into (18.113) and solution for $d(t)$ yields

$$d(t) = 1 - \frac{V_M}{V} \left| \sin \omega t \right| \tag{18.114}$$

Substitution of Eqs. (18.112) and (18.114) into Eq. (18.110) yields the following expression

$$\left\langle i_Q^2 \right\rangle_{T_s} = \frac{V_M^2}{R_e^2}\left(1 - \frac{V_M}{V}\left|\sin \omega t\right|\right)\sin^2(\omega t) \tag{18.115}$$

One can now plug this expression into Eq. (18.109):

$$\begin{aligned} I_{Qrms} &= \sqrt{\frac{1}{T_{ac}}\int_0^{T_{ac}} \left\langle i_Q^2 \right\rangle_{T_s} dt} \\ &= \sqrt{\frac{1}{T_{ac}}\int_0^{T_{ac}} \frac{V_M^2}{R_e^2}\left(1 - \frac{V_M}{V}\left|\sin \omega t\right|\right)\sin^2(\omega t)\, dt} \end{aligned} \tag{18.116}$$

which can be further simplified to

$$I_{Qrms} = \sqrt{\frac{2}{T_{ac}}\frac{V_M^2}{R_e^2}\int_0^{T_{ac}/2}\left(\sin^2(\omega t) - \frac{V_M}{V}\sin^3(\omega t)\right)dt} \tag{18.117}$$

This involves integration of powers of $\sin(\omega t)$ over a complete half-cycle. The integral can be evaluated with the help of the following formula:

$$\frac{1}{\pi}\int_0^{\pi} sin^n(\theta)d\theta = \begin{cases} \frac{2}{\pi}\dfrac{2\cdot 4\cdot 6\cdots(n-1)}{1\cdot 3\cdot 5\cdots n} & \text{if } n \text{ is odd} \\ \dfrac{1\cdot 3\cdot 5\cdots(n-1)}{2\cdot 4\cdot 6\cdots n} & \text{if } n \text{ is even} \end{cases} \tag{18.118}$$

This type of integral commonly arises in rms calculations involving PWM rectifiers. The values of the integral for several choices of n are listed in Table 18.2. Evaluation of the integral in Eq. (18.117) using Eq. (18.118) leads to the following result:

$$I_{Qrms} = \frac{V_M}{\sqrt{2}R_e}\sqrt{1 - \frac{8}{3\pi}\frac{V_M}{V}} = I_{ac\,rms}\sqrt{1 - \frac{8}{3\pi}\frac{V_M}{V}} \tag{18.119}$$

It can be seen that the rms transistor current is minimized by choosing the output voltage V to be as small as possible. The best that can be done is to choose $V = V_M$, which leads to

$$I_{Qrms} = 0.39 I_{ac\,rms} \tag{18.120}$$

Larger values of V lead to a larger rms transistor current.

A similar analysis for the rms diode current leads to the following expression

$$I_{Drms} = I_{ac\,rms}\sqrt{\frac{8}{3\pi}\frac{V_M}{V}} \tag{18.121}$$

The choice $V = V_M$ maximizes the rms diode current, with the result

Table 18.2 Solution of the integral of Eq. (18.118), for several values of n

n	$\frac{1}{\pi}\int_0^{\pi} \sin^n(\theta)d\theta$
1	$\frac{2}{\pi}$
2	$\frac{1}{2}$
3	$\frac{4}{3\pi}$
4	$\frac{3}{8}$
5	$\frac{16}{15\pi}$
6	$\frac{15}{48}$

$$I_{Drms} = 0.92 I_{ac\,rms} \tag{18.122}$$

Larger values of V lead to smaller rms diode current.

Average currents can be computed in a similar way. The results are

$$\begin{aligned} I_{Qav} &= I_{ac\,rms} \frac{2\sqrt{2}}{\pi} \left(1 - \frac{\pi}{8} \frac{V_M}{V}\right) \\ I_{Dav} &= I_{ac\,rms} \frac{V_M}{2\sqrt{2}\,V} \end{aligned} \tag{18.123}$$

Expressions for rms, average, and peak currents of the power stage components of the continuous conduction mode boost converter are summarized in Table 18.3. Expressions are also tabulated for flyback and SEPIC topologies, operating in the continuous conduction mode. In the case of the flyback converter, an L_1–C_1 input filter is also included. In all cases, the effects of switching ripple are neglected.

18.5.2 Comparison of Single-Phase Rectifier Topologies

When isolation is not a rectifier requirement, and when it is acceptable that the dc output voltage be marginally larger than the peak ac input voltage, then the boost converter is a very effective approach. For example, consider the design of a 1 kW rectifier operating from the 240 Vrms input line voltage. If the converter efficiency and power factor are both approximately unity, then the rms input current is I_{rms} = (1000 W)/(240 V) = 4.2 A. The dc output voltage is chosen to be 380 V, or slightly larger than the peak ac input voltage. By use of Eq. (18.119), the rms transistor current is found to be 2 A. This is quite a low value—less than half of the rms input current, which demonstrates how effectively the converter utilizes the power switch. The rms diode current is 3.6 A, and the transistor and diode blocking voltages are 380 V. With a 120 A ac input voltage, the transistor and diode rms currents increase to 6.6 A and 5.1 A, respectively.

The only real drawback of the boost converter is its inability to limit inrush currents. When the dc output voltage is less than the instantaneous input voltage, the control circuit of the boost rectifier loses control of the inductor current waveform. A very large inrush current occurs when the dc output capacitor is initially charged. Additional circuitry must be employed to limit the magnitude of this current.

Buck-boost, SEPIC, and Ćuk topologies can be used to solve the inrush current problem. Since these converters have a $d/(1 - d)$ conversion ratio, their waveforms can be controlled when the output voltage is any positive value. But the price paid for this capability is increased component stresses. For the same 1 kW rectifier with 240 Vrms ac input and 380 V output, the transistor rms current and peak voltage of the nonisolated SEPIC are 5.5 A and 719 V. The rms diode current is 4.85 A. The semiconductor voltage stresses can be reduced by reducing the output voltage, at the expense of increased rms currents. With a 120 V ac input voltage, the transistor and diode rms currents increase to 9.8 A and 6.1 A, respectively.

Isolation can also be obtained in the SEPIC and other topologies, as discussed in Chapter 6. The turns ratio of the isolation transformer can also be used to reduce the primary-side currents when the dc output voltage is low. But the transformer winding rms currents are higher than those of a dc–dc converter, because of the pulsating (twice-line-frequency) power flow. For the 1 kW, 240 V ac input SEPIC example, with a 42 V 23.8 A dc load, and a 4:1 transformer turns ratio, the rms transformer currents are 5.5 A (primary) and 36.4 A (secondary). The rms transistor current is 6.9 A. At 120 V ac input voltage,

Table 18.3 Summary of rectifier current stresses for several converter topologies

	rms	Average	Peak
CCM boost			
Transistor	$I_{ac\,rms}\sqrt{1-\frac{8}{3\pi}\frac{V_M}{V}}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}\left(1-\frac{\pi}{8}\frac{V_M}{V}\right)$	$I_{ac\,rms}\sqrt{2}$
Diode	$I_{dc}\sqrt{\frac{16}{3\pi}\frac{V}{V_M}}$	I_{dc}	$2I_{dc}\frac{V}{V_M}$
Inductor	$I_{ac\,rms}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}$
CCM flyback, with n:1 isolation transformer and input filter			
Transistor, xfmr primary	$I_{ac\,rms}\sqrt{1+\frac{8}{3\pi}\frac{V_M}{nV}}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}\left(1+\frac{V_M}{nV}\right)$
L_1	$I_{ac\,rms}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}$
C_1	$I_{ac\,rms}\sqrt{\frac{8}{3\pi}\frac{V_M}{nV}}$	0	$I_{ac\,rms}\sqrt{2}\max\left(1,\frac{V_M}{nV}\right)$
Diode, xfmr secondary	$I_{dc}\sqrt{\frac{3}{2}+\frac{16}{3\pi}\frac{nV}{V_M}}$	I_{dc}	$2I_{dc}\left(1+\frac{nV}{V_M}\right)$
CCM SEPIC, nonisolated			
Transistor	$I_{ac\,rms}\sqrt{1+\frac{8}{3\pi}\frac{V_M}{V}}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}\left(1+\frac{V_M}{V}\right)$
L_1	$I_{ac\,rms}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}$
C_1	$I_{ac\,rms}\sqrt{\frac{8}{3\pi}\frac{V_M}{V}}$	0	$I_{ac\,rms}\sqrt{2}\max\left(1,\frac{V_M}{V}\right)$
L_2	$I_{ac\,rms}\frac{V_M}{V}\frac{\sqrt{3}}{2}$	$\frac{I_{ac\,rms}}{\sqrt{2}}\frac{V_M}{V}$	$I_{ac\,rms}\frac{V_M}{V}\sqrt{2}$
Diode	$I_{dc}\sqrt{\frac{3}{2}+\frac{16}{3\pi}\frac{V}{V_M}}$	I_{dc}	$2I_{dc}\left(1+\frac{V}{V_M}\right)$
CCM SEPIC, with n:1 isolation transformer			
Transistor	$I_{ac\,rms}\sqrt{1+\frac{8}{3\pi}\frac{V_M}{nV}}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}\left(1+\frac{V_M}{nV}\right)$
L_1	$I_{ac\,rms}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}$
C_1, xfmr primary	$I_{ac\,rms}\sqrt{\frac{8}{3\pi}\frac{V_M}{nV}}$	0	$I_{ac\,rms}\sqrt{2}\max\left(1,\frac{V_M}{nV}\right)$
Diode, xfmr secondary	$I_{dc}\sqrt{\frac{3}{2}+\frac{16}{3\pi}\frac{nV}{V_M}}$	I_{dc}	$2I_{dc}\left(1+\frac{nV}{V_M}\right)$

with, in all cases, $\frac{I_{acrms}}{I_{dc}}=\sqrt{2}\frac{V}{V_M}$, ac input voltage = $V_M\sin(\omega t)$, dc output voltage = V.

these currents increase to 7.7 A, 42.5 A, and 11.4 A, respectively.

18.6 MODELING LOSSES AND EFFICIENCY IN CCM HIGH-QUALITY RECTIFIERS

As in the case of dc–dc converters, we would like to model the converter loss elements so that we can correctly specify the power stage components. The equivalent circuit approach used in the dc–dc case can be generalized to include ac–dc low harmonic rectifiers, although the resulting equations are more complicated because of the low-frequency ac modulation of the waveforms.

A dc–dc boost converter and its steady-state equivalent circuit are illustrated in Fig. 18.32. When the converter operates in equilibrium, the model of Fig. 18.32(b) can be solved to determine the converter losses and efficiency. In the ac–dc case, the input voltage $v_g(t)$ is a rectified sinusoid, and the controller varies the duty cycle $d(t)$ to cause $i_g(t)$ to follow $v_g(t)$ according to

$$i_g(t) = \frac{v_g(t)}{R_e} \tag{18.124}$$

The emulated resistance R_e is chosen by the controller such that the desired dc output voltage is obtained. Ac variations in $d(t)$, $v_g(t)$, and several other system waveforms are not small, and hence the small-signal approximation employed in Chapters 7 to 12 is not justified. We can continue to model the low-frequency components of the converter via averaging, but the resulting equivalent circuits are, in general, time-varying and nonlinear.

For the purposes of determining the rectifier efficiency, it is assumed that (1) the inductor is sufficiently small, such that it has negligible influence on the ac-line-frequency components of the system waveforms, and (2) the capacitor is large, so that the output voltage $v(t)$ is essentially equal to its equilibrium dc value, with negligible low- or high-frequency ac variations. So in the ac–dc case, the model becomes as shown in Fig. 18.33. Low-frequency components ($\ll f_s$) of the controller waveforms are sketched in Fig. 18.34.

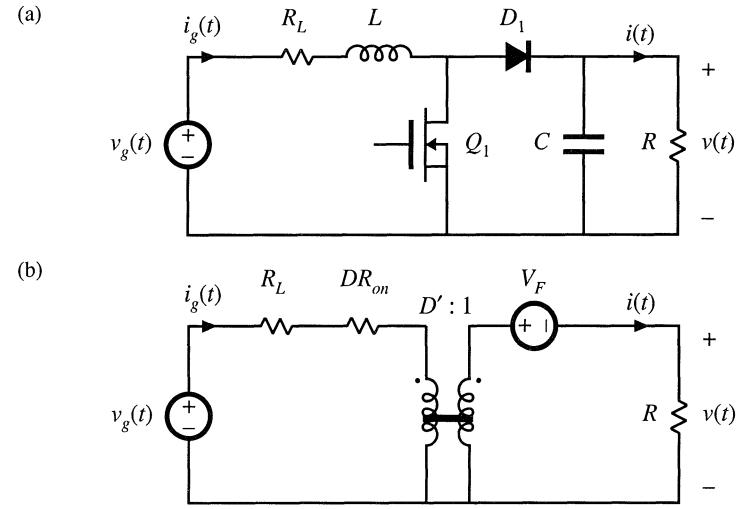

Fig. 18.32 Dc–dc boost converter, (a), and a steady-state equivalent circuit, (b), which models the inductor resistance R_L, MOSFET on-resistance R_{on}, and diode forward voltage drop V_F.

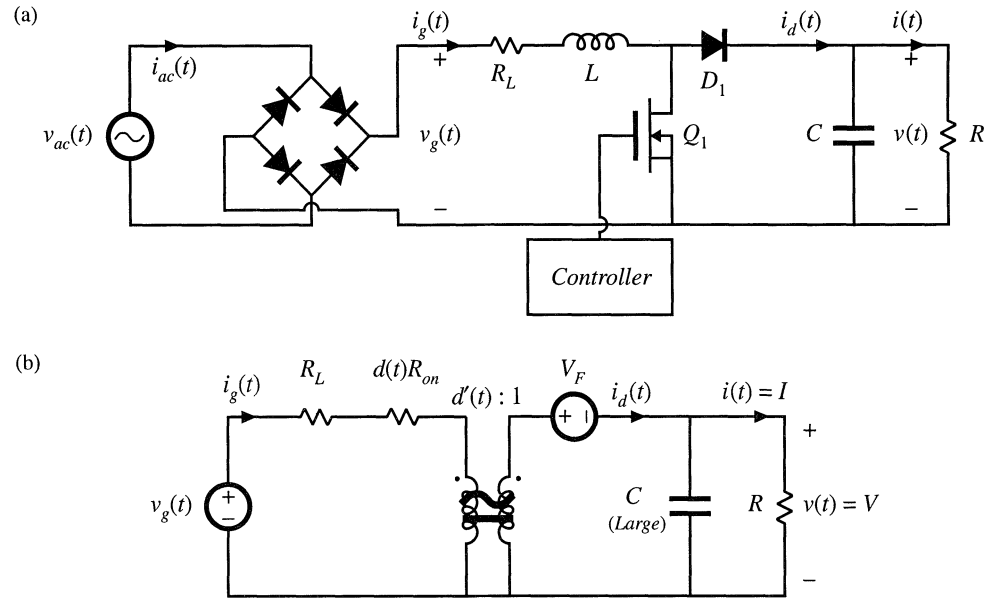

Fig. 18.33 Ac–dc boost rectifier, (a), and a low-frequency equivalent circuit, (b), that models converter losses and efficiency.

To find the rectifier waveforms, losses, and efficiency, we must solve the circuit of Fig. 18.33(b), under the conditions that the controller varies the duty cycle $d(t)$ such that Eq. (18.124) is satisfied. This leads to time-varying circuit elements $d(t)R_{on}$ and the $d'(t) : 1$ transformer. The solution that follows involves the following steps: (1) solve for the $d(t)$ waveform; (2) average $i_d(t)$ to find its dc component, equal to the load current I; and (3) find other quantities of interest such as the rectifier efficiency.

The simplified boost converter circuit model of Fig. 18.35, in which only the MOSFET conduction loss is accounted for, is solved here. However, the results can be generalized directly to the circuit of Fig. 18.33(b); doing so is left as a homework problem. A similar procedure can also be followed to derive expressions for the losses and efficiencies of other rectifier topologies.

18.6.1 Expression for Controller Duty Cycle $d(t)$

The controller varies the duty cycle $d(t)$ such that Eq. (18.124) is satisfied. By solving the input-side loop of Fig. 18.35, we obtain

$$i_g(t)d(t)R_{on} = v_g(t) - d'(t)v \tag{18.125}$$

Substitute Eq. (18.124) into (18.125) to eliminate $i_g(t)$:

$$\frac{v_g(t)}{R_e}\, d(t)R_{on} = v_g(t) - d'(t)v \tag{18.126}$$

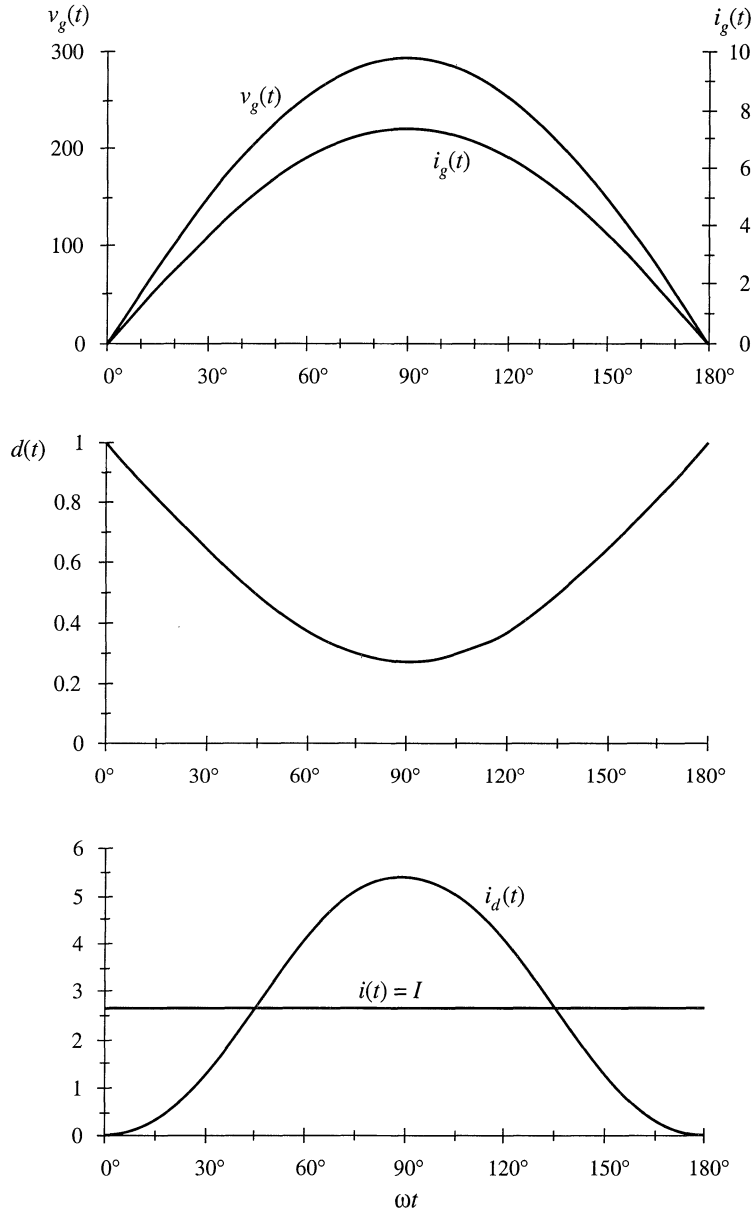

Fig. 18.34 Typical low-frequency components of the boost rectifier waveforms.

with
$$v_g(t) = V_M \left| \sin \omega t \right| \tag{18.127}$$

We can now solve for the duty cycle $d(t)$. The result is

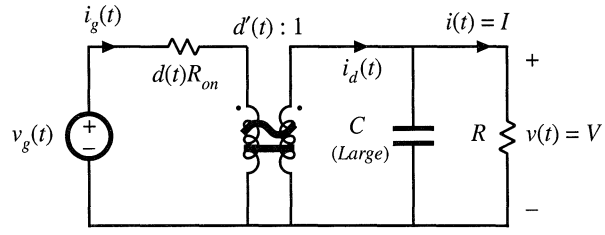

Fig. 18.35 Simplified boost power stage low-frequency equivalent circuit, in which only the MOSFET on-resistance is modeled.

$$d(t) = \frac{v - v_g(t)}{v - v_g(t)\dfrac{R_{on}}{R_e}} \tag{18.128}$$

This expression neglects the converter dynamics, an assumption that is justified when these dynamics are sufficiently faster than the ac line voltage variation. The expression also neglects operation in the discontinuous conduction mode near the zero-crossing of the ac line voltage waveform. This is justified when the rectifier operates in the continuous conduction mode for most of the ac line cycle, because the power loss near the zero-crossing is negligible.

18.6.2 Expression for the DC Load Current

By charge balance on output capacitor C, the dc load current I is equal to the dc component of the diode current i_d:

$$I = \langle i_d \rangle_{T_{ac}} \tag{18.129}$$

Solution of Fig. 18.35 for $i_d(t)$ yields

$$i_d(t) = d'(t) i_g(t) = d'(t) \frac{v_g(t)}{R_e} \tag{18.130}$$

From Eq. (18.128), $d'(t) = 1 - d(t)$ is given by

$$d'(t) = \frac{v_g(t)\left(1 - \dfrac{R_{on}}{R_e}\right)}{v - v_g(t)\dfrac{R_{on}}{R_e}} \tag{18.131}$$

so

$$i_d(t) = \frac{v_g^2(t)}{R_e} \frac{\left(1 - \dfrac{R_{on}}{R_e}\right)}{v - v_g(t)\dfrac{R_{on}}{R_e}} \tag{18.132}$$

Now substitute $v_g(t) = V_M \sin \omega t$, and integrate to find $\langle i_d(t) \rangle_{T_{ac}}$:

$$I = \langle i_d \rangle_{T_{ac}} = \frac{2}{T_{ac}} \int_0^{T_{ac}/2} \left(\frac{V_M^2}{R_e} \right) \frac{\left(1 - \frac{R_{on}}{R_e}\right) \sin^2(\omega t)}{\left(v - \frac{V_M R_{on}}{R_e} \sin(\omega t)\right)} dt \tag{18.133}$$

Again, $T_{ac} = 2\pi/\omega$ is the ac line period. Equation (18.133) can be rewritten as

$$I = \frac{2}{T_{ac}} \frac{V_M^2}{V R_e} \left(1 - \frac{R_{on}}{R_e}\right) \int_0^{T_{ac}/2} \frac{\sin^2(\omega t)}{1 - a \sin(\omega t)} dt \tag{18.134}$$

where

$$a = \left(\frac{V_M}{V}\right)\left(\frac{R_{on}}{R_e}\right) \tag{18.135}$$

By waveform symmetry, we need only integrate from 0 to $T_{ac}/4$. Also, make the substitution $\theta = \omega t$:

$$I = \frac{V_M^2}{V R_e} \left(1 - \frac{R_{on}}{R_e}\right) \frac{2}{\pi} \int_0^{\pi/2} \frac{\sin^2(\theta)}{1 - a \sin(\theta)} d\theta \tag{18.136}$$

Evaluation of this integral is tedious. It arises in not only the boost rectifier, but in a number of other high-quality rectifier topologies as well. The derivation is not given here, but involves the substitution $z = \tan(\theta/2)$, performing a partial fraction expansion of the resulting rational function of z, and integration of the results. The solution is:

$$\frac{4}{\pi} \int_0^{\pi/2} \frac{\sin^2(\theta)}{1 - a \sin(\theta)} d\theta = F(a) = \frac{2}{a^2 \pi} \left(-2a - \pi + \frac{4 \sin^{-1}(a) + 2 \cos^{-1}(a)}{\sqrt{1 - a^2}} \right) \tag{18.137}$$

This equation is somewhat complicated, but it is in closed form, and can easily be evaluated by computer spreadsheet. The quantity a, which is a measure of the loss resistance R_{on} relative to the emulated resistance R_e, is typically much smaller than 1. $F(a)$ is plotted in Fig. 18.36. The function $F(a)$ can be well-approximated as follows:

$$F(a) \approx 1 + 0.862a + 0.78a^2 \tag{18.138}$$

For $|a| \leq 0.15$, the $F(a)$ predicted by this approximate expression is within 0.1% of the exact value. If the a^2 term is omitted, then the accuracy drops to ± 2% over the same range of a. The rectifier efficiency η calculated in the next section depends directly on $F(a)$, and hence the accuracy of $F(a)$ coincides with the accuracy of η.

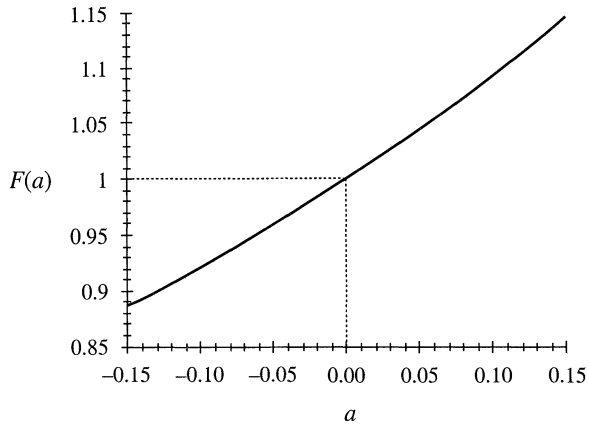

Fig. 18.36 Plot of the integral $F(a)$ vs. a.

18.6.3 Solution for Converter Efficiency η

Now that we have found the dc load current, we can calculate the converter efficiency η. The average input power is

$$P_{in} = \langle p_{in}(t) \rangle_{T_{ac}} = \frac{V_M^2}{2R_e} \tag{18.139}$$

The average load power is

$$P_{out} = VI = (V)\left(\frac{V_M^2}{VR_e}\left(1 - \frac{R_{on}}{R_e}\right)\frac{F(a)}{2}\right) \tag{18.140}$$

where

$$a = \left(\frac{V_M}{V}\right)\left(\frac{R_{on}}{R_e}\right) \tag{18.141}$$

Here, we have substituted Eq. (18.136) for I. The efficiency is therefore

$$\eta = \frac{P_{out}}{P_{in}} = \left(1 - \frac{R_{on}}{R_e}\right) F(a) \tag{18.142}$$

by substitution of Eqs. (18.139) and (18.140). If desired, the parabolic approximation for $F(a)$, Eq. (18.138), can be employed. This leads to

$$\eta \approx \left(1 - \frac{R_{on}}{R_e}\right)\left(1 + 0.862\,\frac{V_M}{V}\,\frac{R_{on}}{R_e} + 0.78\left(\frac{V_M}{V}\,\frac{R_{on}}{R_e}\right)^2\right) \tag{18.143}$$

Equations (18.142) and (18.143) show how the efficiency varies with MOSFET on resistance R_{on} and

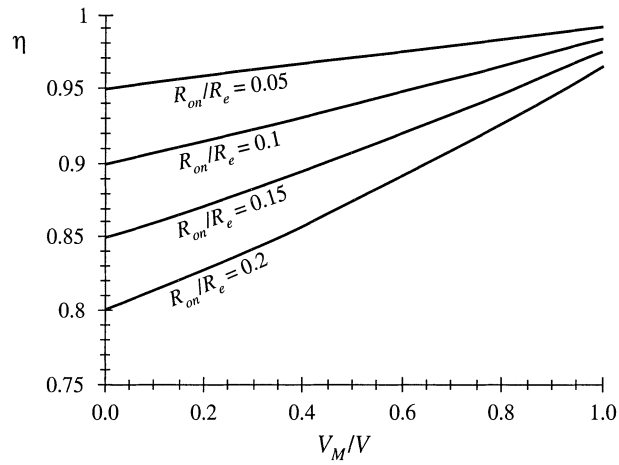

Fig. 18.37 Boost rectifier efficiency, Eq. (18.142), accounting for MOSFET on resistance.

with ac peak voltage V_M. Equation (18.142) is plotted in Fig. 18.37. It can be seen that high efficiency is obtained when the peak ac line voltage V_M is close to the dc output voltage V. Efficiencies in the range 90% to 95% can then be obtained, even with MOSFET on-resistances as high as $0.2R_e$. Of course, Fig. 18.37 is optimistic because it neglects sources of loss other than the MOSFET conduction loss.

18.6.4 Design Example

Let us utilize Fig. 18.37 to design for a given efficiency. Consider the following specifications:

Output voltage	390 V
Output power	500 W
rms input voltage	120 V
Efficiency	95%

Assume that losses other than the MOSFET conduction loss are negligible. The average input power is

$$P_{in} = \frac{P_{out}}{\eta} = \frac{500\ \text{W}}{0.95} = 526\ \text{W} \tag{18.144}$$

The emulated resistance is therefore

$$R_e = \frac{V_{g,rms}^2}{P_{in}} = \frac{(120\ \text{V})^2}{526\ \text{W}} = 27.4\ \Omega \tag{18.145}$$

Also,

$$\frac{V_M}{V} = \frac{120\sqrt{2}\ \text{V}}{390\ \text{V}} = 0.435 \tag{18.146}$$

From Fig. 18.37, or by evaluation of the exact equation (18.142), 95% efficiency with $V_M/V = 0.435$ occurs with $R_{on}/R_e \approx 0.077$. So we require a MOSFET having an on-resistance of

$$R_{on} \leq (0.077)\, R_e = (0.077)\,(27.4\ \Omega) = 2.11\ \Omega \tag{18.147}$$

Of course, other converter losses have not been accounted for, which will reduce the efficiency.

It is instructive to compare this result with that obtained using the expressions for rms current from Section 18.5. The rms transistor current of the ideal CCM boost converter is given by Eq. (18.119). The rms input current will be equal to $P_{in}/V_{g,rms}$ = (526 W)/(120 V) = 4.38 A. Hence, Eq. (18.119) predicts an rms transistor current of

$$\begin{aligned} I_{Qrms} &= I_{ac\ rms} \sqrt{1 - \frac{8}{3\pi}\frac{V_M}{V}} \\ &= (4.38\ \text{A}) \sqrt{1 - \frac{8}{3\pi}\frac{(120\ \text{V})\sqrt{2}}{(390\ \text{V})}} \\ &= 3.48\ \text{A} \end{aligned} \tag{18.148}$$

Hence, the MOSFET on-resistance should be chosen according to

$$R_{on} \leq \frac{P_{in} - P_{out}}{I_{Qrms}^2} = \frac{(526\ \text{W}) - (500\ \text{W})}{(4.38\ \text{A})^2} = 2.17\ \Omega \tag{18.149}$$

This calculation is approximate because Eq. (18.119) was derived using the waveforms of the ideal (lossless) converter. Nonetheless, it gives an answer that is very close to the more exact result of Eq. (18.147). We would expect this approximate approach to exhibit good accuracy in this example, because of the high 95% efficiency.

18.7 IDEAL THREE-PHASE RECTIFIERS

The single-phase ideal rectifier concepts of the previous sections can be generalized to cover ideal three-phase rectifiers. Figure 18.38(a) illustrates the properties of an ideal three-phase rectifier, which presents a balanced resistive load to the utility system. A three-phase converter system is controlled such that resistor emulation is obtained in each input phase. The rectifier three-phase input port can then be modeled by per-phase effective resistances R_e, as illustrated in Fig. 18.38(a). The instantaneous powers apparently consumed by these resistors are transferred to the rectifier dc output port. The rectifier output port can therefore be modeled by power sources equal to the instantaneous powers flowing into the effective resistances R_e. It is irrelevant whether the three power sources are connected in series or in parallel; in either event, they can be combined into a single source equal to the total three-phase instantaneous input power as illustrated in Fig. 18.38(b).

If the three-phase ac input voltages are

$$\begin{aligned} v_{an}(t) &= V_M \sin\left(\omega t\right) \\ v_{bn}(t) &= V_M \sin\left(\omega t - 120°\right) \\ v_{cn}(t) &= V_M \sin\left(\omega t - 240°\right) \end{aligned} \tag{18.150}$$

then the instantaneous powers flowing into the phase a, b, and c effective resistances R_e are

$$
\begin{aligned}
p_a(t) &= \frac{v_{an}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t\right)\right) \\
p_b(t) &= \frac{v_{bn}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t - 240°\right)\right) \\
p_c(t) &= \frac{v_{cn}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t - 120°\right)\right)
\end{aligned}
\tag{18.151}
$$

Each instantaneous phase power contains a dc term $V_M^2/(2R_e)$, and a second-harmonic term. The total instantaneous three-phase power is

$$
p_{tot}(t) = p_a(t) + p_b(t) + p_c(t) = \frac{3}{2}\frac{V_M^2}{R_e} \tag{18.152}
$$

This is the instantaneous power which flows out of the rectifier dc output port. Note that the second harmonic terms add to zero, such that the rectifier instantaneous output power is constant. This is a consequence of the fact that the instantaneous power flow in any balanced three-phase ac system is constant. So, unlike the single-phase case, the ideal three-phase rectifier can supply constant instantaneous power to a dc load, without the need for internal low-frequency energy storage.

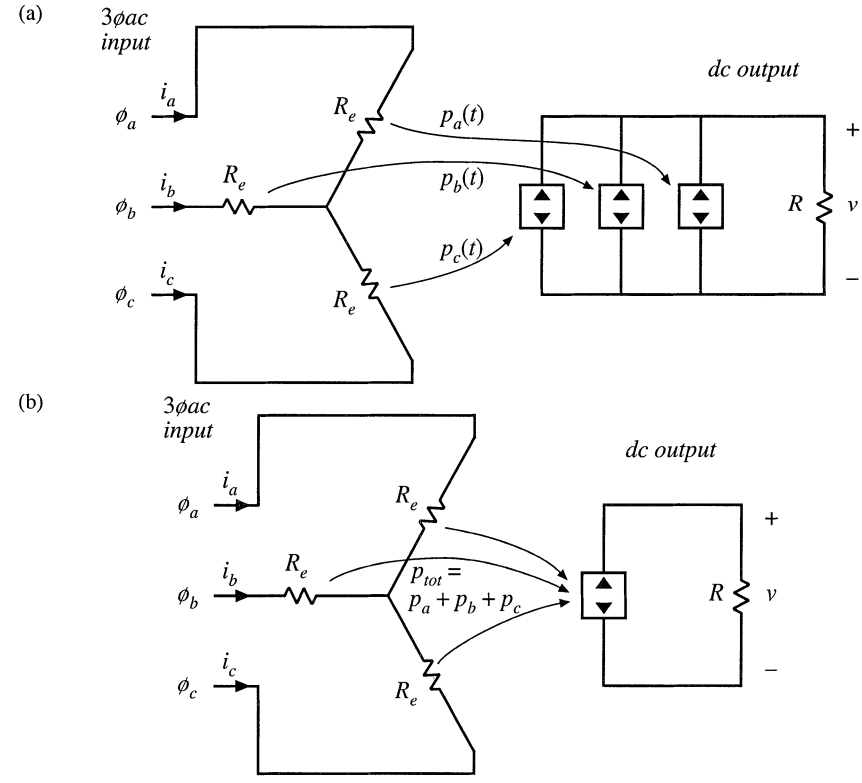

Fig. 18.38 Development of the ideal three-phase rectifier model: (a) three ideal single-phase rectifiers, (b) combination of the three power sources into an equivalent single power source.

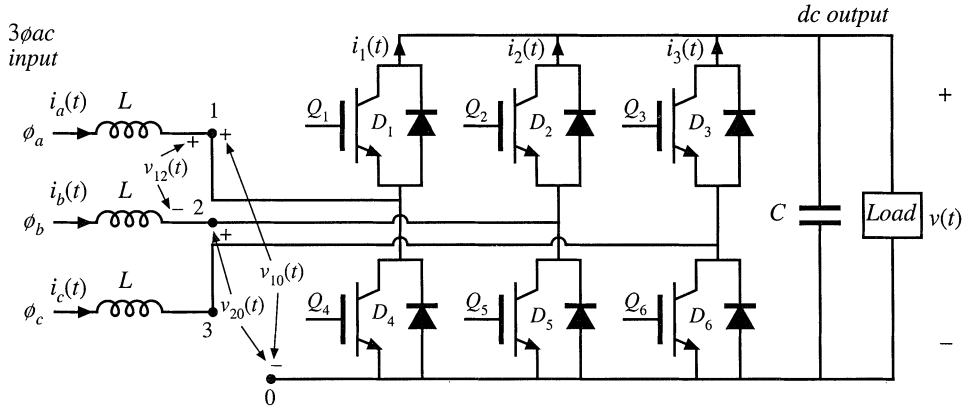

Fig. 18.39 Boost-type 3øac–dc PWM rectifier.

A variety of 3øac–dc PWM rectifiers are known; a few of the many references on this subject are listed in the references [42–59]. The most well-known topology is the three-phase ac–dc boost rectifier, illustrated in Fig. 18.39. This converter requires six SPST current-bidirectional two-quadrant switches. The inductors and capacitor filter the high-frequency switching harmonics, and have little influence on the low-frequency ac components of the waveforms. The switches of each phase are controlled to obtain input resistor emulation, either with a multiplying controller scheme similar to Fig. 18.5, or with some other approach. To obtain undistorted line current waveforms, the dc output voltage V must be greater than or equal to the peak line-to-line ac input voltage $V_{L,pk}$. In a typical realization, V is somewhat greater than $V_{L,pk}$. This converter resembles the voltage-source inverter, discussed briefly in Chapter 4, except that the converter is operated as a rectifier, and the converter input currents are controlled via high-frequency pulse-width modulation.

The three-phase boost rectifier of Fig. 18.39 has several attributes that make it the leading candidate for most 3øac–dc rectifier applications. The ac input currents are nonpulsating, and hence very little additional input EMI filtering is required. As in the case of the single-phase boost rectifier, the rms transistor currents and also the conduction losses of the three-phase boost rectifier are low relative to other 3øac–dc topologies such as the current-source inverter. The converter is capable of bidirectional power flow. A disadvantage is the requirement for six active devices: when compared with a dc–dc converter of similar ratings, the active semiconductor utilization (discussed in Chapter 6) is low. Also, since the rectifier has a boost characteristic, it is not suitable for direct replacement of traditional buck-type phase-controlled rectifiers.

The literature contains a wide variety of schemes for controlling the switches of a six-switch three-phase bridge network, which are applicable for control of the switches of Fig. 18.39. The basic operation of the converter can be most easily understood by assuming that the switches are controlled via simple sinusoidal pulse-width modulation. Transistor Q_1 is driven with duty cycle $d_1(t)$, while transistor Q_4 is driven by the complement of $d_1(t)$, or $d_1'(t) = 1 - d_1(t)$. Transistors Q_2 and Q_5 are driven with duty cycles $d_2(t)$ and $d_2'(t)$, respectively, and transistors Q_3 and Q_6 are driven with duty cycles $d_3(t)$ and $d_3'(t)$, respectively. The switch voltage waveforms of Fig. 18.40 are obtained. The average switch voltages are

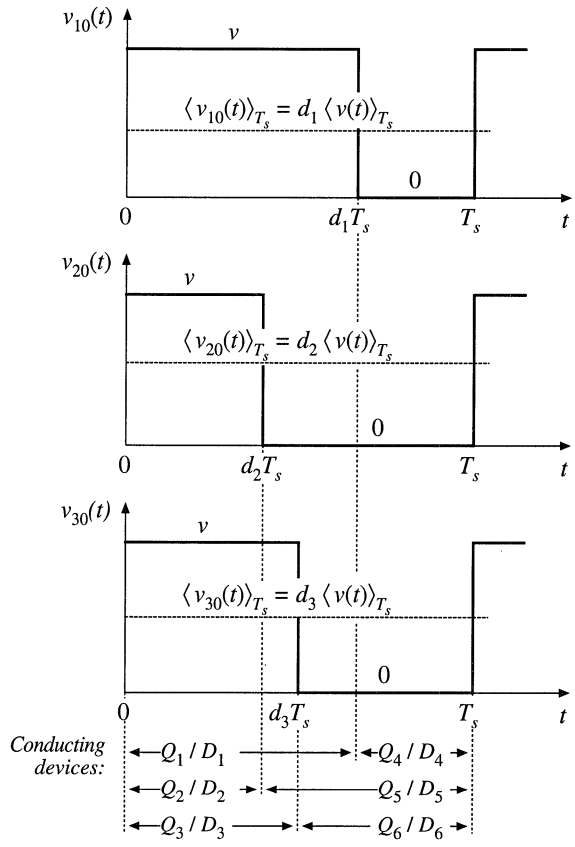

Fig. 18.40 Switch waveforms, 3øac–dc boost rectifier.

$$\begin{aligned}\langle v_{10}(t)\rangle_{T_s} &= d_1(t)\langle v(t)\rangle_{T_s}\\ \langle v_{20}(t)\rangle_{T_s} &= d_2(t)\langle v(t)\rangle_{T_s}\\ \langle v_{30}(t)\rangle_{T_s} &= d_3(t)\langle v(t)\rangle_{T_s}\end{aligned} \tag{18.153}$$

The averaged line-to-line switch voltages are therefore

$$\begin{aligned}\langle v_{12}(t)\rangle_{T_s} &= \langle v_{10}(t)\rangle_{T_s} - \langle v_{20}(t)\rangle_{T_s} = \big(d_1(t) - d_2(t)\big)\langle v(t)\rangle_{T_s}\\ \langle v_{23}(t)\rangle_{T_s} &= \langle v_{20}(t)\rangle_{T_s} - \langle v_{30}(t)\rangle_{T_s} = \big(d_2(t) - d_3(t)\big)\langle v(t)\rangle_{T_s}\\ \langle v_{31}(t)\rangle_{T_s} &= \langle v_{30}(t)\rangle_{T_s} - \langle v_{10}(t)\rangle_{T_s} = \big(d_3(t) - d_1(t)\big)\langle v(t)\rangle_{T_s}\end{aligned} \tag{18.154}$$

In a similar manner, the average switch currents can be shown to be

$$\begin{aligned}\langle i_1(t)\rangle_{T_s} &= d_1(t)\,\langle i_a(t)\rangle_{T_s}\\ \langle i_2(t)\rangle_{T_s} &= d_2(t)\,\langle i_b(t)\rangle_{T_s}\\ \langle i_3(t)\rangle_{T_s} &= d_3(t)\,\langle i_c(t)\rangle_{T_s}\end{aligned} \tag{18.155}$$

Equations (18.154) and (18.155) lead to the circuit-averaged model of Fig. 18.41.

With sinusoidal PWM, the duty cycles are varied sinusoidally in synchronism with the ac line, as follows:

$$\begin{aligned}d_1(t) &= D_0 + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi\right)\\ d_2(t) &= D_0 + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi - 120^\circ\right)\\ d_3(t) &= D_0 + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi - 240^\circ\right)\end{aligned} \tag{18.156}$$

where ω is the ac line frequency. Since each instantaneous duty cycle must lie in the interval [0,1], the dc bias D_0 is required. The factor D_m is called the *modulation index*; for $D_0 = 0.5$, D_m must be less than or equal to one. Other choices of D_0 further restrict D_m. In general, the modulation index can be defined as equal to the peak-to-peak amplitude of the fundamental component of the duty cycle variation.

If the switching frequency is sufficiently large, then filter inductors L can be small in value, such that they have negligible effect on the low-frequency ac waveforms. The averaged switch voltage $\langle v_{12}(t)\rangle_{T_s}$ then becomes approximately equal to the ac line-line voltage $v_{ab}(t)$:

$$\langle v_{12}(t)\rangle_{T_s} = \left(d_1(t) - d_2(t)\right)\langle v(t)\rangle_{T_s} \approx v_{ab}(t) \tag{18.157}$$

Substitution of Eqs. (18.150) and (18.156) leads to

$$\tfrac{1}{2} D_m \left[\sin\left(\omega t - \varphi\right) - \sin\left(\omega t - \varphi - 120^\circ\right)\right]\langle v(t)\rangle_{T_s} = V_M\left[\sin\left(\omega t\right) - \sin\left(\omega t - 120^\circ\right)\right] \tag{18.158}$$

For small L, the angle φ must tend to zero, and hence the sinusoidal terms in Eq. (18.158) cancel out. In steady-state, the dc output voltage is $\langle v(t)\rangle_{T_s} = V$. Equation (18.158) then becomes

$$\tfrac{1}{2} D_m V = V_M \tag{18.159}$$

Solution for the dc output voltage V leads to

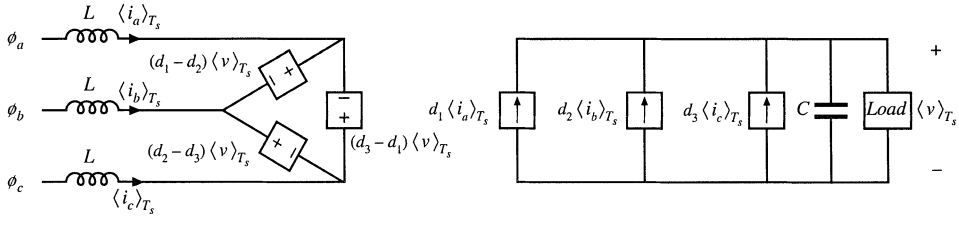

Fig. 18.41 Averaged model of the open-loop 3øac–dc boost rectifier.

$$V = \frac{2V_M}{D_m} \tag{18.160}$$

Equation (18.160) can be written in terms of the peak line-to-line voltage $V_{L,pk}$, as

$$V = \frac{2}{\sqrt{3}} \frac{V_{L,pk}}{D_m} = 1.15 \frac{V_{L,pk}}{D_m} \tag{18.161}$$

With $D_m \leq 1$, the dc output voltage V must be greater than or equal to 1.15 times the peak line-to-line ac input voltage. Thus, the rectifier has a boost characteristic.

The sinusoidal PWM approach of Eq. (18.156) is not the only way to vary the duty cycles to obtain sinusoidal ac voltages and currents. For example, triplen harmonics can be added to the duty cycle expressions of Eq. (18.156). These triplen harmonics cancel out in Eq. (18.154), such that the average inverter input voltages $\langle v_{12}(t)\rangle_{T_s}$, $\langle v_{23}(t)\rangle_{T_s}$, and $\langle v_{31}(t)\rangle_{T_s}$ contain only fundamental. Figure 18.42 illustrates duty cycle variations that lead to a dc output voltage V equal to $V_{L,pk}$. The effective modulation index in this case is 1.15. The ac-side voltages and currents are again undistorted. Further increases in the modulation index can be attained only by introduction of distortion in the ac-side voltages and currents. Of course, in practice the duty cycle modulations are usually generated by the feedback loops that control the input current waveforms to attain resistor emulation.

Three-phase ac-to-dc rectifiers having buck, buck-boost, or other characteristics, are possible, but find much less use than the boost topology. A 3øac-dc rectifier system can also be constructed simply using three separate single-phase rectifiers [34]; however, each single-phase rectifier must then contain transformer isolation, leading to substantially increased switch stress and loss. Other unconventional approaches to three-phase low-harmonic rectification have also been recently explored, such as the Vienna rectifier [56,59], single-switch approaches [49–55], and other circuits[44,45,46,57,58].

Yet another approach to solving the problem of three-phase rectifier harmonics is the *harmonic correction* scheme illustrated in Fig. 18.43. An active six-switch three-phase bridge removes the harmonics generated by a nonlinear three-phase load such as an uncontrolled rectifier. The harmonic corrector is controlled such that its ac line currents contain harmonics that are equal in magnitude but opposite in phase to the harmonics generated by the nonlinear load. No average power flows into the harmonic corrector. The total kVA rating of the harmonic corrector semiconductor devices depends on the magnitudes of the harmonics produced by the nonlinear load. If the THD generated by the load is not too large, then

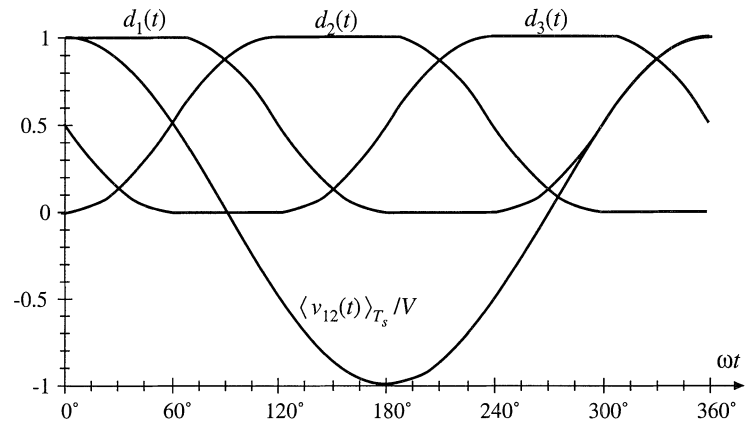

Fig. 18.42 A modulation strategy that leads to a dc output voltage equal to the peak input line-line voltage.

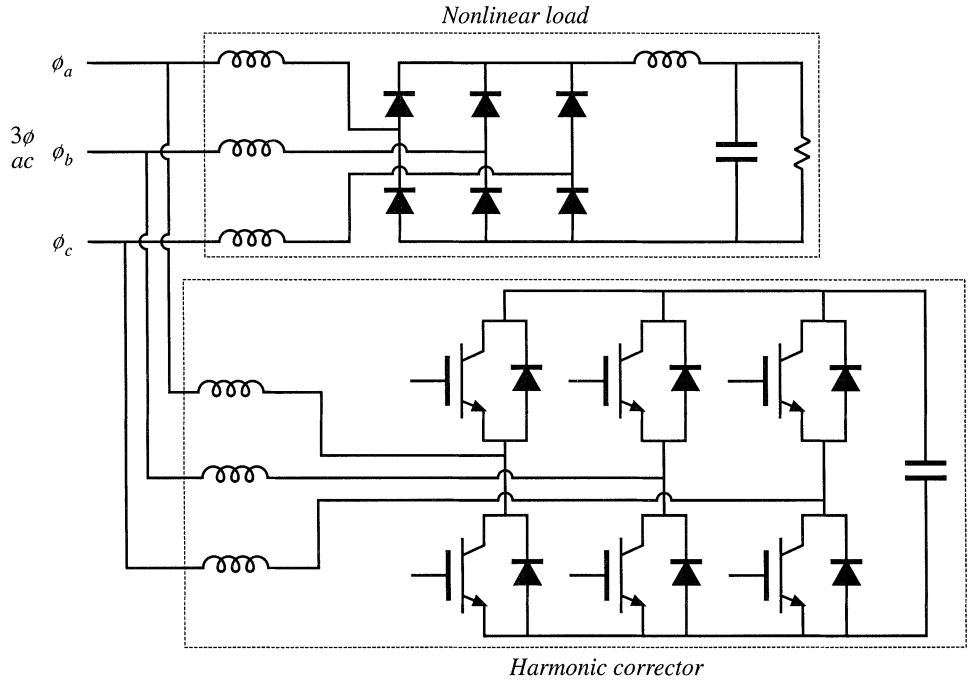

Fig. 18.43 A harmonic corrector, based on the 3øac–dc CCM boost converter of Fig. 18.39.

the harmonic corrector scheme requires less total active silicon than the CCM boost-type rectifier of Fig. 18.39. But if the uncontrolled rectifier contains small ac line inductances, such that it operates in the discontinuous conduction mode with large THD, then it is probably better to simply replace the uncontrolled rectifier with the CCM boost-type rectifier of Fig. 18.39.

18.8 SUMMARY OF KEY POINTS

1. The ideal rectifier presents an effective resistive load, the emulated resistance R_e, to the ac power system. The power apparently "consumed" by R_e is transferred to the dc output port. In a three-phase ideal rectifier, input resistor emulation is obtained in each phase. In both the single-phase and three-phase cases, the output port follows a power source characteristic, dependent on the instantaneous ac input power. Ideal rectifiers can perform the function of low-harmonic rectification, without need for low-frequency reactive elements.

2. The dc–dc boost converter, as well as other converters capable of increasing the voltage according to Eq. (18.12), can be adapted to the ideal rectifier application. A control system causes the input current to be proportional to the input voltage. The converter may operate in CCM, DCM, or in both modes. The mode boundary can be expressed as a function of R_e, $2L/T_s$, and the instantaneous voltage ratio $v_g(t)/V$. A well-designed average current controller leads to resistor emulation regardless of the operating mode; however, other schemes may lead to distorted current waveforms when the mode boundary is crossed.

3. In a single-phase system, the instantaneous ac input power is pulsating, while the dc load power is constant. Whenever the instantaneous input and output powers are not equal, the ideal rectifier system must

contain energy storage. A large capacitor is commonly employed; the voltage of this capacitor must be allowed to vary independently, as necessary to store and release energy. A slow feedback loop regulates the dc component of the capacitor voltage, to ensure that the average ac input power and dc load power are balanced.

4. RMS values of rectifiers waveforms can be computed by double integration. In the case of the boost converter, the rms transistor current can be as low as 39% of the rms ac input current, when the dc output voltage V is close in value to the peak ac input voltage V_M. Other converter topologies such as the buck-boost, SEPIC, and Ćuk converters exhibit significantly higher rms transistor currents but are capable of limiting the converter inrush current.

5. In the three-phase case, a boost-type rectifier based on the PWM voltage-source inverter also exhibits low rms transistor currents. This approach requires six active switching elements, and its dc output voltage must be greater than the peak input line-to-line voltage. Average current control can be used to obtain input resistor emulation. An equivalent circuit can be derived by averaging the switch waveforms. The converter operation can be understood by assuming that the switch duty cycles vary sinusoidally; expressions for the average converter waveforms can then be derived.

6. Converter losses and efficiency can be modeled using the steady-state equivalent circuit models of Chapter 3, with a time-varying duty cycle. The output current is averaged over one ac line period, to determine its dc component. The converter losses and efficiency can then be computed. This approach is approximate, in that (*i*) it assumes that the converter dynamics are much faster than the ac line frequency, and (*ii*) it neglects operation in the discontinuous conduction mode.

7. Average current control involves direct regulation of the low-frequency components of the rectifier input current to follow the input voltage. Feedforward can also be added, to cancel the influence of ac line voltage variations on the dc output voltage.

8. Current programmed control can also be adapted to attain input resistor emulation in rectifiers. The programmed current reference signal $i_c(t)$ is made proportional to the ac input voltage. The difference between $i_c(t)$ and the average inductor current leads to distortion, owing to the inductor current ripple and the need for a stabilizing artificial ramp. Several approaches are known for reducing the resulting harmonic distortion of the line current waveform.

9. Hysteretic control, particularly with 100% current ripple, has a simple controller implementation. The disadvantages are variable switching frequency, and increased peak currents.

10. Nonlinear carrier control also leads to a simple controller implementation, and has the advantage of CCM operation with small peak transistor current.

11. The outer low-bandwidth control system, which regulates the dc output voltage to balance the rectifier and load powers, can be modeled by averaging the rectifier waveforms over one-half of the ac line period T_{2L}. This causes the dc-side system equations to become time-invariant. A small-signal model is then obtained by perturbation and linearization.

12. The inner high-bandwidth control system, which regulates the ac input current waveform to attain resistor emulation, is in general highly nonlinear. However, in the case of the boost rectifier, a valid small-signal model can be derived. This approach is unsuccessful in the case of other converters; one must then resort to other approaches such as the quasi-static approximation or simulation.

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PROBLEMS

18.1 The boost converter of Fig. 18.5 is replaced by a buck-boost converter. Inductor energy storage has negligible influence on the low-frequency components of the converter waveforms. The average load power is P_{load}. The dc output voltage is V and the sinusoidal ac input voltage has peak amplitude V_M.

(a) Determine expressions for the duty cycle variations $d(t)$ and the inductor current variation $i(t)$, assuming that the converter operates in the continuous conduction mode.

(b) Derive the conditions for operation in the continuous conduction mode. Manipulate your result to show that the converter operates in CCM when R_e is less than $R_{e,crit}(L, T_s, v_g(t), V)$, and determine $R_{e,crit}$.

(c) For what values of R_e does the converter always operate in CCM? in DCM?

(d) The ac input voltage has rms amplitude in the range 108 V to 132 V. The maximum load power is 100 W, and the minimum load power is 10 W. The dc output voltage is 120 V. The switching frequency is 75 kHz. What value of L guarantees that the converter always operates in CCM? in DCM?

18.2 Derive expressions for the input characteristics of the buck-boost converter, similar to Eqs. (18.25) to (18.33). Sketch the converter input characteristics, and label the CCM–DCM boundary.

18.3 Derive expressions for the rms transistor and diode currents of rectifiers based on the single-phase CCM Ćuk topology. Express your results in forms similar to those of Table 18.3.

18.4 To obtain an isolated dc output, the boost converter in Fig. 18.5 is replaced by the full-bridge transformer-isolated CCM boost converter of Fig. 6.35. Derive an expression for the rms transistor current. Express your result as a function of $I_{ac\ rms}$, n, V, and V_M.

18.5 Comparison of CCM boost and isolated SEPIC topologies as universal-input single-phase rectifiers. You are given that the dc output voltage is $V = 400$ V, the load power is $P = 500$ W, and the rms input voltage varies between 90 and 270 V, such that the peak ac input voltage V_M varies between $V_{Mmin} = 127$ V and $V_{Mmax} = 382$ V. Define the transistor stress S as the product of the worst-case peak transistor voltage and the worst-case rms transistor current. It is desired to minimize S.

(a) Determine S for the boost converter in this application.

(b) Briefly discuss your result of part (a): if universal input operation was not required, and hence $V_M = 382$ V always, what S would result?

In the isolated SEPIC, the transformer turns ratio $n : 1$ can be chosen to optimize the design.

(c) Express S for the SEPIC as a function of n, V, P, V_{Mmin}, and V_{Mmax}.

(d) Choose n for the SEPIC such that S is minimized in this application. Compare with the results of parts (a) and (b).

18.6 In the boost-type dc–3øac rectifier of Fig. 18.39, the ac-side inductances L are not small: they exhibit line-frequency impedances that should not be ignored. The three-phase ac voltages are given by Eq. (18.150), and the duty cycles are modulated as in Eq. (18.156). The converter operates in the continuous conduction mode.

(a) Determine the magnitudes and phases of the line-to-neutral average voltages at the ac inputs to the switch network. Express your result in terms of D_m, V, and φ.

(b) Determine the real power P and reactive power Q drawn from the 3øac source. Express your results as functions of V_M, V, D_m, φ, and ωL.

(c) How must φ be chosen to obtain unity power factor?

18.7 In the boost-type dc–3øac rectifier of Fig. 18.39, the switch duty ratios are modulated as illustrated in Fig. 18.42. When the inductances L are sufficiently small, a dc output voltage V equal to the peak line-to-line ac input voltage can be obtained, with undistorted ac line currents. As illustrated in Fig. 18.42, $d_1(t)$ is equal to 1 for $0^\circ \le \omega t \le 60^\circ$, where $\omega t = 0^\circ$ when $\langle v_{12}(t) \rangle_{T_s} = V$.

(a) Derive expressions for $d_2(t)$ and $d_3(t)$, over the interval $0^\circ \le \omega t \le 60^\circ$.

(b) State how $d_1(t)$, $d_2(t)$, and $d_3(t)$ should vary over each 60° interval.

18.8 The buck-type 3øac–dc rectifier of Fig. 18.44 operates in the continuous conduction mode. Transistors Q_1 to Q_6 operate with duty cycles $d_1(t)$ to $d_6(t)$, respectively.

(a) Determine the constraints on switch operation. Which transistors must not conduct simultaneously? Which duty cycles must total unity?

(b) Average the 3ø bridge switch network, to determine expressions for the average ac-side switch currents $\langle i_a(t) \rangle_{T_s}$, $\langle i_b(t) \rangle_{T_s}$, and $\langle i_c(t) \rangle_{T_s}$.

(c) Show that the average dc-side switch voltage can be expressed as

$$\left\langle v_d(t) \right\rangle_{T_s} = \left(d_1(t) - d_4(t) \right) \left\langle v_{an}(t) \right\rangle_{T_s} + \left(d_2(t) - d_5(t) \right) \left\langle v_{bn}(t) \right\rangle_{T_s} + \left(d_3(t) - d_6(t) \right) \left\langle v_{cn}(t) \right\rangle_{T_s}$$

(d) The duty cycles are varied as follows:

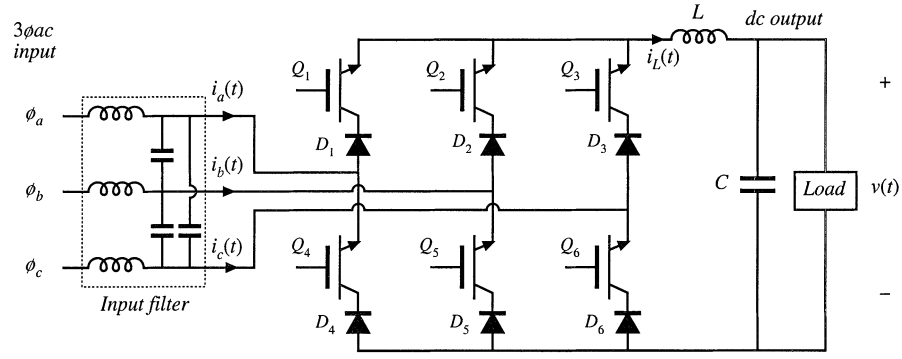

Fig. 18.44 Buck-type 3øac–dc rectifier, Problem 18.8.

$$d_1(t) = \tfrac{1}{3} + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi\right)$$
$$d_2(t) = \tfrac{1}{3} + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi - 120°\right)$$
$$d_3(t) = \tfrac{1}{3} + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi - 240°\right)$$
$$d_4(t) = \tfrac{1}{3} - \tfrac{1}{2} D_m \sin\left(\omega t - \varphi\right)$$
$$d_5(t) = \tfrac{1}{3} - \tfrac{1}{2} D_m \sin\left(\omega t - \varphi - 120°\right)$$
$$d_6(t) = \tfrac{1}{3} - \tfrac{1}{2} D_m \sin\left(\omega t - \varphi - 240°\right)$$

with the ac input voltages given by Eq. (18.150). The input filter has negligible effect of the low-frequency components of the converter waveforms. Determine the steady-state dc output voltage V, as a function of V_M, D_m, and φ.

(e) Determine the power factor. You may assume that the input filter completely removes the switching harmonics from the currents $i_a(t)$, $i_b(t)$, and $i_c(t)$. However, the input filter elements consume or supply negligible line-frequency reactive power.

18.9 In the three-phase DCM flyback rectifier of Fig. 18.45, the input filter has negligible effect on the low-frequency components of the input ac waveforms. The transistor operates with switching frequency f_s and duty cycle d. Flyback transformers T_1, T_2, and T_3 each have magnetizing inductance L referred to the primary, turns ratio n : 1, and have negligible leakage inductances.

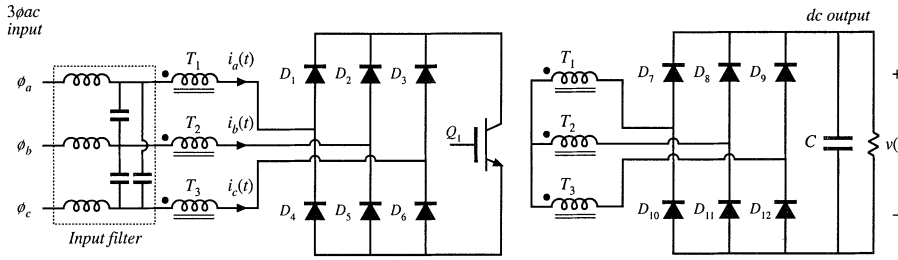

Fig. 18.45 Isolated 3øac–dc rectifier based on the flyback converter operating in discontinuous conduction mode: Problem 18.9.

(a) Determine expressions for the low-frequency components of the ac input and dc output currents.

(b) Derive an averaged equivalent circuit model for the converter, and give expressions for the ele-

ment values.

(c) Derive the conditions for operation in the discontinuous conduction mode.

18.10 Power stage design of a universal-input boost rectifier. The objective of this problem is to work out the power stage design of a low harmonic rectifier based on the boost converter. This converter is to be designed to operate anywhere in the world, and hence the input voltage may vary over the range 90 to 270 Vrms, 50 to 60 Hz. The converter produces a regulated 385 V dc output, at 1000 W. The switching frequency f_s is 100 kHz. You may assume that the controller operates perfectly, to produce an undistorted ac line current waveform and a well-regulated dc output voltage.

(a) Derive an expression for how the duty cycle $d(t)$ will vary over the ac line cycle. You may neglect converter dynamics and losses. Sketch $d(t)$ under conditions of maximum and minimum ac line voltage.

(b) Specify the inductor:

(i) Specify the value of L such that, at the peak of the sinusoidal input voltage, and under worst-case conditions, the inductor current ripple Δi_g is 20% of the instantaneous low frequency current $i_g(t)$.

(ii) Specify the worst-case values of the peak and rms inductor current, assuming 100% efficiency.

(c) Determine the worst-case rms currents of the MOSFET and diode, assuming 100% efficiency.

(d) Specify the value of C that leads to a worst-case low-frequency ($\ll f_s$) output voltage peak-peak ripple of 5 V.

(e) Given the following loss elements

Inductor winding resistance	0.1 Ω
MOSFET on-resistance	0.4 Ω
Diode forward voltage drop	1.5 V
Switching loss: model as	$i_g^2(t)(0.25\ \Omega)$

For a constant 1000 W load, and assuming that the controller operates perfectly as described above, find the rectifier efficiency

(i) at an ac input voltage of 90 V rms

(ii) at an ac input voltage of 270 V rms

18.11 The flyback converter shown in Fig. 18.46 operates in the continuous conduction mode. The MOSFET

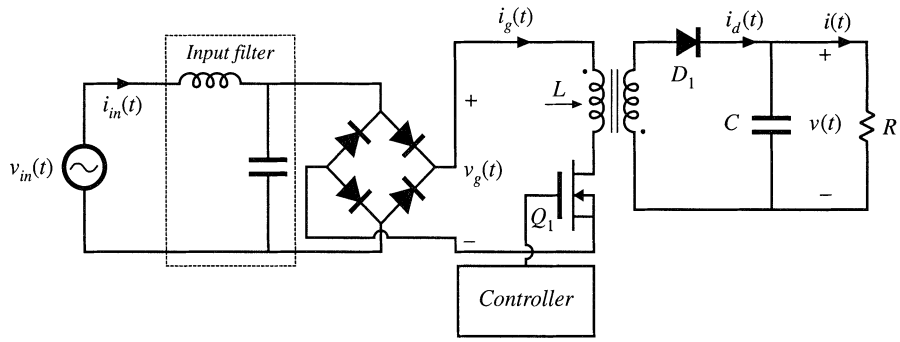

Fig. 18.46 Low-harmonic rectifier system based on the CCM flyback converter, Problem 18.11.

has on-resistance R_{on}, and diode D_1 has a constant forward voltage drop V_D. All other loss elements can

be neglected. The turns ratio of the flyback transformer is 1:1. The controller varies the duty cycle such that $\langle i_g(t) \rangle_{T_s}$ is equal to $v_g(t)/R_e$, where R_e is the emulated resistance. The input voltage is $v_{in}(t) = V_M \sin(\omega t)$. The input filter removes the switching harmonics from the input current $i_g(t)$, but has negligible effect on the low-frequency components of the converter waveforms.

(a) Derive an expression for the rectifier efficiency, in terms of V_M, V, V_D, R_{on}, and R_e.

(b) Given the following values, find the value of MOSFET on-resistance which leads to an efficiency of 96%.

rms input voltage	120 V
Dc output voltage	120 V
Diode D_1 forward voltage drop	1.5 V
Load power	200 W

18.12 Derive an expression for the emulated resistance $R_e(V_{g,rms}, R_s, k_v, v_{control})$ of the average-current-controlled boost rectifier with ac line voltage feedforward, Fig. 18.14.

18.13 Derive the CPM boost rectifier static input characteristics, Eq. (18.57).

18.14 The boost rectifier system of Fig. 18.47 employs average current control with ac line voltage feedforward.

The ac line frequency is 50 Hz. The rectifier drives a constant-power load of 500 W. The pulse-width modulator contains a ramp having a peak-to-peak amplitude of 3 V. There is no compensator in the inner wide-bandwidth average current control feedback loop. The average current sensing circuit has gain

$$\frac{v_a(s)}{i_g(s)} = \frac{R_s}{\left(1 + \frac{s}{\omega_0}\right)}$$

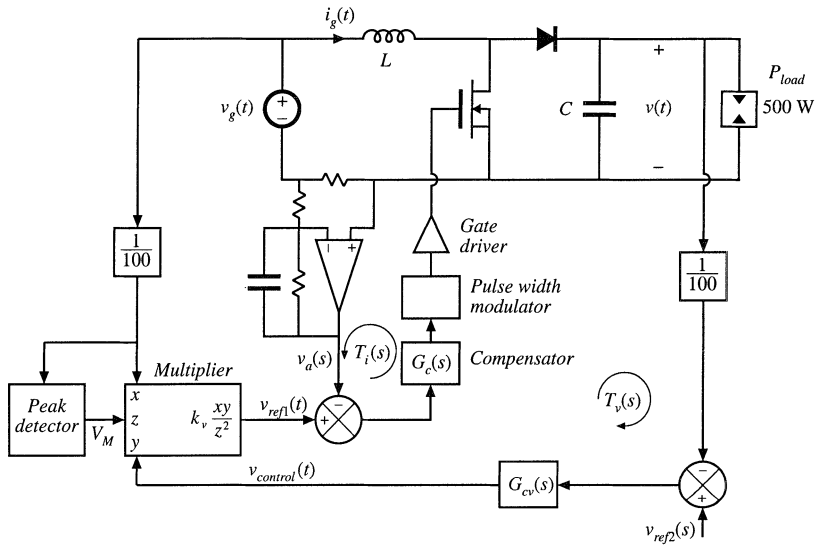

Fig. 18.47 Average current controlled boost rectifier with input voltage feedforward, Problem 18.14.

Other converter parameter values are

$$f_s = 100 \text{ kHz} \qquad L = 2.5 \text{ mH}$$

$$f_0 = \frac{\omega_0}{2\pi} = 10 \text{ kHz} \qquad R_s = 1\ \Omega$$

$$V = 385 \text{ V} \qquad V_{g,rms} = 230 \text{ V}$$

(a) Construct the magnitude and phase Bode diagrams of the loop gain $T_i(s)$ of the average-current-control loop. Label important features.

(b) Determine numerical values of the crossover frequency and phase margin of $T_i(s)$.

The outer low-bandwidth feedback loop has loop gain $T_v(s)$. The compensator of this loop has constant gain $G_{cv}(s) = 330$. The multiplier gain is $k_v = 2$. The capacitor value is $C = 680\ \mu$F. The reference voltage $v_{ref2}(t)$ is 3.85 V.

(c) Determine the peak magnitude of the output 100 Hz voltage ripple.

(d) Determine the quiescent control voltage $V_{control}$.

(e) Construct the magnitude and phase Bode diagrams of the loop gain $T_v(s)$ of the outer feedback loop. Label important features.

(f) Determine numerical values of the crossover frequency and phase margin of $T_v(s)$.

18.15 A critical conduction mode controller causes a boost rectifier to exhibit an ac input current waveform similar to Fig. 18.19(b). The ac input voltage is 120 Vrms at 60 Hz. The rectifier supplies 225 Vdc to a 120 W load. The boost converter inductance is $L = 600\ \mu$H.

(a) Determine the emulated resistance R_e.

(b) Write the numerical expression for the converter switching frequency f_s, as a function of t_{on} and the applied terminal voltages. Sketch f_s vs. time.

(c) What is the maximum switching frequency? What is the minimum switching frequency?

(d) Derive an analytical expression for the rms transistor current for this control method, as a function of the magnitude of the sinusoidal line current. Compare the rms transistor current of this approach with a CCM boost rectifier having negligible current switching ripple.