20
Soft Switching

In addition to the resonant circuits introduced in Chapter 19, there has been much interest in reducing the switching loss of the PWM converters of the previous chapters. Several of the more popular approaches to obtaining *soft switching* in buck, boost, and other converters, are discussed in this chapter.

Mechanisms that cause switching loss are discussed in Chapter 4, including diode reverse recovery, semiconductor output capacitances, and IGBT current tailing. Soft switching involves mitigation of one or more of these switching loss mechanisms in a PWM converter. The energy that would otherwise be lost is recovered, and is transferred to the converter source or load. The operation of a semiconductor device, during a given turn-on or turn-off switching transition, can be classified as hard-switched, zero-current switched, or zero-voltage switched. Operation of diodes and transistors with soft switching is examined in Section 20.1. In particular, it is preferable to operate diodes with zero-voltage switching at their turn-off transitions, and to operate MOSFETs with zero-voltage switching during their turn-on transitions. However, zero-voltage switching comes at the expense of increased conduction loss, and so the engineer must consider the effect of soft switching on the overall converter efficiency.

Resonant switch converters are a broad class of converters in which the PWM switch network of a conventional buck, boost, or other converter is replaced with a switch cell containing resonant elements. These resonant elements are positioned such that the semiconductor devices operate with zero-current or zero-voltage switching, and such that one or more of the switching loss mechanisms is reduced or eliminated. Other soft-switching approaches may employ resonant switching transitions, but otherwise exhibit the approximately rectangular waveforms of hard-switched converters. In any case, the resulting hybrid converter combines the properties of the resonant switching network and the parent hard-switched PWM converter.

Soft-switching converters can exhibit reduced switching loss, at the expense of increased conduction loss. Obtaining zero-voltage or zero-current switching requires that the resonant elements have large ripple; often, these elements are operated in a manner similar to the discontinuous conduction

R. W. Erickson et al., *Fundamentals of Power Electronics*

modes of the series or parallel resonant converters. As in other resonant schemes, the objectives of designing such a converter are: (1) to obtain smaller transformer and low-pass filter elements via increase of the switching frequency, and/or (2) to reduce the switching loss induced by component nonidealities such as diode stored charge, semiconductor device capacitances, and transformer leakage inductance and winding capacitance.

The resonant switch and soft-switching ideas are quite general, and can be applied to a variety of topologies and applications. A large number of resonant switch networks have been documented in the literature; a few basic approaches are listed here [1–24]. The basic zero-current-switching quasi-resonant switch network is analyzed in detail in Section 20.2. Expressions for the average components of the switch network terminal waveforms are found, leading to determination of the *switch conversion ratio* μ. The switch conversion ratio μ performs the role of the duty cycle d of CCM PWM switch networks. For example, the buck converter exhibits conversion ratio M equal to μ. Both half-wave and full-wave ringing of the tank network is considered; these lead to different switch conversion ratio functions μ. In general, given a PWM CCM converter having conversion ratio $M(d)$, we can replace the PWM switch network with a resonant switch network having switch conversion ratio μ. The resulting quasi-resonant converter will then have conversion ratio $M(\mu)$. So we can obtain soft-switching versions of all of the basic converters (buck, boost, buck-boost, forward, flyback, etc.), that exhibit zero-voltage or zero-current switching and other desirable properties.

In Section 20.3, the characteristics of several other resonant switch networks are listed: the zero-voltage-switching quasi-resonant switch network, the zero-current-switching and zero-voltage-switching quasi-square-wave networks, and the multiresonant switch network. One can obtain zero-voltage switching in all transistors and diodes using these networks.

Several related soft-switching approaches are now popular, which attain zero-voltage switching of the transistor or transistors in commonly-used converters. The zero-voltage transition approach finds application in full-bridge buck-derived converters. Active-clamp snubbers are often added to forward and flyback converters, to attain zero-voltage switching and to reset the transformer. These circuits lead to zero-voltage switching of the transistors, but (less-than-optimal) zero-current switching of the secondary-side diodes. Nonetheless, high efficiency can be achieved. An auxiliary resonant-commutated pole can achieve zero-voltage switching in voltage-source inverters. These converters are briefly discussed in Section 20.4.

20.1 SOFT-SWITCHING MECHANISMS OF SEMICONDUCTOR DEVICES

When loosely used, the terms "zero-current switching" and "zero-voltage switching" normally refer to one or more switching transitions of the transistor in a converter. However, to fully understand how a converter generates switching loss, one must closely examine the switching transitions of every semiconductor device. As described in Section 4.3, there are typically several mechanisms that are sources of significant switching loss. At the turn-off transition of a diode, its reverse-recovery process can induce loss in the transistor or other elements of the converter. The energy stored in the output capacitance of a MOSFET can be lost when the MOSFET turns on. IGBTs can lose significant energy during their turn-off transition, owing to the current-tailing phenomenon. The effects of zero-current switching and zero-voltage switching on each of these devices is discussed in detail below.

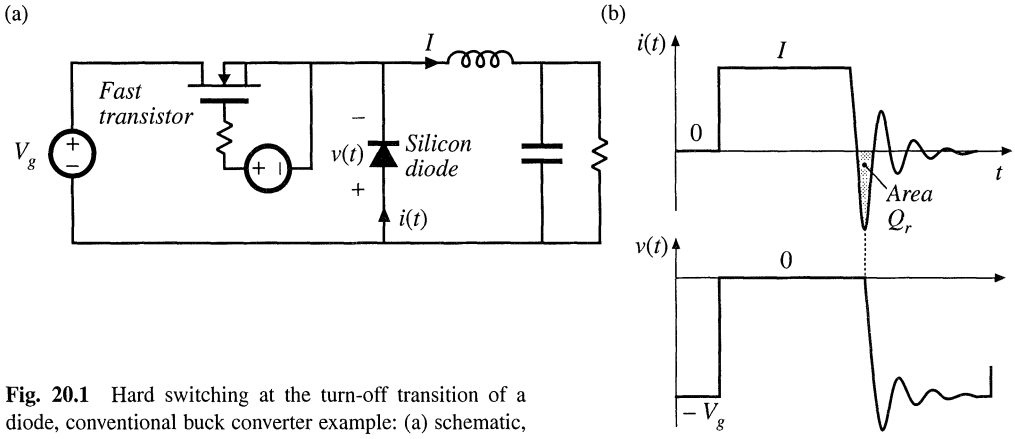

Fig. 20.1 Hard switching at the turn-off transition of a diode, conventional buck converter example: (a) schematic, (b) diode voltage and current waveforms.

20.1.1 Diode Switching

As discussed in Chapter 4, the reverse-recovery process usually leads to significant switching loss associated with the turn-off transition of diodes. This is often the largest single source of loss in a hard-switched converter. Normally, negligible loss is associated with the turn-on transition of power diodes. Three types of diode turn-off transition waveforms are commonly encountered in modern switching converters: hard switching, zero-current switching, and zero-voltage switching.

Figure 20.1 illustrates a conventional hard-switched PWM buck converter. The diode voltage and current waveforms $v(t)$ and $i(t)$ are also illustrated, with an exaggerated reverse recovery time. The output inductor current ripple is small. The diode turns off when the transistor is turned on; the reverse recovery process leads to a negative peak current of large amplitude. The diode must immediately support the full reverse voltage V_g, and hence both $v(t)$ and $i(t)$ must change with large slopes during reverse recovery. As described in Section 4.3.2, hard switching of the diode induces energy loss W_D in the transistor, given approximately by

$$W_D = V_g Q_r + t_r V_g I \tag{20.1}$$

where Q_r is the diode recovered charge and t_r is the reverse recovery time, both taken to be positive quantities. The recovered charge is relatively large because the slope di/dt is large during the turn-off transition. The resonant circuit formed by the diode output capacitance C_j and the diode package and other wiring inductances leads to ringing at the end of the reverse recovery time.

Figure 20.2 illustrates zero-current switching at the turn-off transition of a diode. The converter example is a quasi-resonant zero-voltage switching buck converter (see Section 20.3.1). The output inductor current ripple is again small. However, tank inductor L_r is now connected in series with the diode. The resulting diode current waveform $i(t)$ changes with a limited slope as shown. The diode reverse-recovery process commences when $i(t)$ passes through zero and becomes negative. The negative $i(t)$ actively removes stored charge from the diode; during this reverse recovery time, the diode remains forward-biased. When the stored charge is removed, then the diode voltage must rapidly change to $-V_g$. As described in Section 4.3.3, energy W_D is stored in inductor L_r at the end of the reverse recovery time, given by

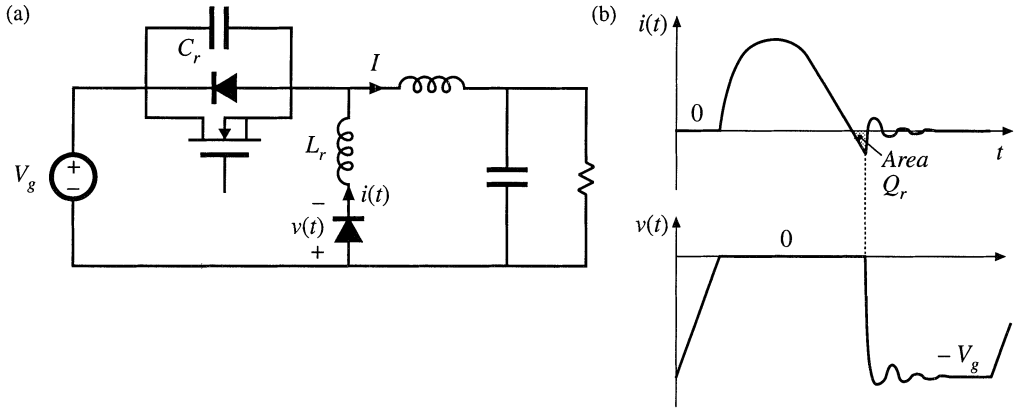

Fig. 20.2 Zero-current switching at the turn-off transition of a diode, ZVS quasi-resonant buck converter example: (a) converter schematic, (b) diode voltage and current waveforms.

$$W_D = V_g Q_r \tag{20.2}$$

The resonant circuit formed by L_r and the diode output capacitance C_j then cause this energy to be circulated between L_r and C_j. This energy is eventually dissipated by parasitic resistive elements in the circuit, and hence is lost. Since Eqs. (20.1) and (20.2) are similar in form, the switching losses induced by the reverse-recovery processes of diodes operating with hard switching and with zero-current switching are similar in magnitude. Zero-current switching may lead to somewhat lower loss because the reduced *di/dt* leads to less recovered charge Q_r. Zero-current switching of diodes also typically leads to increased peak inverse diode voltage during the ringing of L_r and C_j, because of the relatively large value of L_r.

When a diode operates with hard switching or zero-current switching, and when substantial inductance is present in series with the diode, then significant ringing is observed in the diode voltage waveform. A resonant circuit, comprised of the series inductance and the diode output capacitance, is excited by the diode reverse recovery process, and the resulting ringing voltage can be of large enough magnitude to lead to breakdown and failure of the diode. A common example is the diodes on the secondary side of a hard-switched transformer-isolated converter; the resonant circuit is then formed by the transformer leakage inductance and the diode output capacitance. Other examples are the circuits of Figs. 20.2 and 20.36, in which the series inductance is a discrete tank inductor.

A simple snubber circuit that is often used to protect the diode from excessive reverse voltage is

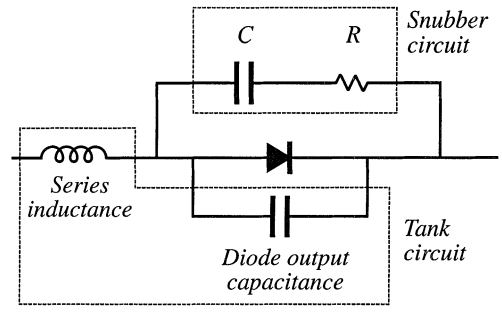

Fig. 20.3 A dissipative snubber circuit, for protection of a diode from excessive voltage caused by ringing.

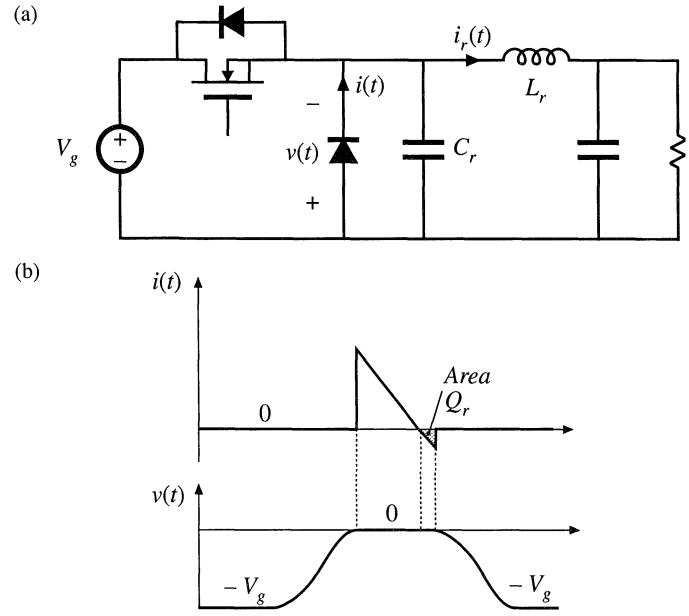

Fig. 20.4 Zero-voltage switching at the turn-off transition of a diode, ZVS quasi-squarewave buck converter example: (a) converter schematic, (b) diode current and voltage waveforms.

illustrated in Fig. 20.3. Resistor R damps the ringing of the resonant circuit. Capacitor C prevents the off-state voltage of the diode from causing excessive power loss in R. Nonetheless, the energy consumed by R per switching period is typically greater than Eqs. (20.1) or (20.2).

Figure 20.4 illustrates zero-voltage switching at the turn-off transition of a diode. The figure illustrates the example of a zero-voltage switching quasi-square wave buck converter, discussed in Section 20.3.3. The output inductor L_r of this converter assumes the role of the tank inductor, and exhibits large current ripple that causes the current $i_r(t)$ to reverse polarity. While the diode conducts, its current $i(t)$ is equal to $i_r(t)$. When $i_r(t)$ becomes negative, the diode continues to conduct until its stored charge Q_r has been removed. The diode then becomes reverse-biased, and $i_r(t)$ flows through capacitor C_r and the diode output capacitance C_j. The diode voltage and current both change with limited slope in this type of switching, and the loss induced by the diode reverse-recovery process is negligible because the waveforms are not significantly damped by parasitic resistances in the circuit, and because the peak currents during reverse recovery are relatively low. The diode stored charge and diode output capacitance both behave as an effective nonlinear capacitor that can be combined with (or replace) tank capacitor C_r. Snubber circuits such as Fig. 20.3 are not necessary when the diode operates with zero-voltage switching.

Thus, zero-voltage switching at the turn-off transition of a diode is the preferred approach, that leads to minimum switching loss. Zero-current switching at the turn-off transition can be problematic, because of the high peak inverse voltage induced across the diode by ringing.

20.1.2 MOSFET Switching

The switching loss mechanisms typically encountered by a MOSFET in a hard-switched converter are discussed in Chapter 4, and typical MOSFET voltage and current waveforms are illustrated in Fig. 20.5. The most significant components of switching loss in the MOSFET of this circuit are: (1) the loss

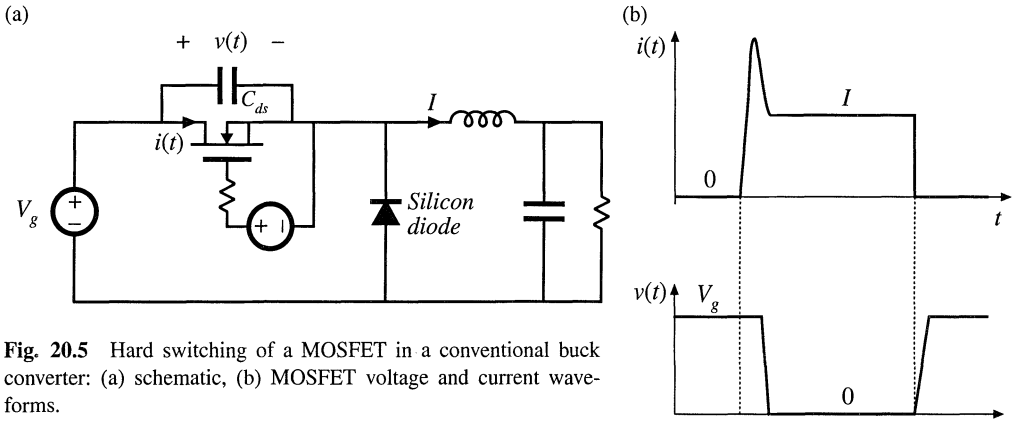

Fig. 20.5 Hard switching of a MOSFET in a conventional buck converter: (a) schematic, (b) MOSFET voltage and current waveforms.

induced by the diode reverse recovery process, and (2) the loss of the energy stored in the MOSFET output capacitance C_{ds}. Both loss mechanisms occur during the MOSFET turn-on process.

In the hard-switched circuit of Fig. 20.5, there is essentially no switching loss incurred during the MOSFET turn-off transition. This occurs because of the substantial output capacitance C_{ds} of the MOSFET. This capacitance holds the voltage $v(t)$ close to zero while the MOSFET turns off, so that the turn-off switching loss is very small. After the MOSFET has turned off, the output inductor current I flows through C_{ds}. The voltage $v(t)$ then increases until $v = V_g$ and the diode becomes forward biased.

However, when the MOSFET turns on, a high peak current flows through the MOSFET channel, induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode. This leads to substantial energy loss during the hard-switched turn-on transition of the MOSFET.

When a MOSFET (or other transistor) operates with hard switching, and when substantial inductance is present in series with the MOSFET, then significant ringing is observed in the MOSFET voltage waveform. A resonant circuit, composed of the MOSFET output capacitance and the series inductance, is excited when the MOSFET turns off, and the resulting ringing voltage can be of large enough magnitude to lead to breakdown and failure of the MOSFET. A common example is the MOS-

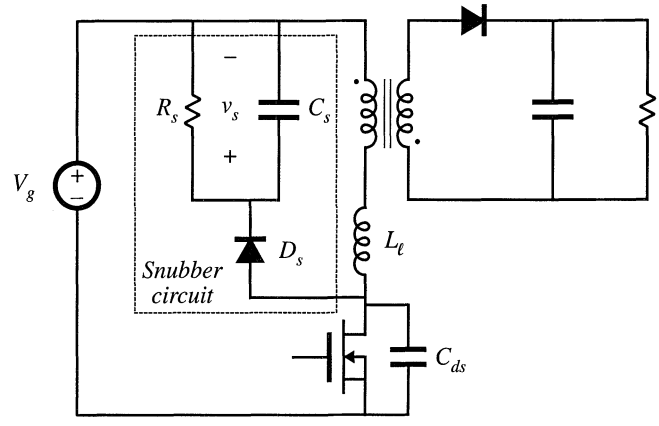

Fig. 20.6 Insertion of a dissipative voltage-clamped snubber circuit into a flyback converter. The MOSFET voltage is clamped to a peak value of $(V_g + v_s)$.

FET of the flyback converter, in which series inductance is introduced by the transformer leakage inductance. An R–C snubber circuit, similar to that used for the diode in Fig. 20.3, can be used to protect the MOSFET from damage caused by excessive applied voltage. Another common snubber circuit is illustrated in Fig. 20.6. When the MOSFET turns off, the current flowing in the transformer leakage inductance L_ℓ begins to flow into the MOSFET capacitance C_{ds}. These parasitic elements then ring, and the peak transistor voltage can significantly exceed the ideal value of $(D/D')V_g$.

One simple way to design the snubber circuit of Fig. 20.6 is to choose the capacitance C_s to be large, so that $v_s(t) \approx V_s$ contains negligible switching ripple. The resistance R_s is then chosen so that the power consumption of R_s at the desired voltage V_s is equal to the switching loss caused by L_ℓ:

$$\frac{V_s^2}{R_s} \approx \frac{1}{2} L i^2 f_s \tag{20.3}$$

The current i is equal to the current flowing in the transformer primary just before the MOSFET is turned off. This approximate expression is useful for obtaining a first estimate of how to choose R_s to obtain a given desired V_s.

Zero-current switching does not affect the switching loss that arises from the MOSFET output capacitance, and it may or may not influence the loss induced by diode reverse recovery. In consequence, zero-current switching is of little or no help in improving the efficiency of converters that employ MOSFETs.

Zero-voltage switching can prevent both diode reverse recovery and semiconductor output capacitances from inducing switching loss in MOSFETs. An example is illustrated in Fig. 20.7. This circuit is again a zero-voltage switching quasi-squarewave example, discussed in Section 20.3.3. The converter circuit naturally discharges the energy stored in C_{ds}, before the MOSFET is switched on. When the drain-to-source voltage $v(t)$ passes through zero, the MOSFET body diode becomes forward-biased. The MOSFET can then be turned on at zero voltage, without incurring turn-on switching loss. The MOSFET turn-on transition must be completed before the tank inductor current $i_r(t)$ becomes positive. The MOSFET turn-off transition is also lossless, and is similar to the hard-switched case discussed above.

Zero-voltage switching of a MOSFET also causes its body diode to operate with zero-voltage switching. This can eliminate the switching loss associated with reverse recovery of the slow body diode, and improve the reliability of circuits that forward-bias this diode.

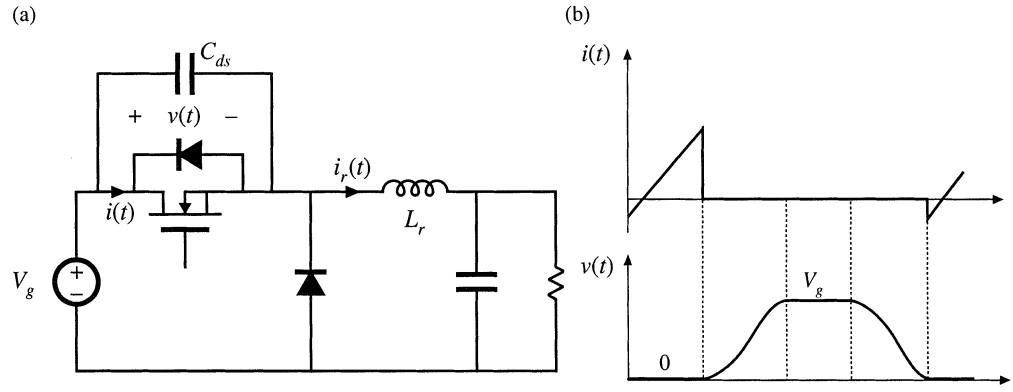

Fig. 20.7 Zero-voltage switching of a MOSFET, ZVS quasi-squarewave buck converter example. The MOSFET, its body diode, and its output capacitance C_{ds} are illustrated. (a) converter schematic, (b) MOSFET voltage and current waveforms.

Zero-voltage switching can also eliminate the overvoltage problems associated with transformer leakage inductances, removing the need for voltage-clamped snubber circuits such as in Fig. 20.6. An example is discussed in Section 20.4.2.

20.1.3 IGBT Switching

Like the MOSFET, the IGBT typically encounters substantial switching loss during its turn-on transition, induced by the reverse-recovery process of diodes within the converter. In addition, the IGBT exhibits significant switching loss during its turn-off transition, caused by the current tailing phenomenon (*see* Chapter 4).

Zero-voltage switching has been successfully applied to IGBT circuits—an example is the auxiliary resonant commutation circuit discussed in Section 20.4.3. This has the principal advantage of eliminating the switching loss caused by diode reverse recovery. Although zero-voltage switching can reduce the loss incurred during the turn-off transition, it is difficult to eliminate the substantial loss caused by current tailing.

20.2 THE ZERO-CURRENT SWITCHING QUASI-RESONANT SWITCH CELL

Figure 20.8(a) illustrates a generic buck converter, consisting of a switch cell cascaded by an L–C low-pass filter. When the switch cell is realized as in Fig. 20.8(b), then a conventional PWM buck converter is obtained. Figures 20.8(b) and (c) illustrate two other possible realizations of the switch cell: the half-wave and full-wave zero-current-switching quasi-resonant switches [1, 2]. In these switch cells, a resonant tank capacitor C_r is placed in parallel with diode D_2, while resonant tank capacitor L_r is placed in series with the active transistor element.

Both resonant switch cells require a two-quadrant SPST switch. In the half-wave switch cell of Fig. 20.8(c), diode D_1 is added in series with transistor Q_1. This causes the Q_1–D_1 SPST switch to turn off at the first zero crossing of the tank inductor current $i_1(t)$. In the full-wave switch cell of Fig. 20.8(d), antiparallel diode D_1 allows bidirectional flow of the tank inductor current $i_1(t)$. With this switch network, the Q_1–D_1 SPST switch is normally turned off at the second zero-crossing of the $i_1(t)$ waveform. In either switch cell, the L_r and C_r elements are relatively small in value, such that their resonant frequency f_0 is greater than the switching frequency f_s, where

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{\omega_0}{2\pi} \tag{20.4}$$

In the analysis which follows, it is assumed that the converter filter element values L and C have negligible switching ripple. Hence, the switch cell terminal waveforms $v_1(t)$ and $i_2(t)$ are well-approximated by their average values:

$$\begin{aligned} i_2(t) &\approx \langle i_2(t) \rangle_{T_s} \\ v_1(t) &\approx \langle v_1(t) \rangle_{T_s} \end{aligned} \tag{20.5}$$

with the average defined as in Eq. (7.3). In steady-state, we can further approximate $v_1(t)$ and $i_2(t)$ by their dc components V_1 and I_2:

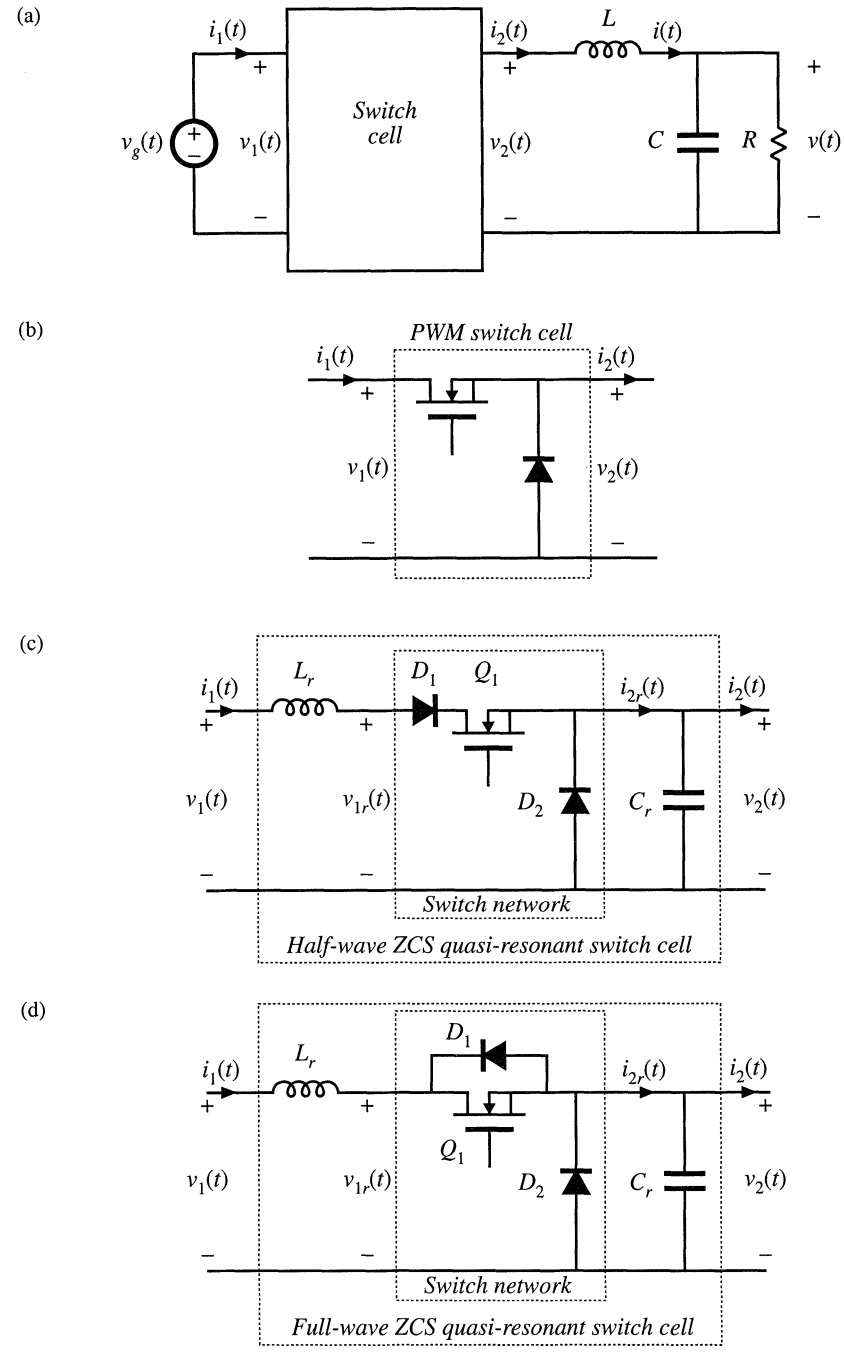

Fig. 20.8 Implementation of the switch cell in a buck converter: (a) buck converter, with arbitrary switch cell; (b) PWM switch cell; (c) half-wave ZCS quasi-resonant switch cell; (d) full-wave ZCS quasi-resonant switch cell.

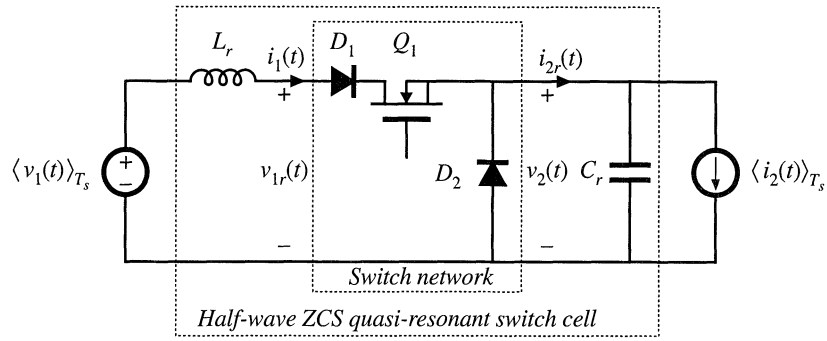

Fig. 20.9 The half-wave ZCS quasi-resonant switch cell, driven by the terminal quantities $\langle v_1(t)\rangle_{T_s}$ and $\langle i_2(t)\rangle_{T_s}$.

$$\begin{aligned} i_2(t) &\approx I_2 \\ v_1(t) &\approx V_1 \end{aligned} \tag{20.6}$$

Thus, the small-ripple approximation is employed for the converter filter elements, as usual.

To understand the operation of the half-wave ZCS quasi-resonant switch cell, we can solve the simplified circuit illustrated in Fig. 20.9. In accordance with the averaged switch modeling approach of Sections 7.4 and 11.1, it is desired to determine the average terminal waveforms $\langle v_2(t)\rangle_{T_s}$ and $\langle i_1(t)\rangle_{T_s}$, as functions of the applied quantities $\langle v_1(t)\rangle_{T_s}$ and $\langle i_2(t)\rangle_{T_s}$. The switch conversion ratio μ is then given by

$$\mu = \frac{\langle v_2(t)\rangle_{T_s}}{\langle v_{1r}(t)\rangle_{T_s}} = \frac{\langle i_1(t)\rangle_{T_s}}{\langle i_{2r}(t)\rangle_{T_s}} \tag{20.7}$$

In steady state, we can write

$$\mu = \frac{V_2}{V_1} = \frac{I_1}{I_2} \tag{20.8}$$

The steady-state analysis of this section employs Eq. (20.8) to determine μ.

20.2.1 Waveforms of the Half-Wave ZCS Quasi-Resonant Switch Cell

Typical waveforms of the half-wave cell of Fig. 20.9 are illustrated in Fig. 20.10. Each switching period consists of four subintervals as shown, having angular lengths α, β, δ, and ξ. The switching period begins when the controller turns on transistor Q_1. The initial values of the tank inductor current $i_1(t)$ and tank capacitor voltage $v_2(t)$ are zero. During subinterval 1, all three semiconductor devices conduct. Diode D_2 is forward-biased because $i_1(t)$ is less than I_2. In consequence, during subinterval 1 the switch cell reduces to the circuit of Fig. 20.11.

The slope of the inductor current is given by

$$\frac{di_1(t)}{dt} = \frac{V_1}{L_r} \tag{20.9}$$

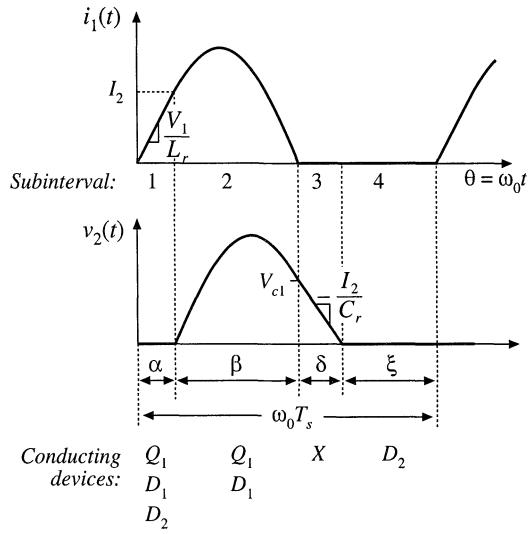

Fig. 20.10 Tank inductor current and capacitor voltage waveforms, for the half-wave ZCS quasi-resonant switch of Fig. 20.9.

with the initial condition $i_1(0) = 0$. The solution is

$$i_1(t) = \frac{V_1}{L_r} t = \omega_0 t \frac{V_1}{R_0} \tag{20.10}$$

where the tank characteristic impedance R_0 is defined as

$$R_0 = \sqrt{\frac{L_r}{C_r}} \tag{20.11}$$

It is convenient to express the waveforms in terms of the angle $\theta = \omega_0 t$, instead of time t. At the end of subinterval 1, $\omega_0 t = \alpha$. The subinterval ends when diode D_2 becomes reverse-biased. Since the diode D_2 current is equal to $I_2 - i_1(t)$, this occurs when $i_1(t) = I_2$. Hence, we can write

$$i_1(\alpha) = \alpha \frac{V_1}{R_0} = I_2 \tag{20.12}$$

Solution for α yields

$$\alpha = \frac{I_2 R_0}{V_1} \tag{20.13}$$

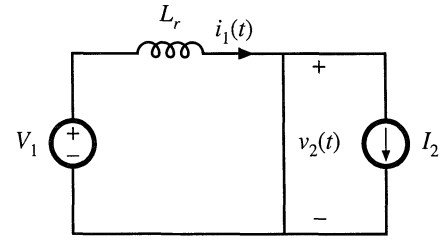

Fig. 20.11 Circuit of the switch network during subinterval 1.

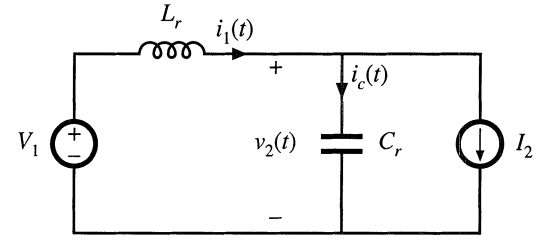

Fig. 20.12 Circuit of the switch network during subinterval 2.

During subinterval 2, transistor Q_1 and diode D_1 conduct, while diode D_2 is reverse-biased. The switch network then becomes the circuit illustrated in Fig. 20.12. The resonant L_r–C_r tank network is excited by the constant sources V_1 and I_2. The network equations are

$$\begin{aligned} L_r \frac{di_1(\omega_0 t)}{dt} &= V_1 - v_2(\omega_0 t) \\ C_r \frac{dv_2(\omega_0 t)}{dt} &= i_1(\omega_0 t) - I_2 \end{aligned} \tag{20.14}$$

with the initial conditions

$$\begin{aligned} v_2(\alpha) &= 0 \\ i_1(\alpha) &= I_2 \end{aligned} \tag{20.15}$$

The solution is

$$\begin{aligned} i_1(\omega_0 t) &= I_2 + \frac{V_1}{R_0} \sin(\omega_0 t - \alpha) \\ v_2(\omega_0 t) &= V_1 \left(1 - \cos(\omega_0 t - \alpha)\right) \end{aligned} \tag{20.16}$$

The tank inductor current rises to a peak value given by

$$I_{1pk} = I_2 + \frac{V_1}{R_0} \tag{20.17}$$

The subinterval ends at the first zero crossing of $i_1(t)$. If we denote the angular length of the subinterval as β, then we can write

$$i_1(\alpha + \beta) = I_2 + \frac{V_1}{R_0} \sin(\beta) = 0 \tag{20.18}$$

Solution for $\sin(\beta)$ yields

$$\sin(\beta) = -\frac{I_2 R_0}{V_1} \tag{20.19}$$

Care must be employed when solving Eq. (20.19) for the angle β. It can be observed from Fig. 20.10 that the angle β is greater than π. The correct branch of the arcsine function must be selected, as follows:

$$\beta = \pi + \sin^{-1}\left(\frac{I_2 R_0}{V_1}\right) \tag{20.20}$$

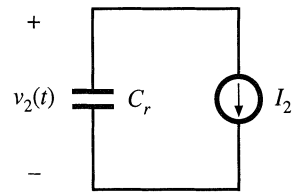

Fig. 20.13 Circuit of the switch network during subinterval 3.

where

$$-\frac{\pi}{2} < \sin^{-1}(x) \leq \frac{\pi}{2}$$

Note that the inequality

$$I_2 < \frac{V_1}{R_0} \tag{20.21}$$

must be satisfied; otherwise, there is no solution to Eq. (20.19). At excessive load currents, where Eq. (20.21) is not satisfied, the tank inductor current never reaches zero, and the transistor does not switch off at zero current.

The tank capacitor voltage at the end of subinterval 2 is found by evaluation of Eq. (20.16) at $\omega_0 t = (\alpha + \beta)$. The cos (β) term can be expressed as

$$\cos(\beta) = -\sqrt{1 - \sin^2(\beta)} = -\sqrt{1 - \left(\frac{I_2 R_0}{V_1}\right)^2} \tag{20.22}$$

Substitution of Eq. (20.22) into Eq. (20.16) leads to

$$v_2(\alpha + \beta) = V_{c1} = V_1\left(1 + \sqrt{1 - \left(\frac{I_2 R_0}{V_1}\right)^2}\right) \tag{20.23}$$

At the end of subinterval 2, diode D_1 becomes reverse-biased. Transistor Q_1 can then be switched off at zero current.

During subinterval 3, all semiconductor devices are off, and the switch cell reduces to the circuit of Fig. 20.13. The tank capacitor C_r is discharged by the filter inductor current I_2. Hence, the tank capacitor voltage v_2 decreases linearly to zero. The circuit equations are

$$\begin{aligned} C_r \frac{dv_2(\omega_0 t)}{dt} &= -I_2 \\ v_2(\alpha + \beta) &= V_{c1} \end{aligned} \tag{20.24}$$

The solution is

$$v_2(\omega_0 t) = V_{c1} - I_2 R_0\left(\omega_0 t - \alpha - \beta\right) \tag{20.25}$$

Subinterval 3 ends when the tank capacitor voltage reaches zero. Diode D_2 then becomes forward-biased. Hence, we can write

$$v_2(\alpha + \beta + \delta) = V_{c1} - I_2 R_0 \delta = 0 \tag{20.26}$$

where δ is the angular length of subinterval 3. Solution for δ yields

$$\delta = \frac{V_{c1}}{I_2 R_0} = \frac{V_1}{I_2 R_0}\left(1 - \sqrt{1 - \left(\frac{I_2 R_0}{V_1}\right)^2}\right) \tag{20.27}$$

Subinterval 4, of angular length ξ, is identical to the diode conduction subinterval of the conventional PWM switch network. Diode D_2 conducts the filter inductor current I_2, and the tank capacitor voltage v_2 is equal to zero. Transistor Q_1 is off, and the input current i_1 is equal to zero.

The angular length of the switching period is

$$\omega_0 T_s = \alpha + \beta + \delta + \xi = \frac{2\pi f_0}{f_s} = \frac{2\pi}{F} \tag{20.28}$$

where

$$F = \frac{f_s}{f_0} \tag{20.29}$$

Quasi-resonant switch networks are usually controlled by variation of the switching frequency f_s or, in normalized terms, by variation of F. Note that the interval lengths α, β, and δ are determined by the response of the tank network. Hence, control of the switching frequency is equivalent to control of the fourth subinterval length ξ. The subinterval length ξ must be positive, and hence, the minimum switching period is limited as follows:

$$\omega_0 T_s \geq \alpha + \beta + \delta \tag{20.30}$$

Substitution of Eqs. (20.13), (20.20), and (20.27) into Eq. (20.30) yields

$$\frac{2\pi}{F} \geq \frac{I_2 R_0}{V_1} + \pi + \sin^{-1}\left(\frac{I_2 R_0}{V_1}\right) + \frac{V_1}{I_2 R_0}\left(1 - \sqrt{1 - \left(\frac{I_2 R_0}{V_1}\right)^2}\right) \tag{20.31}$$

This expression limits the maximum switching frequency, or maximum F, of the half-wave ZCS quasi-resonant switch cell.

20.2.2 The Average Terminal Waveforms

It is now desired to solve for the power processing function performed by the switch network. The switch conversion ratio μ is a generalization of the duty cycle d. It expresses how a resonant switch network controls the average voltages and currents of a converter. In our buck converter example, we can define μ as the ratio of $\langle v_2(t)\rangle_{T_s}$ to $\langle v_1(t)\rangle_{T_s}$, or equivalently, the ratio of $\langle i_1(t)\rangle_{T_s}$ to $\langle i_2(t)\rangle_{T_s}$. In a hard-switched PWM network, this ratio is equal to the duty cycle d. Hence, analytical results derived for hard-switched PWM converters can be adapted to quasi-resonant converters, simply by replacing d with μ. In this section, we derive an expression for μ, by averaging the terminal waveforms of the switch network.

The switch input current waveform $i_1(t)$ of Fig. 20.10 is reproduced in Fig. 20.14. The average switch input current is given by

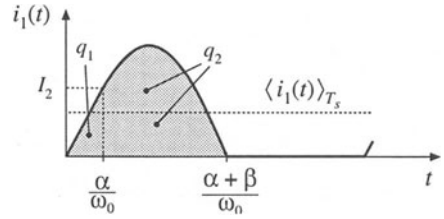

Fig. 20.14 Input current waveform $i_1(t)$, and the areas q_1 and q_2 during subintervals 1 and 2 respectively.

$$\langle i_1(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} i_1(t)dt = \frac{q_1+q_2}{T_s} \tag{20.32}$$

The charge quantities q_1 and q_2 are the areas under the $i_1(t)$ waveform during the first and second subintervals, respectively. The charge q_1 is given by the triangle area formula

$$q_1 = \int_0^{\frac{\alpha}{\omega_0}} i_1(t)dt = \frac{1}{2}\left(\frac{\alpha}{\omega_0}\right)(I_2) \tag{20.33}$$

The time α/ω_0 is the length of subinterval 1. The charge q_2 is

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_1(t)dt \tag{20.34}$$

According to Fig. 20.12, during subinterval 2 the current $i_1(t)$ can be related to the tank capacitor current $i_C(t)$ and the switch output current I_2 by the node equation

$$i_1(t) = i_C(t) + I_2 \tag{20.35}$$

Substitution of Eq. (20.35) into Eq. (20.34) leads to

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t)dt + \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2 dt \tag{20.36}$$

Both integrals in Eq. (20.36) can easily be evaluated, as follows. Since the second term involves the integral of the constant current I_2, this term is

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2 dt = I_2\frac{\beta}{\omega_0} \tag{20.37}$$

The first term in Eq. (20.36) involves the integral of the capacitor current over subinterval 2. Hence, this term is equal to the change in capacitor charge over the second subinterval:

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t)dt = C\left(v_2\left(\frac{\alpha+\beta}{\omega_0}\right) - v_2\left(\frac{\alpha}{\omega_0}\right)\right) \tag{20.38}$$

(recall that $\Delta q = C\Delta v$ in a capacitor). During the second subinterval, the tank capacitor voltage is initially zero, and has a final value of V_{c1}. Hence, Eq. (20.38) reduces to

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t)dt = C\left(V_{c1} - 0\right) = CV_{c1} \tag{20.39}$$

Substitution of Eqs. (20.37) and (20.39) into Eq. (20.36) leads to the following expression for q_2:

$$q_2 = CV_{c1} + I_2\frac{\beta}{\omega_0} \tag{20.40}$$

Equations (20.33) and (20.40) can now be inserted into Eq. (20.32), to obtain the following expression for the switch input current:

$$\left\langle i_1(t)\right\rangle_{T_s} = \frac{\alpha I_2}{2\omega_0 T_s} + \frac{CV_{c1}}{T_s} + \frac{\beta I_2}{\omega_0 T_s} \tag{20.41}$$

Substitution of Eq. (20.41) into (20.8) leads to the following expression for the switch conversion ratio:

$$\mu = \frac{\left\langle i_1(t)\right\rangle_{T_s}}{I_2} = \frac{\alpha}{2\omega_0 T_s} + \frac{CV_{c1}}{I_2 T_s} + \frac{\beta}{\omega_0 T_s} \tag{20.42}$$

Finally, the quantities α, β, and V_{c1} can be eliminated, using Eqs. (20.13), (20.20), (20.23). The result is

$$\mu = F\frac{1}{2\pi}\left[\frac{1}{2}J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s}\left(1 + \sqrt{1 - J_s^2}\right)\right] \tag{20.43}$$

where

$$J_s = \frac{I_2 R_0}{V_1} \tag{20.44}$$

Equation (20.43) is of the form

$$\mu = FP_{\frac{1}{2}}\left(J_s\right) \tag{20.45}$$

where

$$P_{\frac{1}{2}}\left(J_s\right) = \frac{1}{2\pi}\left[\frac{1}{2}J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s}\left(1 + \sqrt{1 - J_s^2}\right)\right] \tag{20.46}$$

Thus, the switch conversion ratio μ is directly controllable by variation of the switching frequency, through F. The switch conversion ratio is also a function of the applied terminal voltage V_1 and current I_2, via J_s. The function $P_{\frac{1}{2}}(J_s)$ is sketched in Fig. 20.15. The switch conversion ratio μ is sketched in Fig. 20.16, for various values of F and J_s. These characteristics are similar in shape to the function $P(J_s)$, and are simply scaled by the factor F. It can be seen that the conversion ratio μ is a strong function

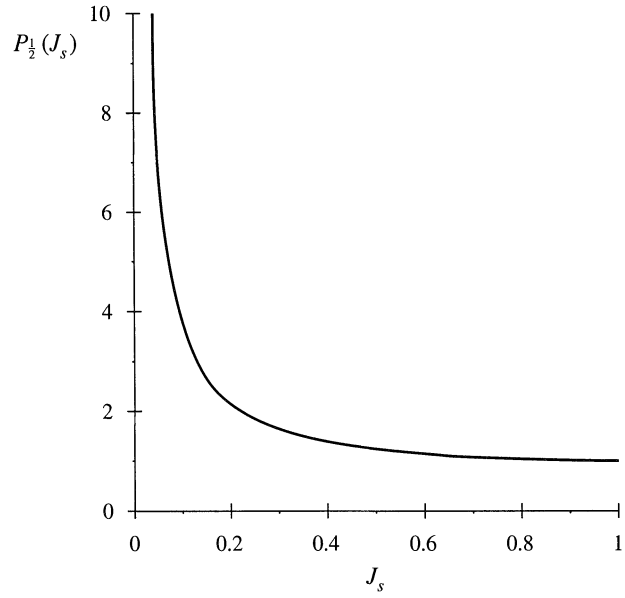

Fig. 20.15 The function $P_{\frac{1}{2}}(J_s)$.

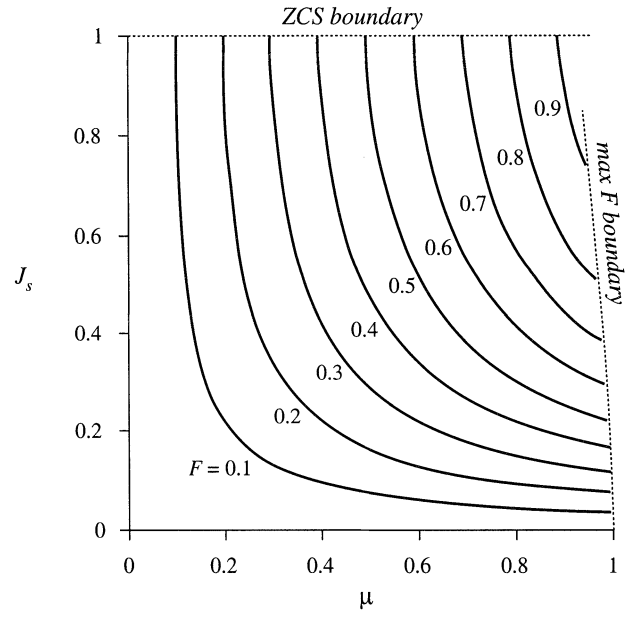

Fig. 20.16 Characteristics of the half-wave ZCS quasi-resonant switch.

of the current I_2, via J_s. The characteristics end at $J_s = 1$; according to Eq. (20.31), the zero current switching property is lost when $J_s > 1$. The characteristics also end at the maximum switching frequency limit given by Eq. (20.31). This expression can be simplified by use of Eq. (20.43), to express the limit in terms of μ as follows:

$$\mu \le 1 - \frac{J_s F}{4\pi} \tag{20.47}$$

The switch conversion ratio μ is thus limited to a value slightly less than 1.

The averaged waveforms of converters containing half-wave ZCS quasi-resonant switches can now be determined. The results of the analysis of PWM converters operating in the continuous conduction mode can be directly adapted to the related quasi-resonant converters, simply by replacing the duty cycle d with the switch conversion ratio μ. For the buck converter example, the conversion ratio is

$$M = \frac{V}{V_g} = \mu \tag{20.48}$$

This result could also be derived by use of the principle of inductor volt-second balance. The average voltage across the filter inductor is $(\mu V_g - V)$. Upon equating this voltage to zero, we obtain Eq. (20.48).

In the buck converter, I_2 is equal to the load current I, while V_1 is equal to the converter input voltage V_g. Hence, the quantity J_s is

$$J_s = \frac{IR_0}{V_g} \tag{20.49}$$

Zero current switching occurs for

$$I \le \frac{V_g}{R_0} \tag{20.50}$$

The output voltage can vary over the range

$$0 \le V \le V_g - \frac{FIR_0}{4\pi} \tag{20.51}$$

which nearly coincides with the PWM output voltage range $0 \le V \le V_g$.

A boost converter employing a half-wave ZCS quasi-resonant switch is illustrated in Fig. 20.17. The conversion ratio of the boost converter is given by

$$M = \frac{V}{V_g} = \frac{1}{1 - \mu} \tag{20.52}$$

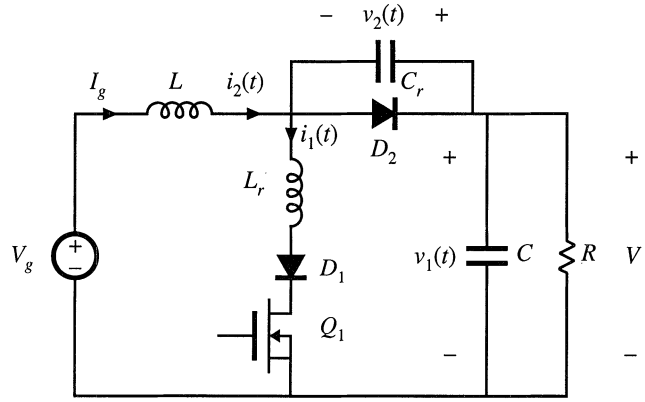

Fig. 20.17 Boost converter containing a half-wave ZCS quasi-resonant switch.

The half-wave switch conversion ratio μ is again given by Eqs. (20.44) to (20.46). For the boost converter, the applied switch voltage V_1 is equal to the output voltage V, while the applied switch current I_2 is equal to the filter inductor current, or I_g. Hence, the quantity J_s is

$$J_s = \frac{I_2 R_0}{V_1} = \frac{I_g R_0}{V} \tag{20.53}$$

Also, the input current I_g of the boost converter is related to the load current I according to

$$I_g = \frac{I}{1-\mu} \tag{20.54}$$

Equations (20.52) to (20.54), in conjunction with Eqs. (20.44) to (20.46), describe the averaged waveforms of the half-wave quasi-resonant ZCS boost converter.

20.2.3 The Full-Wave ZCS Quasi-Resonant Switch Cell

The full-wave ZCS quasi-resonant switch cell is illustrated in Fig. 20.8(d). It differs from the half-wave cell in that elements D_1 and Q_1 are connected in antiparallel, to form a current-bidirectional two-quadrant switch. Typical tank inductor current and tank capacitor voltage waveforms are illustrated in Fig. 20.18. These waveforms are similar to those of the half-wave case, except that the Q_1/D_1 switch interrupts the tank inductor current $i_1(t)$ at its second zero-crossing. While $i_1(t)$ is negative, diode D_1 conducts, and transistor Q_1 can be turned off at zero current.

The analysis is nearly the same as for the half-wave case, with the exception of subinterval 2. The subinterval 2 angular length β and final voltage V_{c1} can be shown to be

$$\beta = \begin{cases} \pi + \sin^{-1}(J_s) & \text{(half wave)} \\ 2\pi - \sin^{-1}(J_s) & \text{(full wave)} \end{cases} \tag{20.55}$$

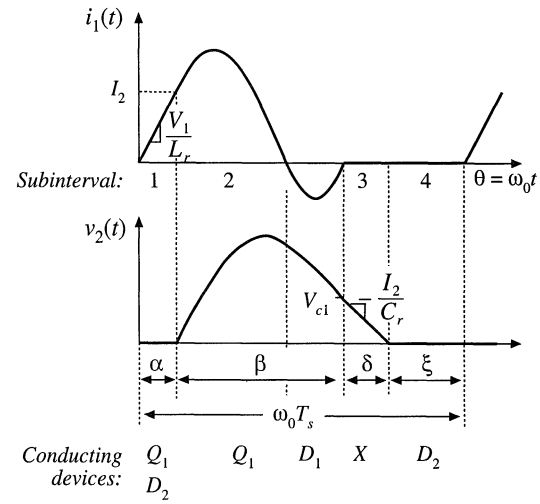

Fig. 20.18 Tank inductor current and capacitor voltage waveforms, for the full-wave ZCS quasi-resonant switch cell of Fig. 20.8(d).

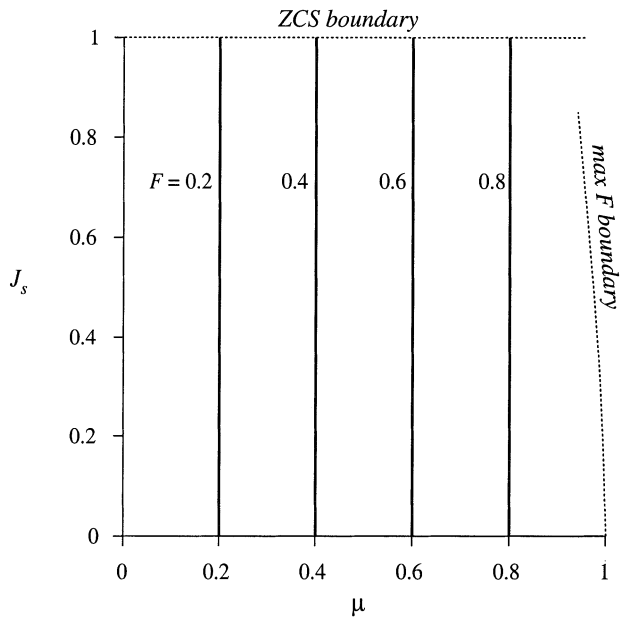

Fig. 20.19 Characteristics of the full-wave ZCS quasi-resonant switch.

$$V_{c1} = \begin{cases} V_1\left(1+\sqrt{1-J_s^2}\right) & \text{(half wave)} \\ V_1\left(1-\sqrt{1-J_s^2}\right) & \text{(full wave)} \end{cases} \tag{20.56}$$

In either case, the switch conversion ratio μ is given by Eq. (20.42). For the full-wave switch, one obtains

$$\mu = FP_1(J_s) \tag{20.57}$$

where $P_1(J_s)$ is given by

$$P_1(J_s) = \frac{1}{2\pi}\left[\tfrac{1}{2}J_s + 2\pi - \sin^{-1}(J_s) + \frac{1}{J_s}\left(1-\sqrt{1-J_s^2}\right)\right] \tag{20.58}$$

In the full-wave case, $P_1(J_s)$ is essentially independent of J_s:

$$P_1(J_s) \approx 1 \tag{20.59}$$

The worst-case deviation of $P_1(J_s)$ from 1 occurs as J_s tends to 1, where $P_1(J_s)$ tends to 0.96. So $P_1(J_s)$ lies within 4% of unity for $0 < J_s < 1$. Hence, for the full-wave case, it is a good approximation to express the switch conversion ratio as

$$\mu \approx F = \frac{f_s}{f_0} \tag{20.60}$$

The full-wave quasi-resonant switch therefore exhibits voltage-source output characteristics, controllable

by F. Equations describing the average waveforms of CCM PWM converters can be adapted to apply to full-wave ZCS quasi-resonant converters, simply by replacing the duty cycle d with the normalized switching frequency F. The conversion ratios of full-wave quasi-resonant converters exhibit negligible dependence on the load current.

The variation of the switch conversion ratio μ with F and J_s is plotted in Fig. 20.19. For a typical voltage regulator application, the range of switching frequency variations is much smaller in the full-wave mode than in the half-wave mode, because μ does not depend on the load current. Variations in the load current do not induce the controller to significantly change the switching frequency.

20.3 RESONANT SWITCH TOPOLOGIES

So far, we have considered the zero-current-switching quasi-resonant switch cell, illustrated in Fig. 20.20. The ideal SPST switch is realized using a voltage-bidirectional or current-bidirectional two-quadrant switch, to obtain half-wave or full-wave ZCS quasi-resonant switch networks, respectively.

The resonant elements L_r and C_r can be moved to several different positions in the converter, without altering the basic switch properties. For example, Fig. 20.21 illustrates connection of the resonant tank capacitor C_r between the cathode of diode D_2, and the converter output or input terminals. Although this may change the dc component of the tank capacitor voltage, the ac components of the tank capacitor voltage waveform are unchanged. Also, the terminal voltage waveform $v_2(t)$ is unchanged. The voltages $v_g(t)$ and $v(t)$ contain negligible high-frequency ac components, and hence the converter input and output terminal potentials can be considered to be at high-frequency ac ground.

A test to determine the topology of a resonant switch network is to replace all low-frequency filter inductors with open circuits, and to replace all dc sources and low-frequency filter capacitors with short circuits [13]. The elements of the resonant switch cell remain. In the case of the zero-current-switching quasi-resonant switch, the network of Fig. 20.22 is always obtained.

It can be seen from Fig. 20.22 that diode D_2 switches on and off at the zero crossings of the tank capacitor voltage $v_2(t)$, while the switch elements Q_1 and D_1 switch at the zero crossings of the tank inductor current $i_1(t)$. Zero voltage switching of diode D_2 is highly advantageous, because it essentially eliminates the switching loss caused by the recovered charge and output capacitance of diode D_2. Zero current switching of Q_1 and D_1 can be used to advantage when Q_1 is realized by an SCR or IGBT. However, in high-frequency converters employing MOSFETs, zero current switching of Q_1 and D_1 is generally a poor choice. Significant switching loss due to the output capacitances of Q_1 and D_1 may be observed. In addition, in the full-wave case, the recovered charge of diode D_1 leads to significant ringing

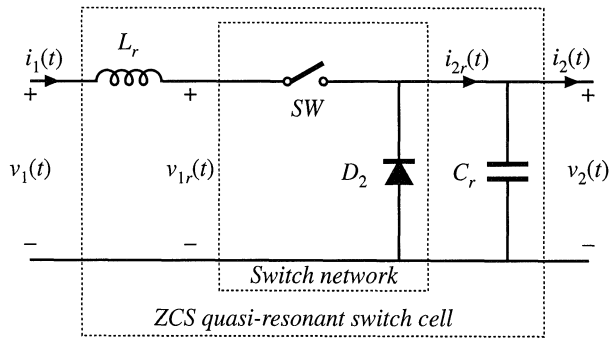

Fig. 20.20 Basic ZCS quasi-resonant switch cell.

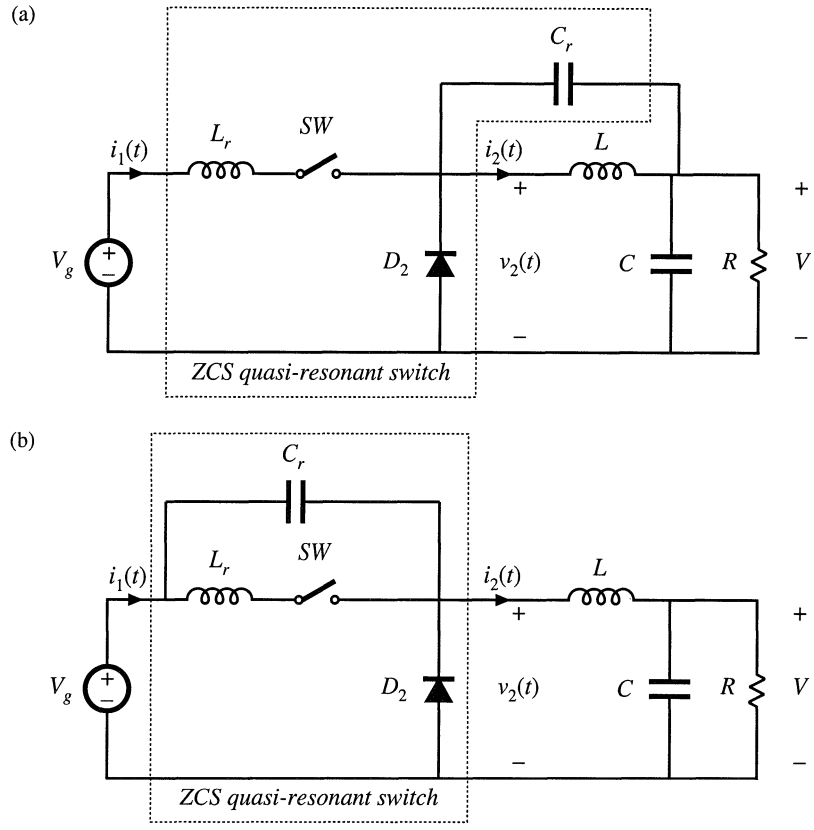

Fig. 20.21 Connection of the tank capacitor of the ZCS quasi-resonant cell to other points at ac ground: (a) connection to the dc output, (b) connection to the dc input. In each case, the ac components of the waveforms are unchanged.

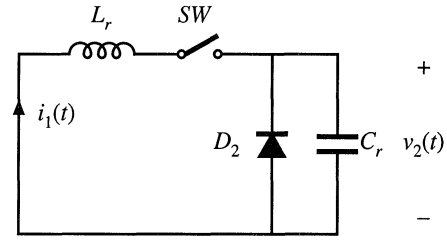

Fig. 20.22 Elimination of converter low-frequency elements causes the ZCS quasi-resonant switch cell to reduce to this network.

and switching loss at the end of subinterval 2 [3].

The ZCS quasi-resonant switch exhibits increased conduction loss, relative to an equivalent PWM switch, because the peak transistor current is increased. The peak transistor current is given by Eq. (20.17); since $J_s \leq 1$, the peak current is $I_{1pk} \geq 2I_2$. In addition, the full-wave ZCS switch exhibits poor efficiency at light load, owing to the conduction loss caused by circulating tank currents. The half-wave ZCS switch exhibits additional conduction loss due to the added forward voltage drop of diode D_1. The peak transistor voltage is V_1, which is identical to the PWM case.

20.3.1 The Zero-Voltage-Switching Quasi-Resonant Switch

The resonant switch network illustrated in Fig. 20.23 is the dual of the network of Fig. 20.22. This network is known as the zero-voltage-switching quasi-resonant switch [4]. Since the tank capacitor C_r appears in parallel with the SPST switch, the elements Q_1 and D_1 used to realize the SPST switch turn on and off at zero voltage. The tank inductor L_r is effectively in series with diode D_2, and hence diode D_2 switches at zero current. Converters containing ZVS quasi-resonant switches can be realized in a number of ways. The only requirement is that, when the low-frequency filter inductors, filter capacitors, and sources are replaced by open- or short-circuits as described above, then the high-frequency switch network of Fig. 20.23 should remain.

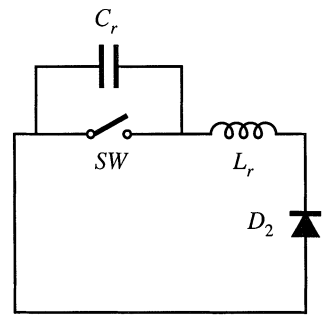

Fig. 20.23 Elimination of converter low-frequency elements reduces the ZVS quasi-resonant switch cell to this network.

For example, a zero-voltage-switching quasi-resonant buck converter is illustrated in Fig. 20.24(a). Typical tank capacitor voltage and tank inductor current waveforms are given in Fig. 20.24(b). A current-bidirectional realization of the two-quadrant SPST switch is shown; this causes the ZVS quasi-resonant switch to operate in the half-wave mode. Use of a voltage-bidirectional two-quadrant SPST switch allows full-wave operation.

By analysis similar to that of Section 20.2, it can be shown that the switch conversion ratio μ of the half-wave ZVS quasi-resonant switch is

$$\mu = 1 - FP_{\frac{1}{2}}\left(\frac{1}{J_s}\right) \tag{20.61}$$

The function $P_{\frac{1}{2}}(J_s)$ is again given by Eq. (20.46), and the quantity J_s is defined in Eq. (20.44). For the full-wave ZVS quasi-resonant switch, one obtains

$$\mu = 1 - FP_1\left(\frac{1}{J_s}\right) \tag{20.62}$$

where $P_1(J_s)$ is given by Eq. (20.58). The condition for zero voltage switching is

$$J_s \geq 1 \tag{20.63}$$

Thus, the zero voltage switching property is lost at light load. The peak transistor voltage is given by

$$\text{peak transistor voltage } V_{cr,pk} = (1 + J_s)V_1 \tag{20.64}$$

This equation predicts that load current variations can lead to large voltage stress on transistor Q_1. For example, if it is desired to obtain zero voltage switching over a 5:1 range of load current variations, then J_s should vary between 1 and 5. According to Eq. (20.64), the peak transistor voltage then varies between two times and six times the applied voltage V_1. The maximum transistor current is equal to the applied current I_2. Although the maximum transistor current in the ZVS quasi-resonant switch is identical to that

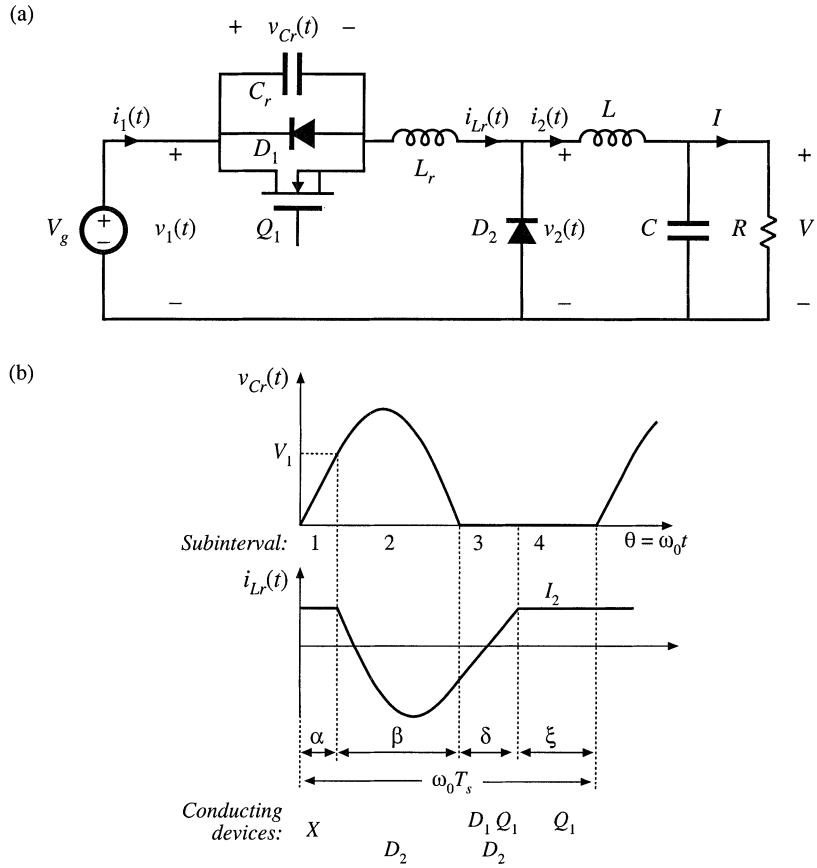

Fig. 20.24 A ZVS quasi-resonant buck converter: (a) circuit, (b) tank waveforms.

of the PWM switch, the peak transistor blocking voltage is substantially increased. This leads to increased conduction loss, because transistor on-resistance increases rapidly with rated blocking voltage.

20.3.2 The Zero-Voltage-Switching Multiresonant Switch

The resonant switch network of Fig. 20.25 contains tank capacitor C_d in parallel with diode D_2, as in the ZCS switch network of Fig. 20.22. In addition, it contains tank capacitor C_s in parallel with the SPST switch, as in the ZVS switch network of Fig. 20.23. In consequence, all semiconductor elements switch at zero voltage. This three-element resonant switch network is known as the zero-voltage-switching multiresonant switch (ZVS MRS). Since no semiconductor output capacitances or diode recovered charges lead to ringing or switching loss, the ZVS MRS exhibits very low switching loss. For the same reason, generation of electromagnetic interference is reduced.

A half-wave ZVS MRS realization of the buck converter is illustrated in Fig. 20.26. In a typical design that must operate over a 5:1 load range and with $0.4 \le \mu \le 0.6$, the designer might choose a maximum F of 1.0, a maximum J of 1.4, and $C_d/C_s = 3$, where these quantities are defined as follows:

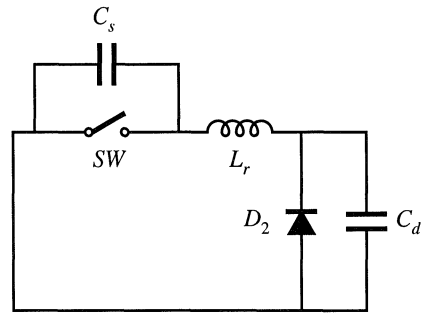

Fig. 20.25 Elimination of converter low-frequency elements reduces the ZVS multiresonant switch cell to this network.

$$f_0 = \frac{1}{2\pi\sqrt{LC_t}} \quad R_0 = \sqrt{\frac{L}{C_t}}$$
$$F = \frac{f_s}{f_0} \quad J = \frac{I_2 R_0}{V_1} \tag{20.65}$$

As usual, the conversion ratio is defined as $\mu = V_2/V_1$. The resulting peak transistor voltage for this typical design is approximately $2.8V_1$, while the peak transistor current is $2I_2$. Hence, conduction losses are higher than in an equivalent PWM switch. The range of switch conversion ratios μ is a function of the capacitor ratio C_d/C_s; in a good design, values of μ ranging from nearly one to nearly zero can be obtained, with a wide range of dc load currents and while maintaining zero voltage switching.

Analysis and design charts for the ZVS MRS are given in [5–8]. Results for the typical choice $C_d = 3C_s$ are plotted in Fig. 20.27. These plots illustrate how the switch conversion ratio μ varies as a function of load current and switching frequency. Figure 20.27(a) also illustrates the boundary of zero-voltage switching: ZVS is lost for operation outside the dashed lines. Decreasing the ratio of C_d to C_s reduces the area of the ZVS region.

Other resonant converters in which all semiconductor devices operate with zero voltage switching are known. Examples include some operating modes of the parallel and LCC resonant converters described in Chapter 19, as well as the class–E converters described in [10–12].

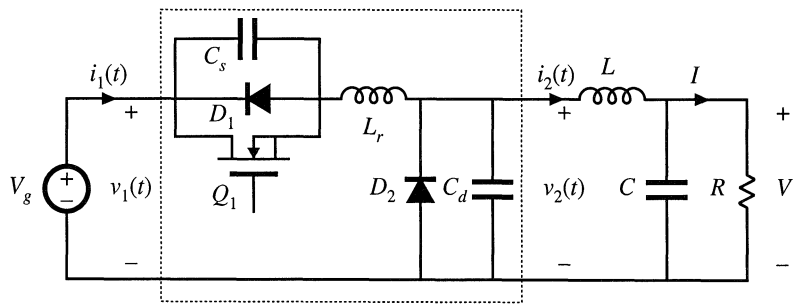

Fig. 20.26 Half-wave ZVS multiresonant buck converter.

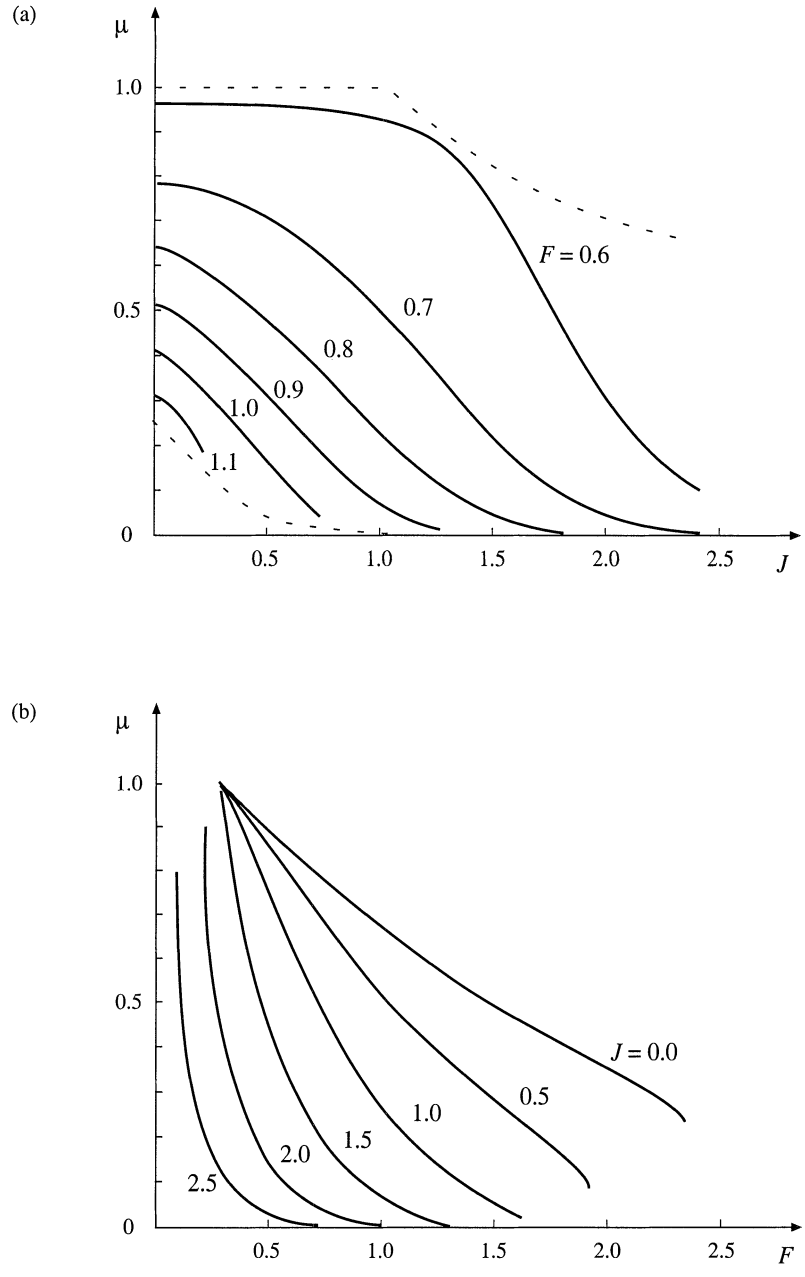

Fig. 20.27 Conversion ratio μ for the multi-resonant switch with $C_d = 3C_s$: (a) conversion ratio μ vs. normalized current J (solid lines: conversion ratio; dashed lines: boundaries of zero-voltage switching), (b) conversion ratio μ vs. normalized switching frequency F.

20.3.3 Quasi-Square-Wave Resonant Switches

Another basic class of resonant switch networks is the quasi-square wave converters. Both zero-voltage switching and zero-current switching versions are known; the resonant tank networks are illustrated in Fig. 20.28. In the network of Fig. 20.28(a), all semiconductor devices are effectively in series with the tank inductor, and hence operate with zero-current switching. In the network of Fig. 20.28(b), all semiconductor devices are effectively in parallel with the tank capacitor, and hence operate with zero-voltage switching.

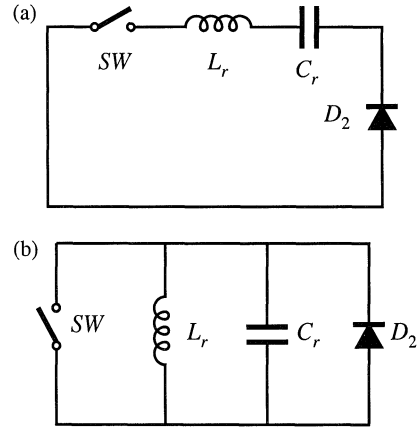

Fig. 20.28 Elimination of converter low-frequency elements reduces the quasi-square-wave switch cells to these networks: (a) ZCS quasi-square-wave network, (b) ZVS quasi-square-wave network.

Figure 20.29 illustrates implementation of a zero current switching quasi-square wave resonant switch, in a buck converter with input filter. Elements L_f and C_f are large in value, and constitute a single-section L–C input filter. Elements L_r and C_r form the series resonant tank; these elements are placed in series with input filter capacitor C_f. Since C_r and C_f are connected in series, they can be combined into a single small-value capacitor. In this zero-current-switching converter, the peak transistor current is identical to the peak transistor current of an equivalent PWM converter. However, the peak transistor blocking voltage is increased. The ZCS QSW resonant switch exhibits a switch conversion ratio μ that is restricted to the range $0 \le \mu \le 0.5$. Analysis of this resonant switch is given in [13–14].

A buck converter, containing a zero-voltage-switching quasi-square wave (ZVS QSW) resonant switch, is illustrated in Fig. 20.30. Typical waveforms are given in Fig. 20.31. Since the tank inductor L_r and the output filter inductor L are connected in parallel, these two elements can be combined into a single inductor having a small value nearly equal to L_r. Analyses of the ZVS QSW resonant switch are given in [14,15,18]. A related full-bridge converter is described in [16]. The ZVS QSW resonant switch is notable because zero voltage switching is obtained in all semiconductor devices, yet the peak transistor voltage is identical to that of an equivalent PWM switch [13]. However, the peak transistor currents are increased.

Characteristics of the zero-voltage-switching quasi-square wave resonant switch are plotted in Fig. 20.32. The switch conversion ratio $\mu = V_2/V_1$ is plotted as a function of normalized switching fre-

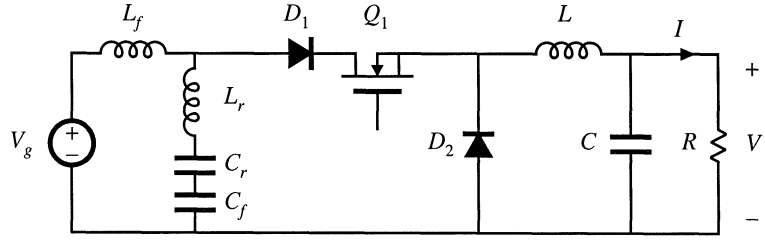

Fig. 20.29 Incorporation of a ZCS quasi-square-wave resonant switch into a buck converter containing an L–C input filter.

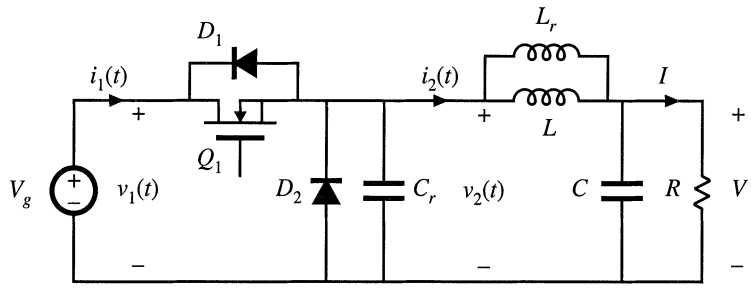

Fig. 20.30 Incorporation of a ZVS quasi-square-wave resonant switch into a buck converter.

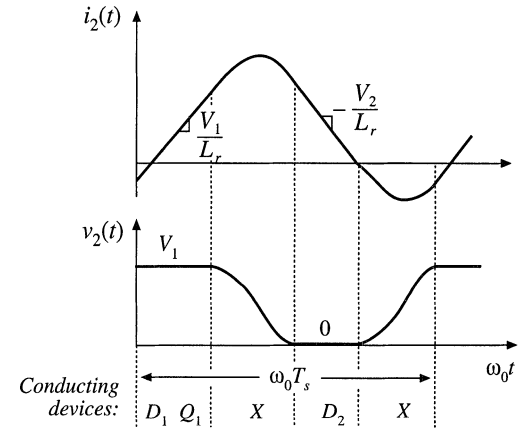

Fig. 20.31 Waveforms of the ZVS quasi-square-wave resonant switch converter of Fig. 20.30.

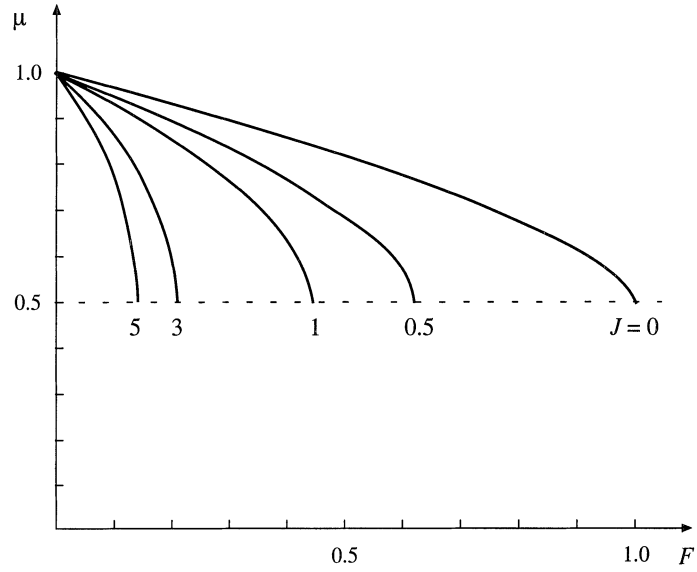

Fig. 20.32 Characteristics of the ZVS quasi-square wave resonant switch network: switch conversion ratio μ, as a function of F and J. Dashed line: ZVS boundary.

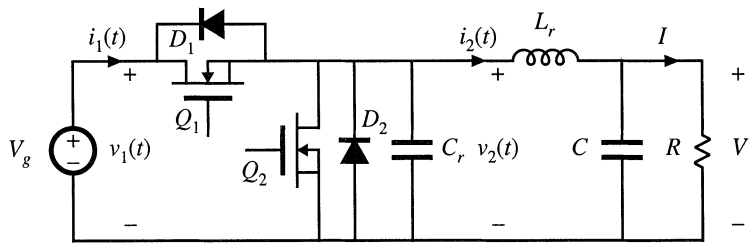

Fig. 20.33 Quasi-square wave ZVS buck converter containing a synchronous rectifier.

quency F and normalized output current J, where these quantities are defined as follows:

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad R_0 = \sqrt{\frac{L_r}{C_r}}$$
$$F = \frac{f_s}{f_0} \qquad J = \frac{I_2 R_0}{V_1} \tag{20.66}$$

In addition, the zero-voltage-switching boundary is plotted. It can be seen that the requirement for zero-voltage switching limits the switch conversion ratio μ to the range $0.5 \leq \mu \leq 1$. In consequence, the buck converter of Fig. 20.30 cannot produce output voltages less than $0.5V_g$ without losing the ZVS property. A version which attains $0 \leq \mu \leq 1$, at the expense of increased transistor voltage stress, is described in [17]. In addition, the two-switch version of the ZVS-QSW switch can operate with ZVS for $\mu < 0.5$.

A useful variant of the converter of Fig. 20.30 involves replacement of the diode with a synchronous rectifier, as illustrated in Fig. 20.33 [8,9]. The second transistor introduces an additional degree of freedom in control of the converter, because this transistor can be allowed to conduct longer than the diode would otherwise conduct. This fact can be used to extend the region of zero-voltage switching to conversion ratios approaching zero, and also to operate the converter with constant switching frequency.

Typical tank element waveforms for the circuit of Fig. 20.33 are illustrated in Fig. 20.34. These waveforms resemble those of the single switch case, Fig. 20.31, except that the tank current is negative while transistor Q_2 conducts. The duty cycle D is defined with respect to the turn-off transitions

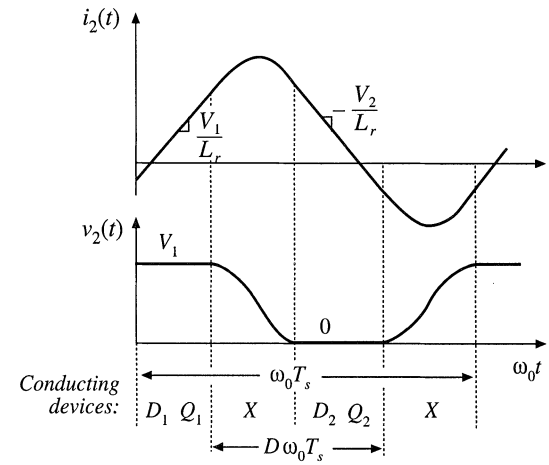

Fig. 20.34 Waveforms for the two-switch QSW-ZVS converter of Fig. 20.33.

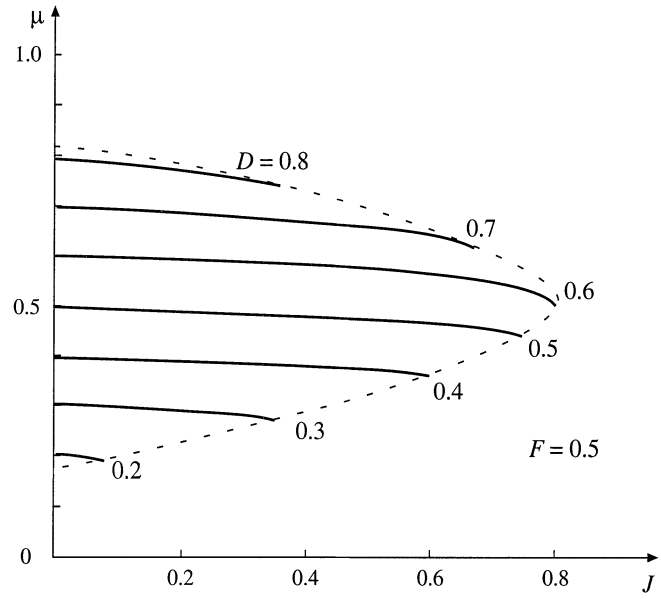

Fig. 20.35 Conversion ratio μ, as a function of duty cycle D and normalized load current J, for the two-switch QSW-ZVS switch illustrated in Fig. 20.33. Curves are plotted for constant-frequency control with $F = 0.5$. The dashed line is the zero-voltage switching boundary.

of transistors Q_1 and Q_2, as illustrated.

Characteristics of the two-switch QSW-ZVS switch network are plotted in Fig. 20.35, for the case of constant switching frequency at $F = 0.5$. The boundary of zero-voltage switching is also illustrated. Operation at a lower value of F causes the ZVS boundary to be extended to larger values of J, and to values of μ that more closely approach the extreme values $\mu = 0$ and $\mu = 1$.

To the commutation intervals can be neglected, one would expect that the switch conversion ratio μ is simply equal to the duty cycle D. It can be seen from Fig. 20.35 that this is indeed the case. The characteristics are approximately horizontal lines, nearly independent of load current J.

Zero-voltage switching quasi-square wave converters exhibit very low switching loss, because all semiconductor elements operate with zero-voltage switching. In the constant-frequency case containing a synchronous rectifier, the converter behavior is nearly the same as for the hard-switched PWM case, since $\mu \approx D$. The major disadvantage is the increased conduction loss, caused by the reversal of the inductor current.

20.4 SOFT SWITCHING IN PWM CONVERTERS

The quasi-square wave approach of the previous section is notable because it attains zero-voltage switching without increasing the peak voltage applied to the transistor. Several related soft-switching approaches have now become popular, which also attain zero-voltage switching without increasing the transistor peak voltage stress. In this section, popular zero-voltage switching versions of the full bridge, forward, and flyback converters, as well as the voltage-source inverter, are briefly discussed.

20.4.1 The Zero-Voltage Transition Full-Bridge Converter

It is possible to obtain soft switching in other types of converters as well. An example is the zero-voltage transition (ZVT) converter based on the full-bridge transformer–isolated buck converter, illustrated in Fig. 20.36 [25–28]. The transistor and diode output capacitances are represented in the figure by capacitances C_{leg}. Commutating inductor L_c is placed in series with the transformer; the net inductance L_c includes both transformer leakage inductance and the inductance of an additional discrete element. This inductor causes the full-bridge switch network to drive an effective inductive load, and results in zero-voltage switching of the primary-side semiconductor devices. Although the waveforms are not sinusoidal, it can nonetheless be said that the switch network output current $i_c(t)$ lags the voltage $v_s(t)$, because the zero crossings of $i_c(t)$ occur after the ZVS switching transitions are completed.

The output voltage is controlled via phase control. As illustrated in Fig. 20.37, both halves of the bridge switch network operate with a 50% duty cycle, and the phase difference between the half-bridge switch networks is controlled. The idealized waveforms of Fig. 20.37 neglect the switching transitions, and the subinterval numbers correspond to those of the more detailed Fig. 20.38. The phase shift variable ϕ lies in the range $0 \le \phi \le 1$, and assumes the role of the duty cycle d in this converter. The quantity ϕ is defined as

$$\phi = \frac{(t_1 - t_0)}{\left(\frac{T_s}{2}\right)} \tag{20.67}$$

By volt-second balance on the secondary-side filter inductor, the conversion ratio $M(\phi)$ is expressed as

$$M(\phi) = \frac{V}{V_g} = n\phi \tag{20.68}$$

This expression neglects the lengths of the switching transitions.

Although the circuit appears symmetrical, the phase-shift control scheme introduces an asymmetry that causes the two half-bridge switch networks to behave quite differently during the switching transitions. During subintervals 4 and 10, energy is actively transmitted from the source V_g through the switches and transformer. These subintervals are initiated by the switching of the half-bridge network

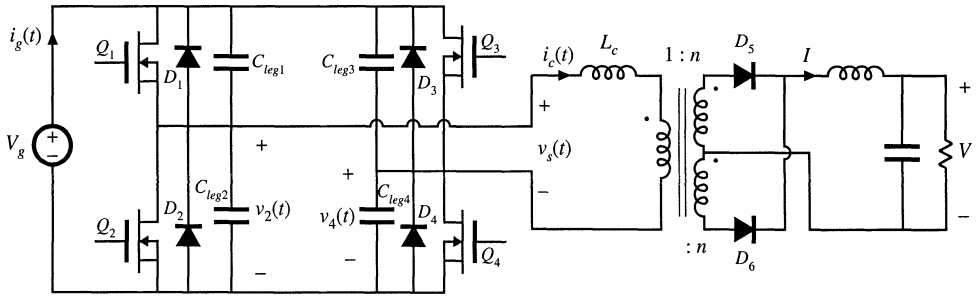

Fig. 20.36 Zero-voltage transition converter, based on the full-bridge isolated buck converter.

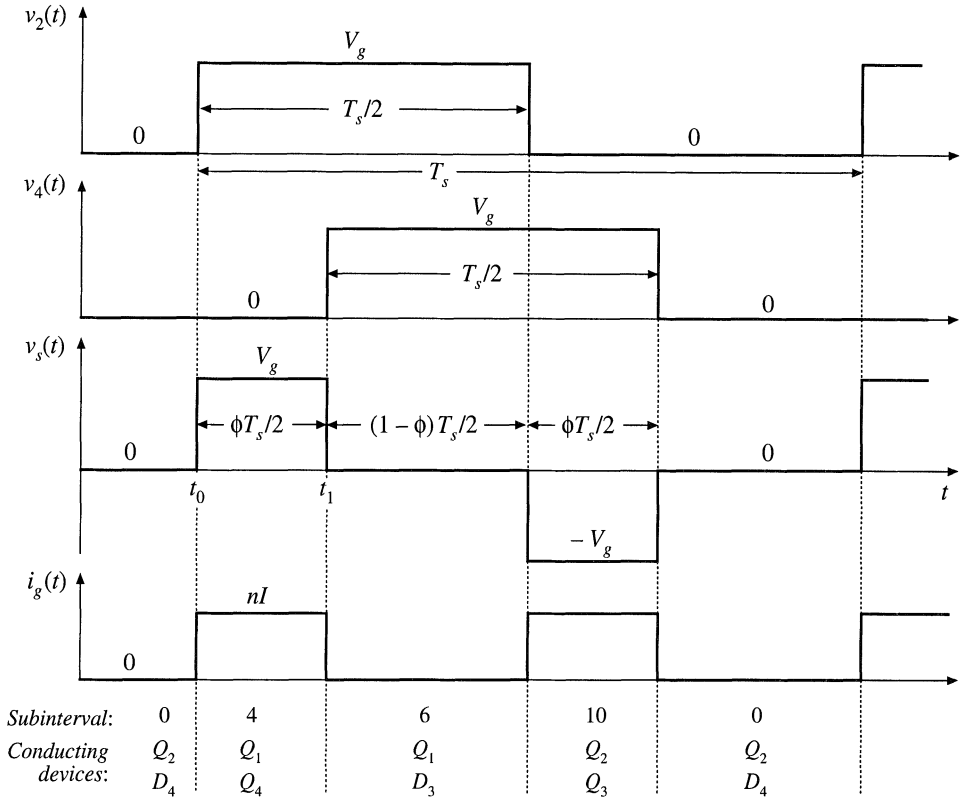

Fig. 20.37 Phase-shift control of the ZVT full-bridge converter. Switching transitions are neglected in this figure, and subinterval numbering follows Fig. 20.38.

composed of the elements Q_1, D_1, Q_2, and D_2, called the "passive-to-active" (P–A) transition [27]. Subintervals 4 and 10 are terminated by the switching of the half-bridge network comprised by the elements Q_3, D_3, Q_4, and D_4, called the "active-to-passive" (A–P) transition.

The turn-on and turn-off switching processes of this converter are similar to the zero-voltage-switching turn-off process described in the previous section. Detailed primary-side waveforms are illustrated in Fig. 20.38. During subinterval 0, Q_2 and D_4 conduct. If the transformer magnetizing current i_M is negligible, then the commutating inductor current is given by $i_c(t_0) = -nI$, where I is the load current. The passive-to-active transition is initiated when transistor Q_2 is turned off. The negative i_c then causes capacitors C_{leg1} and C_{leg2} to charge, increasing $v_2(t)$. During subinterval 1, L_c, C_{leg1}, and C_{leg2} form a resonant network that rings with approximately sinusoidal waveforms. If sufficient energy was initially stored in L_c, then $v_2(t)$ eventually reaches V_g, terminating subinterval 1. Diode D_1 then clamps $v_2(t)$ to V_g during subinterval 2. Transistor Q_1 is turned on at zero voltage during subinterval 2; in practice, this is implemented by insertion of a small delay between the switching transitions of transistors Q_2 and Q_1.

If L_c does not initially store sufficient energy to charge the total capacitance ($C_{leg1} + C_{leg2}$) from $v_2 = 0$ to $v_2 = V_g$ during subinterval 1, then $v_2(t)$ will never reach V_g. Switching loss will then occur when transistor Q_1 is turned on. This situation typically occurs at light load, where I is small. Sometimes, the design engineer may choose to simply accept this power loss; after all, other losses such as conduction loss are small at light load. An alternative is to modify the circuit to increase the energy stored in L_c at

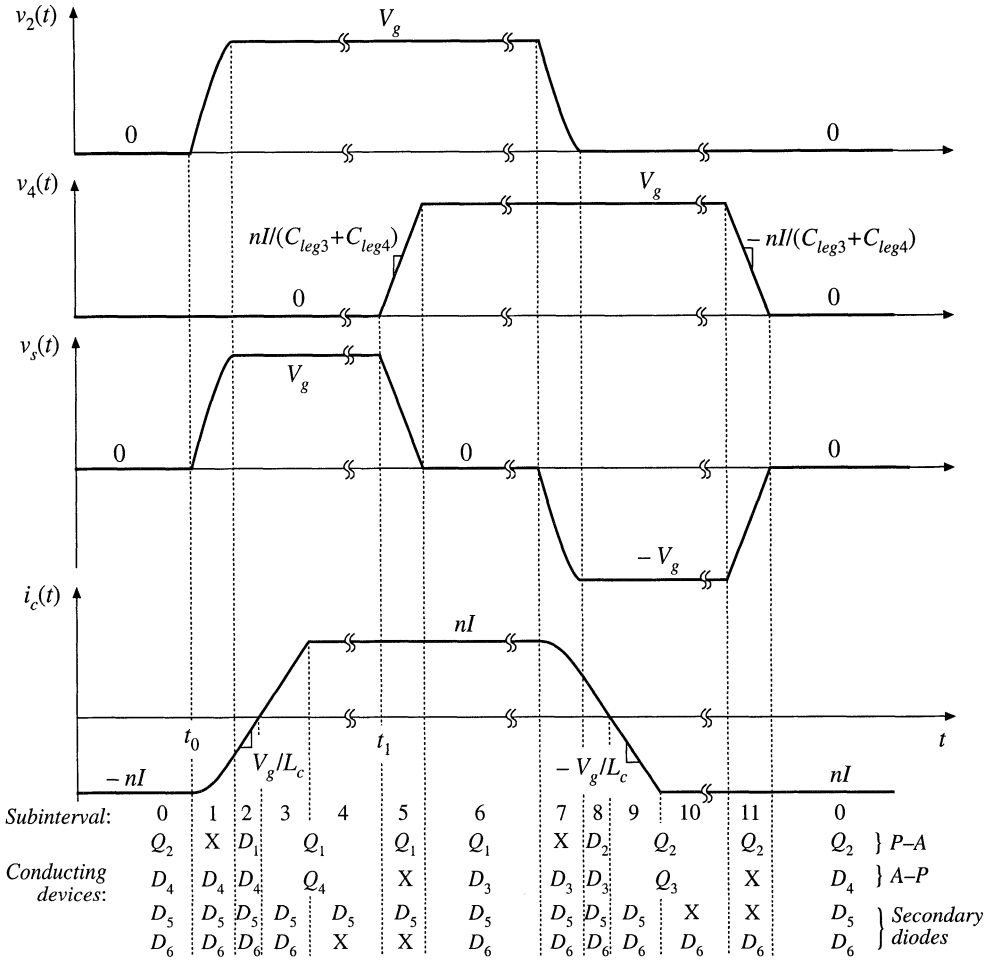

Fig. 20.38 Detailed diagram of primary-side waveforms of the ZVT full-bridge converter, illustrating the zero-voltage switching mechanisms. An ideal transformer is assumed.

$t = t_0$ under light load conditions. One way to accomplish this is to increase the transformer magnetizing current $i_M(t_0)$ to a significant level; at the beginning of subinterval 1, i_c is then equal to $i_c(t_0) = -nI + i_M(t_0)$ with $i_M(t_0) < 0$. At light load where I is small, the magnetizing current maintains the required level of i_c.

During subintervals 0, 1, 2, and 3, secondary-side diodes D_5 and D_6 both conduct; hence, zero voltage appears across all transformer windings. In consequence, voltage V_g is applied to commutating inductor L_c during subintervals 2 and 3, causing $i_c(t)$ to increase with slope V_g/L_c. Current $i_c(t)$ reaches zero at the end of subinterval 2, and increases to the positive value $+nI$ at the end of subinterval 3. The reversal of polarity of $i_c(t)$ enables zero-voltage switching during the next switching transitions, subinterval 5 and subintervals 7–9.

At the end of subinterval 3, the current in diode D_6 has decreased to zero. D_6 then becomes reverse-biased, with zero-current switching. At this instant, diode D_6 must begin to block voltage $2nV_g$.

The output capacitance of D_6 prevents the voltage from changing immediately to $2nV_g$; instead, the resonant circuit formed by L_c and the D_6 output capacitance begins to ring in a manner similar to Fig. 4.54. Peak D_6 voltages are typically observed that are considerably in excess of $2nV_g$, and it is usually necessary to add voltage-clamp snubbers that prevent the secondary-side diode voltages from exceeding a safe value. Several dissipative and non-dissipative approaches are discussed in [26–28].

The active-to-passive switching transition occurs during subinterval 5. This subinterval is initiated when transistor Q_4 is turned off. The positive current $i_c(t_1)$ is equal to the reflected load current nI, and charges capacitors C_{leg3} and C_{leg4} from $v_4 = 0$ to $v_4 = V_g$. Subinterval 5 ends when v_4 reaches V_g; Diode D_3 then becomes forward-biased. Transistor Q_3 is then turned on during subinterval 6, with zero-voltage switching. This is typically implemented by insertion of a small delay between the switching of transistors Q_4 and Q_3. Because i_c is constant and equal to nI during subinterval 5, the active-to-passive transition maintains zero-voltage switching at all load currents.

Circuit behavior during the next half switching period, comprising subintervals 6 to 11, is symmetrical and therefore similar to the behavior observed during subintervals 0 to 5. The switching transitions of transistors Q_1 and Q_2 are passive-to-active transitions, and occur with zero-voltage switching provided that sufficient energy is stored in L_c as described above. The switching transitions of Q_3 and Q_4 are active-to-passive, and occur with zero-voltage switching at all loads.

The zero-voltage transition converter exhibits low primary-side switching loss and generated EMI. Conduction loss is increased with respect to an ideal PWM full-bridge topology, because of the current i_c that circulates through the primary-side semiconductors during subintervals 0 and 6. However, this increase in conduction loss can be small if the range of input voltage variations is narrow. This soft-switching approach has now found commercial success.

20.4.2 The Auxiliary Switch Approach

A similar approach can be used in forward, flyback, and other transformer-isolated converters. As illustrated in Fig. 20.39, an "active-clamp snubber" network consisting of a capacitor and auxiliary MOSFET Q_2 is added, that is effectively in parallel with the original power transistor Q_1 [29]. The MOSFET body diodes and output drain-to-source capacitances, as well as the transformer leakage inductance L_ℓ, participate in the circuit operation. These elements lead to zero-voltage switching, with waveforms similar to those of the ZVT full-bridge converter of Section 20.4.1 or the two-transistor QSW-ZVS switch of Section 20.3.3. The transistors are driven by complementary signals; for example, after turning off Q_1, the controller waits for a short delay time and then turns on Q_2.

The active-clamp snubber can be viewed as a voltage-clamp snubber, similar to the dissipative snubber illustrated in Fig. 20.6. However, the snubber contains no resistor; instead, MOSFET Q_2 allows bidirectional power flow, so that the energy stored in capacitor C_s can flow back into the converter.

The voltage v_s can be found by volt-second inductance on the transformer magnetizing inductance. If the lengths of the commutation intervals are neglected, and if the voltage ripple in $v_s(t)$ can be neglected, then one finds that

$$V_s = \frac{D}{D'} V_g \tag{20.69}$$

The voltage v_s is effectively an unloaded output of the converter. With the two-quadrant switch provided by Q_2, this output operates in continuous conduction mode with no load, and hence the peak voltage of Q_1 is clamped to the minimum level necessary to balance the volt-seconds applied to the transformer magnetizing inductance.

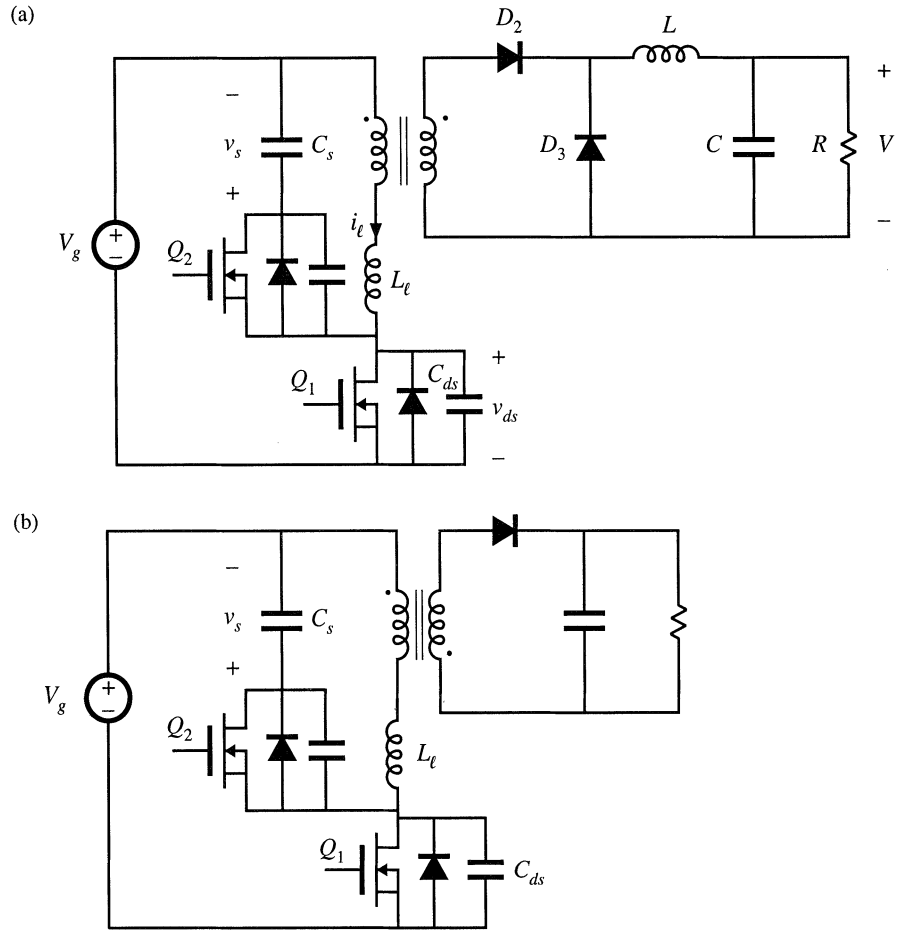

Fig. 20.39 Active-clamp snubber circuits: (a) forward converter, (b) flyback converter.

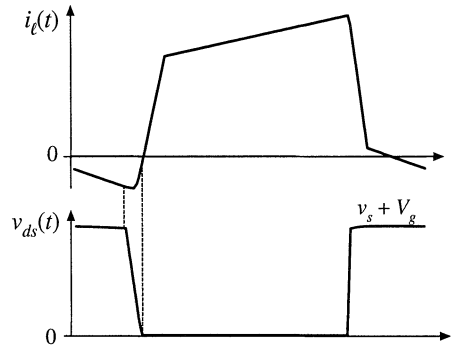

Fig. 20.40 Waveforms of the active-clamp snubber circuit of Fig. 20.39(a).

Typical waveforms for a forward converter incorporating an active-clamp snubber are illustrated in Fig. 20.40. The current $i_\ell(t)$ reverses direction while Q_2 conducts. When Q_2 turns off, capacitor C_{ds} begins to discharge. When v_{ds} reaches zero, the body diode of Q_1 becomes forward-biased. Q_1 can then be turned on at zero voltage.

An added benefit of the active clamp snubber, when used in a forward converter, is that it resets the transformer. Consequently, the converter can operate at any duty cycle, including duty cycles greater than 50%. When the converter must operate with a wide range of input voltages, this can allow substantial improvements in transistor stresses and efficiency. The MOSFETs in Fig. 20.39 operate with zero-voltage switching, while the secondary-side diodes operate with zero-current switching.

This approach is quite versatile, and similar auxiliary circuits can be added to other converter circuits to obtain zero-voltage switching [30,31].

20.4.3 Auxiliary Resonant Commutated Pole

The auxiliary resonant commutated pole (ARCP) is a related circuit that uses an auxiliary four-quadrant switch (or two equivalent two-quadrant switches) to obtain soft switching in the transistors of a bridge inverter circuit [32–34]. This approach finds application in dc–ac inverter circuits. Figure 20.41 illustrates a half-bridge circuit, or one phase of a three-phase voltage-source inverter, driving an ac load. This circuit can lead to zero-voltage switching that mitigates the switching loss induced by the reverse recovery of diodes D_1 and D_2. Filter inductor L_f is relatively large, so that the output current $i_a(t)$ is essentially constant during the resonant commutation interval. Capacitors C_{ds} are relatively small, and model the output capacitances of the semiconductor devices. Inductor L_r is also relatively small, and elements L_r and C_{ds} form a resonant circuit that rings during part of the commutation process. Semiconductor switching devices Q_3, Q_4, D_3, and D_4 form an auxiliary four-quadrant switch that turns on to initiate the resonant commutation process.

Typical commutation waveforms are illustrated in Fig. 20.42(a), for the case in which the ac load current i_a is positive. Diode D_2 is initially conducting the output current i_a. It is desired to turn off D_2 and turn on Q_1, with zero-voltage switching. This is accomplished with the following sequence:

Interval 1. Turn on transistor Q_3. Devices D_2, Q_3, and D_4 conduct.

Interval 2. When the current in D_2 reaches zero, D_2 turns off. A resonant ringing interval occurs.

Interval 3. When the voltage v_{an} reaches $V_g/2$, diode D_1 begins to become forward-biased. Transistor Q_1 is then immediately turned on at zero voltage.

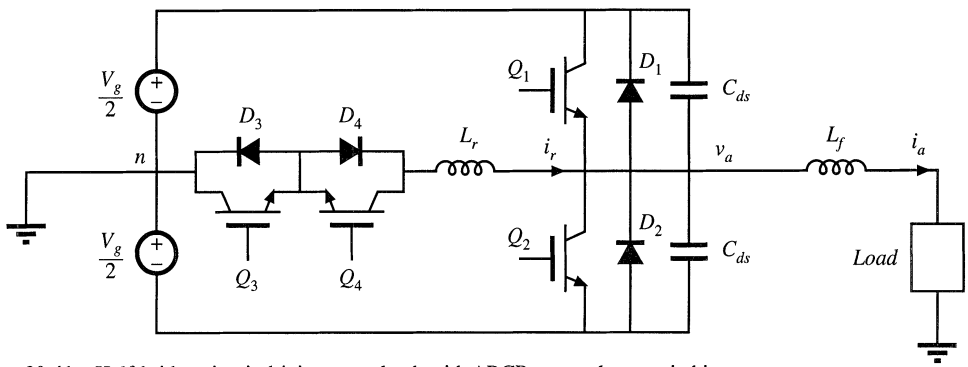

Fig. 20.41 Half-bridge circuit driving an ac load, with ARCP zero-voltage switching.

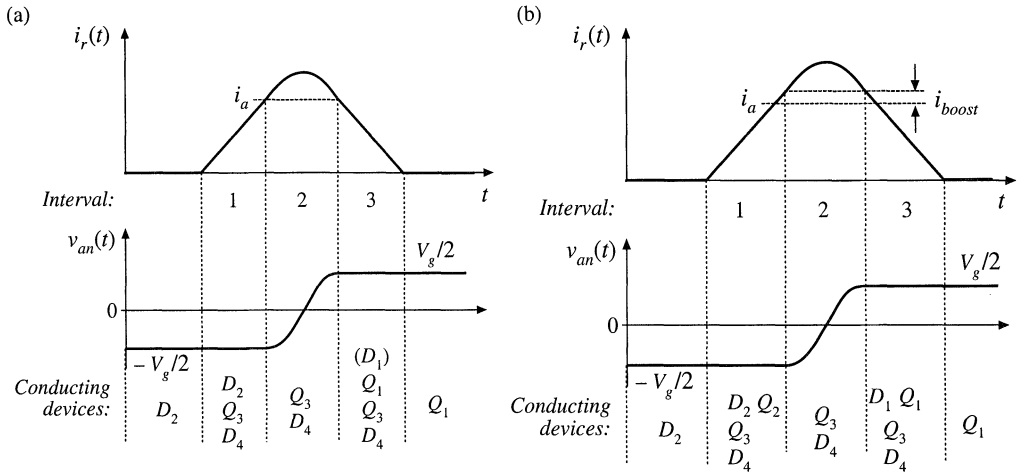

Fig. 20.42 Waveforms of the ARCP circuit of Fig. 20.41: (a) basic waveforms, (b) with current boost.

At the conclusion of interval 3, $i_r(t)$ reaches zero and diode D_3 turns off. For negative current, the process for commutation of diode D_1 is similar, except that transistor Q_4 and diode D_3 conduct the resonant current $i_r(t)$.

One issue related to the waveforms of Fig. 20.42(a) is that the circuit always operates at the boundary of zero-voltage switching. At the end of interval 2, diode D_1 is not actually forward-biased, because its current never actually becomes positive. Instead, transistor Q_1 should be turned on at the beginning of interval 3. If transistor Q_1 is gated on late, then the continued ringing will cause voltage $v_{an}(t)$ to decrease, and zero-voltage switching will be lost.

To further assist in the zero-voltage switching commutation process, transistor Q_2 can be turned on while D_2 conducts, as illustrated in Fig. 20.42(b). Transistor Q_2 is used to lengthen the duration of interval 1: now, when the current $i_r(t)$ exceeds current i_a by an amount i_{boost}, then the controller turns off Q_2 to end interval 1. This causes diode D_1 to become forward-biased during the beginning of interval 3. Transistor Q_1 is then turned on with zero-voltage switching, while D_1 is conducting.

Regardless of whether the circuit operates with the waveforms of Fig. 20.42(a) or (b), the ARCP approach eliminates the switching loss caused by the reverse recovery of diodes D_1 and D_2. Unlike the previous circuits of this chapter, the ARCP has no circulating currents that cause conduction loss, because the tank inductor current $i_r(t)$ is nonzero only in the vicinity of the commutation interval. The approach of Fig. 20.42(a) does not completely eliminate the loss caused by the device output capacitances. This loss is eliminated using the current boost of Fig. 20.42(b), but additional conduction loss is incurred because of the increased peak $i_r(t)$. The waveforms of Fig. 20.42(b) may, in fact, lead to reduced efficiency relative to Fig. 20.42(a)!

20.5 SUMMARY OF KEY POINTS

1. In a resonant switch converter, the switch network of a PWM converter is replaced by a switch network containing resonant elements. The resulting hybrid converter combines the properties of the resonant switch network and the parent PWM converter.

2. Analysis of a resonant or soft-switching switch cell involves determination of the switch conversion ratio μ. The resonant switch waveforms are determined, and are then averaged. The switch conversion ratio μ is

a generalization of the PWM CCM duty cycle d. The results of the averaged analysis of PWM converters operating in CCM can be directly adapted to the related resonant switch converter, simply by replacing d with μ.

3. In the zero-current-switching quasi-resonant switch, diode D_2 operates with zero-voltage switching, while transistor Q_1 and diode D_1 operate with zero-current switching. In the zero-voltage-switching quasi-resonant switch, the transistor Q_1 and diode D_1 operate with zero-voltage switching, while diode D_2 operates with zero-current switching.

4. In the zero-voltage-switching multiresonant switch, all semiconductor devices operate with zero-voltage switching. In consequence, very low switching loss is observed.

5. In the quasi-square-wave zero-voltage-switching resonant switches, all semiconductor devices operate with zero-voltage switching, and with peak voltages equal to those of the parent PWM converter. The switch conversion ratio is restricted to the range $0.5 \leq \mu \leq 1$. Versions containing synchronous rectifiers can operate with values of μ approaching zero.

6. The zero-voltage transition approach, as well as the active-clamp snubber approach, lead to zero-voltage switching of the transistors and zero-current switching of the diodes. These approaches have been successful in substantially improving the efficiencies of transformer-isolated converters. The auxiliary resonant commutated pole induces zero-voltage switching in bridge circuits such as the voltage-source inverter.

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PROBLEMS

20.1 In the forward converter of Fig. 20.43, L and C are large filter elements while L_p, L_s, and C_r have relatively small values. The transformer reset mechanism is not shown; for this problem, you may assume that the transformer is ideal.

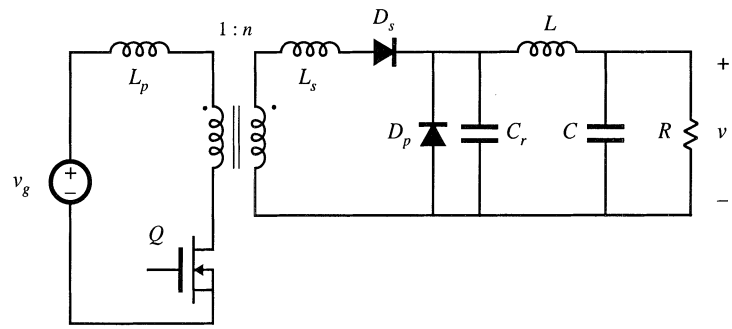

Fig. 20.43 Forward converter with resonant switch, Problem 20.1.

(a) Classify the resonant switch.

(b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?

(c) What is the resonant frequency?

20.2 In the high-voltage converter of Fig. 20.44, capacitor C is relatively large in value. The transformer model includes an ideal $1{:}n$ transformer, in conjunction with magnetizing inductance L_{mp} (referred to the primary side) and winding capacitance C_{ws} (referred to the secondary side). Transistor Q and diode D_p exhibit total output capacitance C_p, while the output capacitance of diode D_s is C_s. Other nonidealities, such as transformer leakage inductance, can be ignored. The resonant switch is well-designed, such that all elements listed above contribute to ideal operation of the converter and resonant switch.

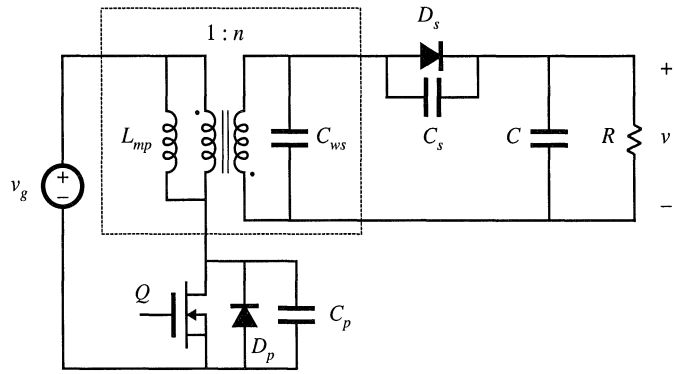

Fig. 20.44 High-voltage dc–dc converter containing a resonant switch network, Problem 20.2.

(a) What type of resonant switch is employed? What is the parent PWM converter?

(b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?

(c) What is the tank resonant frequency?

(d) Sketch the waveforms of the transistor drain-to-source voltage and transformer magnetizing current.

20.3 In the transformer-isolated dc–dc converter of Fig. 20.45, capacitors C_1 and C_2 and inductors L_1 and L_M are relatively large in value, so that they have small switching ripples. The transformer model includes an ideal $1{:}n$ transformer, in conjunction with magnetizing inductance L_M (referred to the primary side) and leakage inductances $L_{\ell 1}$ and $L_{\ell 2}$ as shown. Transistor Q_1 exhibits output capacitances C_{ds}, while the output capacitance of diode D_1 is C_d. MOSFET Q_1 contains a body diode (not explicitly shown). Other nonidealities can be ignored. The resonant switch is well-designed, such that all elements listed above contribute to ideal operation of the converter and resonant switch.

(a) What type of resonant switch is employed? What is the parent PWM converter?

(b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?

20.4 A buck-boost converter is realized using a half-wave ZCS quasi-resonant switch. The load resistance has value R, the input voltage has value V_g, and the converter switching frequency is f_s.

(a) Sketch the circuit schematic.

(b) Write the complete system of equations that can be solved to determine the output voltage V, in terms of the quantities listed above and the component values. It is not necessary to actually solve your equations. You may also quote results listed in this textbook.

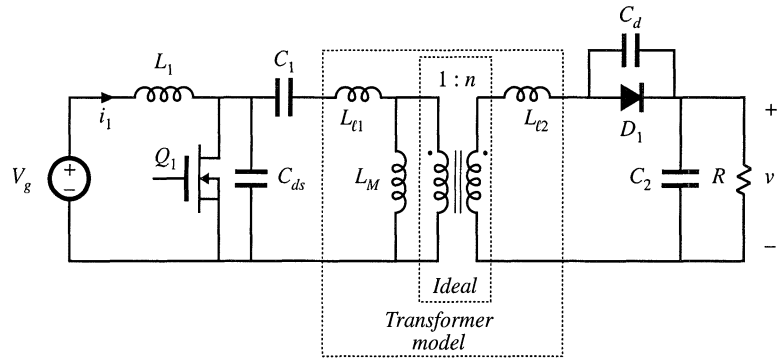

Fig. 20.45 Transformer-isolated dc–dc converter containing a resonant switch network, Problem 20.3.

20.5 It is desired to design a half-wave zero-current-switching quasi-resonant forward converter to operate with the following specifications: $V_g = 320$ V, $V = 42$ V, 5 W $\leq P \leq$ 100 W. Design the converter to operate with a maximum switching frequency of 1 MHz and a switch conversion ratio of $\mu = 0.45$. Attempt to minimize the peak transistor current, while maintaining zero current switching at all operating points. You may neglect the transformer magnetizing current, and ignore the transformer reset scheme.

(a) Specify your choices for the turns ratio n, and the tank elements L_r and C_r, referred to the transformer secondary side.

(b) For your design of part (a), what is the minimum switching frequency?

(c) What is the worst-case peak transistor current?

20.6 Analysis of the ZVS quasi-resonant switch of Fig. 20.24.

(a) For each subinterval, sketch the resonant switch cell circuit, and derive expressions for the tank inductor current and capacitor voltage waveforms.

(b) For subinterval 2, in which Q_1/D_1 are off and D_2 conducts, write the loop equation which relates the tank capacitor voltage, tank inductor voltage, and any other network voltages as appropriate. Hence, for subinterval 2 relate the integral of the tank capacitor voltage to the change in tank inductor current.

(c) Determine the switch-network terminal-waveform average values, and hence derive an expression for the switch conversion ratio μ. Verify that your result coincides with Eq. (20.61).

20.7 Analysis of the full-bridge zero-voltage transition converter of Section 20.4.1. The converter of Fig. 20.36 operates with the waveforms illustrated in Fig. 20.38. According to Eq. (20.68), the conversion ratio of this converter is given approximately by $M(\phi) = n\phi$.

Derive an exact expression for M, based on the waveforms given in Fig. 20.38. Your result should be a function of the length of subinterval 4, the load current, the switching frequency, and the values of the inductance and capacitances. *Note*: there is a reasonably simple answer to this question.