5

The Discontinuous Conduction Mode

When the ideal switches of a dc-dc converter are implemented using current-unidirectional and/or voltage-unidirectional semiconductor switches, one or more new modes of operation known as *discontinuous conduction modes* (DCM) can occur. The discontinuous conduction mode arises when the switching ripple in an inductor current or capacitor voltage is large enough to cause the polarity of the applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch with semiconductor devices are violated. The DCM is commonly observed in dc–dc converters and rectifiers, and can also sometimes occur in inverters or in other converters containing two-quadrant switches.

The discontinuous conduction mode typically occurs with large inductor current ripple in a converter operating at light load and containing current-unidirectional switches. Since it is usually required that converters operate with their loads removed, DCM is frequently encountered. Indeed, some converters are purposely designed to operate in DCM for all loads.

The properties of converters change radically in the discontinuous conduction mode. The conversion ratio M becomes load-dependent, and the output impedance is increased. Control of the output may be lost when the load is removed. We will see in a later chapter that the converter dynamics are also significantly altered.

In this chapter, the origins of the discontinuous conduction mode are explained, and the mode boundary is derived. Techniques for solution of the converter waveforms and output voltage are also described. The principles of inductor volt-second balance and capacitor charge balance must always be true in steady state, regardless of the operating mode. However, application of the small ripple approximation requires some care, since the inductor current ripple (or one of the inductor current or capacitor voltage ripples) is not small.

Buck and boost converters are solved as examples. Characteristics of the basic buck, boost, and buck-boost converters are summarized in tabular form.

R. W. Erickson et al., *Fundamentals of Power Electronics*

5.1 ORIGIN OF THE DISCONTINUOUS CONDUCTION MODE, AND MODE BOUNDARY

Let us consider how the inductor and switch current waveforms change as the load power is reduced. Let's use the buck converter (Fig. 5.1) as a simple example. The inductor current $i_L(t)$ and diode current $i_D(t)$ waveforms are sketched in Fig. 5.2 for the continuous conduction mode. As described in Chapter 2, the inductor current waveform contains a dc component I, plus switching ripple of peak amplitude Δi_L. During the second subinterval, the diode current is identical to the inductor current. The minimum diode current during the second subinterval is equal to $(I - \Delta i_L)$; since the diode is a single-quadrant switch, operation in the continuous conduction mode requires that this current remain positive. As shown in Chapter 2, the inductor current dc component I is equal to the load current:

$$I = \frac{V}{R} \tag{5.1}$$

since no dc current flows through capacitor C. It can be seen that I depends on the load resistance R. The

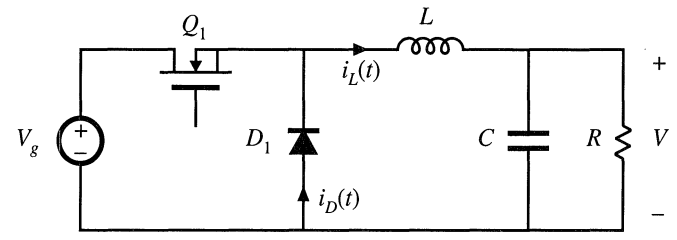

Fig. 5.1 Buck converter example.

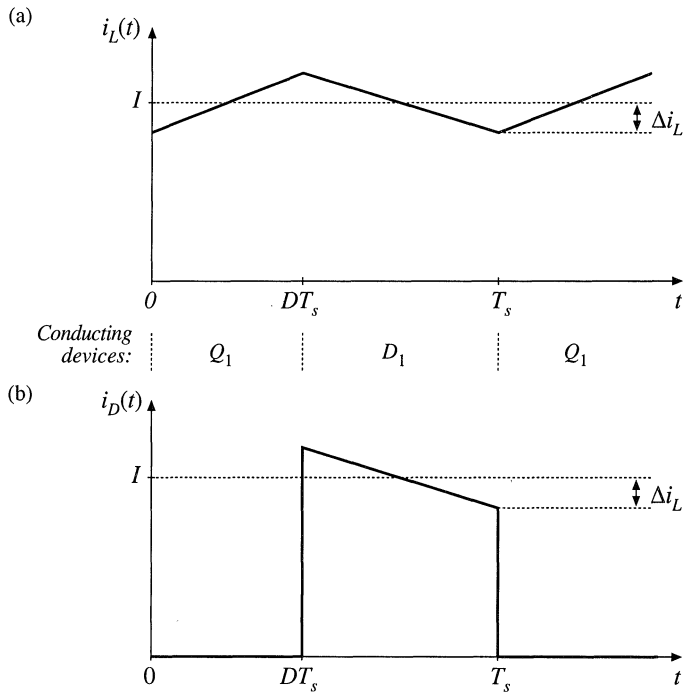

Fig. 5.2 Buck converter waveforms in the continuous conduction mode: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$.

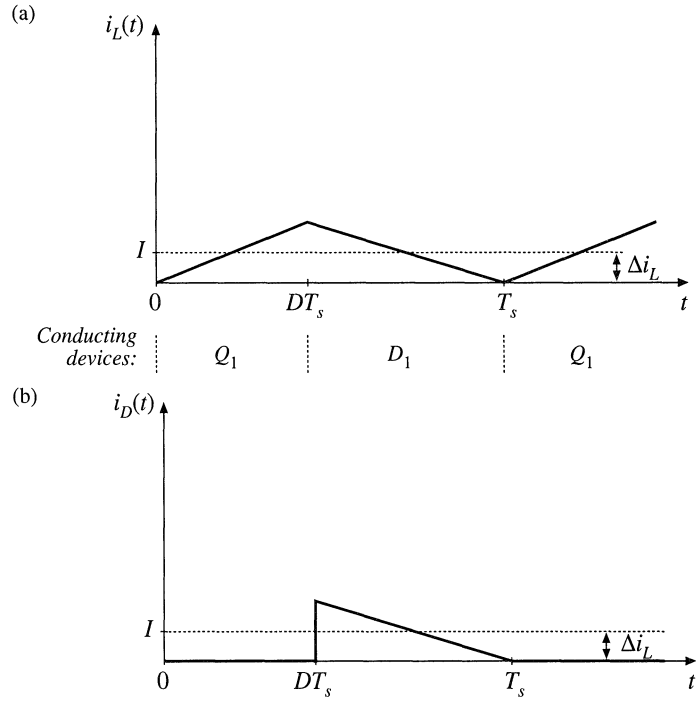

Fig. 5.3 Buck converter waveforms at the boundary between the continuous and discontinuous conduction modes: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$.

switching ripple peak amplitude is:

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L} \tag{5.2}$$

The ripple magnitude depends on the applied voltage $(V_g - V)$, on the inductance L, and on the transistor conduction time DT_s. But it does not depend on the load resistance R. The inductor current ripple magnitude varies with the applied voltages rather than the applied currents.

Suppose now that the load resistance R is increased, so that the dc load current is decreased. The dc component of inductor current I will then decrease, but the ripple magnitude Δi_L will remain unchanged. If we continue to increase R, eventually the point is reached where $I = \Delta i_L$, illustrated in Fig. 5.3. It can be seen that the inductor current $i_L(t)$ and the diode current $i_D(t)$ are both zero at the end of the switching period. Yet the load current is positive and nonzero.

What happens if we continue to increase the load resistance R? The diode current cannot be negative; therefore, the diode must become reverse-biased before the end of the switching period. As illustrated in Fig. 5.4, there are now three subintervals during each switching period T_s. During the first subinterval of length D_1T_s the transistor conducts, and the diode conducts during the second subinterval of length D_2T_s. At the end of the second subinterval the diode current reaches zero, and for the remainder of the switching period neither the transistor nor the diode conduct. The converter operates in the discontinuous conduction mode.

Figure 5.3 suggests a way to find the boundary between the continuous and discontinuous conduction modes. It can be seen that, for this buck converter example, the diode current is positive over the entire interval $DT_s < t < T_s$ provided that $I > \Delta i_L$. Hence, the conditions for operation in the continuous and discontinuous conduction modes are:

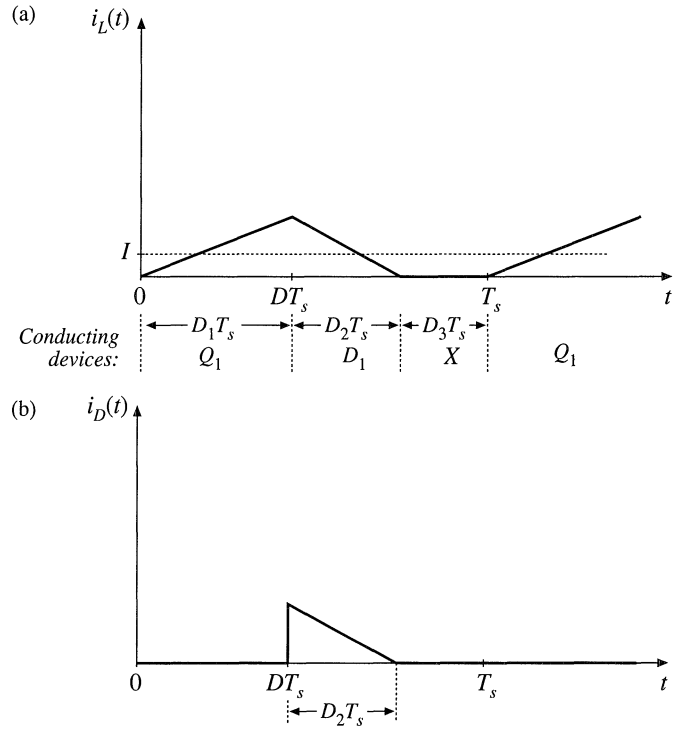

Fig. 5.4 Buck converter waveforms in the discontinuous conduction mode: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$.

$$\begin{aligned} I &> \Delta i_L \quad \text{for CCM} \\ I &< \Delta i_L \quad \text{for DCM} \end{aligned} \tag{5.3}$$

where I and Δi_L are found assuming that the converter operates in the continuous conduction mode. Insertion of Eqs. (5.1) and (5.2) into Eq. (5.3) yields the following condition for operation in the discontinuous conduction mode:

$$\frac{DV_g}{R} < \frac{DD'T_sV_g}{2L} \tag{5.4}$$

Simplification leads to

$$\frac{2L}{RT_s} < D' \tag{5.5}$$

This can also be expressed

$$K < K_{crit}(D) \quad \text{for DCM} \tag{5.6}$$

where

$$K = \frac{2L}{RT_s} \qquad \text{and} \qquad K_{crit}(D) = D'$$

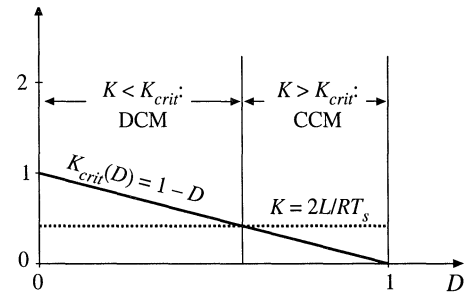

Fig. 5.5 Buck converter $K_{crit}(D)$ vs. D. The converter operates in CCM when $K > K_{crit}$, and in DCM when $K < K_{crit}$.

The dimensionless parameter K is a measure of the tendency of a converter to operate in the discontinuous conduction mode. Large values of K lead to continuous mode operation, while small values lead to the discontinuous mode for some values of duty cycle. The critical value of K at the boundary between modes, $K_{crit}(D)$, is a function of duty cycle, and is equal to D' for the buck converter.

The critical value $K_{crit}(D)$ is plotted vs. duty cycle D in Fig. 5.5. An arbitrary choice of K is also illustrated. For the values shown, it can be seen that the converter operates in DCM at low duty cycle, and in CCM at high duty cycle. Figure 5.6 illustrates what happens with heavier loading. The load resistance R is reduced in value, such that K is larger. If K is greater than one, then the converter operates in the continuous conduction mode for all duty cycles.

It is natural to express the mode boundary in terms of the load resistance R, rather than the dimensionless parameter K. Equation (5.6) can be rearranged to directly expose the dependence of the mode boundary on the load resistance:

$$\begin{aligned} R &< R_{crit}(D) \quad \text{for CCM} \\ R &> R_{crit}(D) \quad \text{for DCM} \end{aligned} \tag{5.7}$$

where

$$R_{crit}(D) = \frac{2L}{D'T_s}$$

So the converter enters the discontinuous conduction mode when the load resistance R exceeds the critical value R_{crit}. This critical value depends on the inductance, the switching period, and the duty cycle. Note that, since $D' \leq 1$, the minimum value of R_{crit} is $2L/T_s$. Therefore, if $R < 2L/T_s$, then the converter will operate in the continuous conduction mode for all duty cycles.

These results can be applied to loads that are not pure linear resistors. An effective load resis-

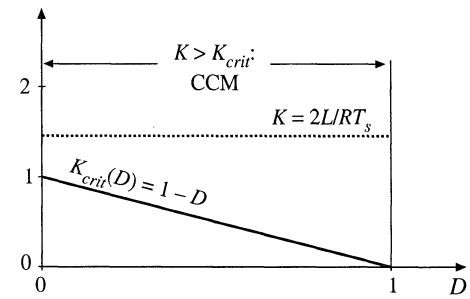

Fig. 5.6 Comparison of K with $K_{crit}(D)$, for a larger value of K. Since $K > 1$, the converter operates in CCM for all D.

Table 5.1 CCM-DCM mode boundaries for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0 \le D \le 1} (K_{crit})$	$R_{crit}(D)$	$\min_{0 \le D \le 1} (R_{crit})$
Buck	$(1-D)$	1	$\frac{2L}{(1-D)T_s}$	$2\frac{L}{T_s}$
Boost	$D(1-D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1-D)^2 T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck–boost	$(1-D)^2$	1	$\frac{2L}{(1-D)^2 T_s}$	$2\frac{L}{T_s}$

tance R is defined as the ratio of the dc output voltage to the dc load current: $R = V/I$. This effective load resistance is then used in the above equations.

A similar mode boundary analysis can be performed for other converters. The boost converter is analyzed in Section 5.3, while analysis of the buck-boost converter is left as a homework problem. The results are listed in Table 5.1, for the three basic dc–dc converters. In each case, the dimensionless parameter K is defined as $K = 2L/RT_s$, and the mode boundary is given by

$$\begin{aligned} K &> K_{crit}(D) \quad \text{or} \quad R < R_{crit}(D) \quad \text{for CCM} \\ K &< K_{crit}(D) \quad \text{or} \quad R > R_{crit}(D) \quad \text{for DCM} \end{aligned} \tag{5.8}$$

5.2 ANALYSIS OF THE CONVERSION RATIO $M(D, K)$

With a few modifications, the same techniques and approximations developed in Chapter 2 for the steady-state analysis of the continuous conduction mode may be applied to the discontinuous conduction mode.

(a) *Inductor volt-second balance.* The dc component of the voltage applied to an inductor must be zero:

$$\langle v_L \rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t)dt = 0 \tag{5.9}$$

(b) *Capacitor charge balance.* The dc component of current applied to a capacitor must be zero:

$$\langle i_C \rangle = \frac{1}{T_s} \int_0^{T_s} i_C(t)dt = 0 \tag{5.10}$$

These principles must be true for any circuit that operates in steady state, regardless of the operating mode.

(c) *The linear ripple approximation.* Care must be used when employing the linear ripple approximation in the discontinuous conduction mode.

(*i*) *Output capacitor voltage ripple.* Regardless of the operating mode, it is required that the output voltage ripple be small. Hence, for a well-designed converter operating in the discontinuous conduction mode, the peak output voltage ripple Δv should be much smaller in magnitude than the output voltage dc component V. So the linear ripple approximation applies to the output voltage waveform:

$$v(t) \approx V \tag{5.11}$$

(*ii*) *Inductor current ripple.* By definition, the inductor current ripple is not small in the discontinuous conduction mode. Indeed, Eq. (5.3) states that the inductor current ripple Δi_L is greater in magnitude than the dc component I. So neglecting the inductor current ripple leads to inaccurate results. In other converters, several inductor currents, or a capacitor voltage, may contain large switching ripple which should not be neglected.

The equations necessary for solution of the voltage conversion ratio can be obtained by invoking volt-second balance for each inductor voltage, and charge balance for each capacitor current, in the network. The switching ripple is ignored in the output capacitor voltage, but the inductor current switching ripple must be accounted for in this buck converter example.

Let us analyze the conversion ratio $M = V/V_g$ of the buck converter of Eq. (5.1). When the transistor conducts, for $0 < t < D_1 T_s$, the converter circuit reduces to the network of Fig. 5.7(a). The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g - v(t) \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \tag{5.12}$$

By making the linear ripple approximation, to ignore the output capacitor voltage ripple, one obtains

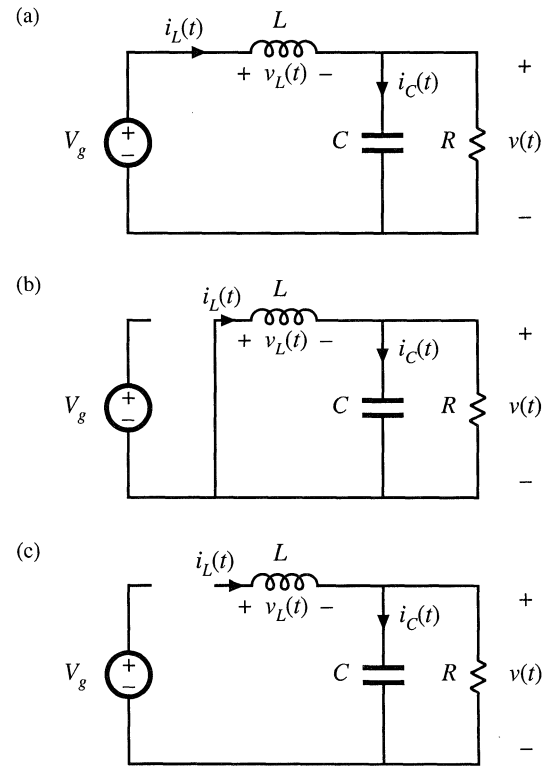

Fig. 5.7 Buck converter circuits for operation in the discontinuous conduction mode: (a) during subinterval 1, (b) during subinterval 2, (c) during subinterval 3.

$$\begin{aligned} v_L(t) &\approx V_g - V \\ i_C(t) &\approx i_L(t) - \frac{V}{R} \end{aligned} \tag{5.13}$$

Note that the inductor current ripple has not been ignored.

The diode conducts during subinterval 2, $D_1T_s < t < (D_1 + D_2)T_s$. The circuit then reduces to Fig. 5.7(b). The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= -v(t) \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \tag{5.14}$$

By neglecting the ripple in the output capacitor voltage, one obtains

$$\begin{aligned} v_L(t) &\approx -V \\ i_C(t) &\approx i_L(t) - \frac{V}{R} \end{aligned} \tag{5.15}$$

The diode becomes reverse-biased at time $t = (D_1 + D_2)T_s$. The circuit is then as shown in Fig. 5.7(c), with both transistor and diode in the off state. The inductor voltage and inductor current are both zero for the remainder of the switching period $(D_1 + D_2)T_s < t < T_s$. The network equations for the third subinterval are given by

$$\begin{aligned} v_L &= 0, \quad i_L = 0 \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \tag{5.16}$$

Note that the inductor current is constant and equal to zero during the third subinterval, and therefore the inductor voltage must also be zero in accordance with the relationship $v_L(t) = L\, di_L(t)/dt$. In practice, parasitic ringing is observed during this subinterval. This ringing occurs owing to the resonant circuit formed by the inductor and the semiconductor device capacitances, and typically has little influence on the converter steady-state properties. Again ignoring the output capacitor voltage ripple, one obtains

$$\begin{aligned} v_L(t) &= 0 \\ i_C(t) &= -\frac{V}{R} \end{aligned} \tag{5.17}$$

Equations (5.13), (5.15), and (5.17) can now be used to plot the inductor voltage waveform as in Fig. 5.8. According to the principle of inductor volt-second balance, the dc component of this waveform must be zero. Since the waveform is rectangular, its dc component (or average value) is easily evaluated:

$$\langle v_L(t) \rangle = D_1\left(V_g - V\right) + D_2\left(-V\right) + D_3\left(0\right) = 0 \tag{5.18}$$

Solution for the output voltage yields

$$V = V_g \frac{D_1}{D_1 + D_2} \tag{5.19}$$

The transistor duty cycle D (which coincides with the subinterval 1 duty cycle D_1) is the control input to the converter, and can be considered known. But the subinterval 2 duty cycle D_2 is unknown, and hence

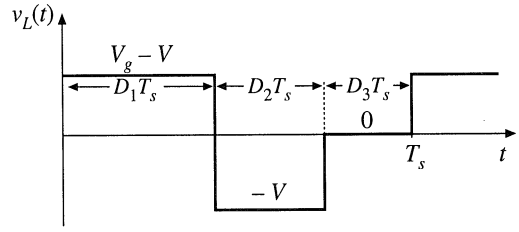

Fig. 5.8 Inductor voltage waveform $v_L(t)$, buck converter operating in discontinuous conduction mode.

another equation is needed to eliminate D_2 and solve for the output voltage V.

The second equation is obtained by use of capacitor charge balance. The connection of the capacitor to its adjacent components is detailed in Fig. 5.9. The node equation of this network is

$$i_L(t) = i_C(t) + \frac{v(t)}{R} \tag{5.20}$$

By capacitor charge balance, the dc component of capacitor current must be zero:

$$\langle i_C \rangle = 0 \tag{5.21}$$

Therefore, the dc load current must be supplied entirely by the other elements connected to the node. In particular, for the case of the buck converter, the dc component of inductor current must be equal to the dc load current:

$$\langle i_L \rangle = \frac{V}{R} \tag{5.22}$$

So we need to compute the dc component of the inductor current.

Since the inductor current ripple is not small, determination of the inductor current dc component requires that we examine the current waveform in detail. The inductor current waveform is sketched in Fig. 5.10. The current begins the switching period at zero, and increases during the first subinterval with a constant slope, given by the applied voltage divided by the inductance. The peak inductor current i_{pk} is equal to the constant slope, multiplied by the length of the first subinterval:

$$i_L(D_1T_s) = i_{pk} = \frac{V_g - V}{L} D_1T_s \tag{5.23}$$

The dc component of the inductor current is again the average value:

$$\langle i_L \rangle = \frac{1}{T_s} \int_0^{T_s} i_L(t)\,dt \tag{5.24}$$

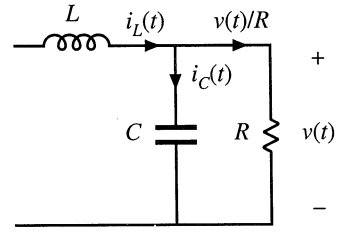

Fig. 5.9 Connection of the output capacitor to adjacent components.

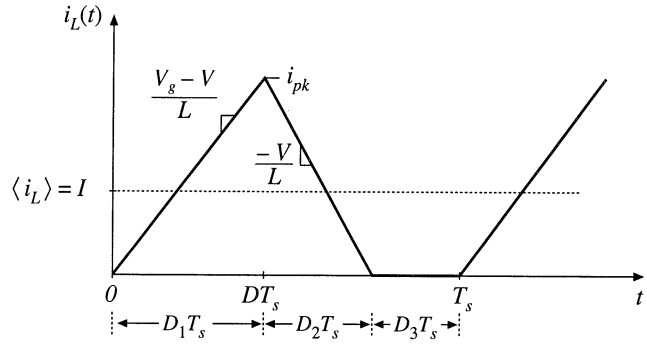

Fig. 5.10 Inductor current waveform $i_L(t)$, buck converter operating in discontinuous conduction mode.

The integral, or area under the iL(t) curve, is the area of the triangle having height i_{pk} and base dimension $(D_1 + D_2)T_s$. Use of the triangle area formula yields

$$\int_0^{T_s} i_L(t)dt = \tfrac{1}{2} i_{pk}\left(D_1 + D_2\right)T_s \tag{5.25}$$

Substitution of Eqs. (5.23) and (5.25) into Eq. (5.24) leads to

$$\langle i_L \rangle = \left(V_g - V\right)\left(\frac{D_1 T_s}{2L}\right)\left(D_1 + D_2\right) \tag{5.26}$$

Finally, by equating this result to the dc load current, according to Eq. (5.22), we obtain

$$\frac{V}{R} = \frac{D_1 T_s}{2L}\left(D_1 + D_2\right)\left(V_g - V\right) \tag{5.27}$$

Thus, we have two unknowns, V and D_2, and we have two equations. The first equation, Eq. (5.19), was obtained by inductor volt-second balance, while the second equation, Eq. (5.27), was obtained using capacitor charge balance. Elimination of D_2 from the two equations, and solution for the voltage conversion ratio $M(D_1, K) = V/V_g$, yields

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + \dfrac{4K}{D_1^2}}} \tag{5.28}$$

where $K = 2L/RT_s$

valid for $K < K_{crit}$

This is the solution of the buck converter operating in discontinuous conduction mode.

The complete buck converter characteristics, including both continuous and discontinuous conduction modes, are therefore

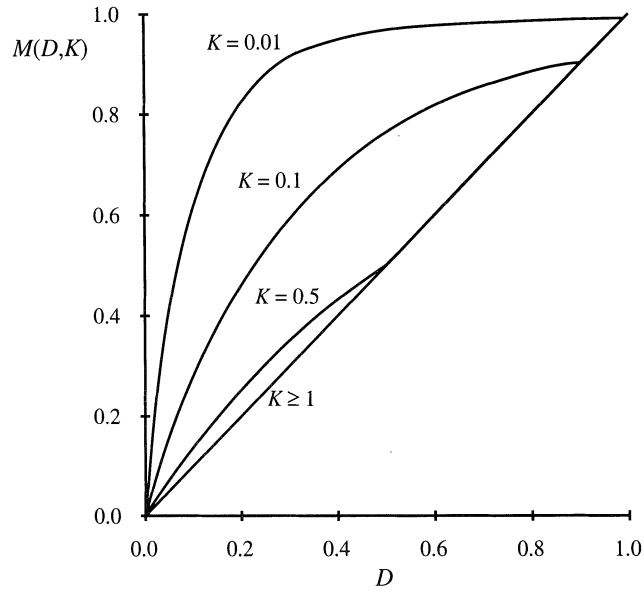

Fig. 5.11 Voltage conversion ratio $M(D, K)$, buck converter.

$$M = \begin{cases} D & \text{for } K > K_{crit} \\ \dfrac{2}{1 + \sqrt{1 + \dfrac{4K}{D^2}}} & \text{for } K < K_{crit} \end{cases} \tag{5.29}$$

where the transistor duty cycle D is identical to the subinterval 1 duty cycle D_1 of the above derivation. These characteristics are plotted in Fig. 5.11, for several values of K. It can be seen that the effect of the discontinuous conduction mode is to cause the output voltage to increase. As K tends to zero (the unloaded case), M tends to unity for all nonzero D. The characteristics are continuous, and Eq. (5.28) intersects the CCM characteristic $M = D$ at the mode boundary.

5.3 BOOST CONVERTER EXAMPLE

As a second example, consider the boost converter of Fig. 5.12. Let's determine the boundary between modes, and solve for the conversion ratio in the discontinuous conduction mode. Behavior of the boost converter operating in the continuous conduction mode was analyzed previously, in Section 2.3, and expressions for the inductor current dc component I and ripple peak magnitude Δi_L were found.

When the diode conducts, its current is identical to the inductor current $i_L(t)$. As can be seen from Fig. 2.18, the minimum value of the inductor current during the diode conduction subinterval $DT_s < t < T_s$ is $(I - \Delta i_L)$. If this minimum current is positive, then the diode is forward-biased for the entire subinterval $DT_s < t < T_s$, and the converter operates in the continuous conduction mode. So the conditions for operation of the boost converter in the continuous and discontinuous conduction modes are:

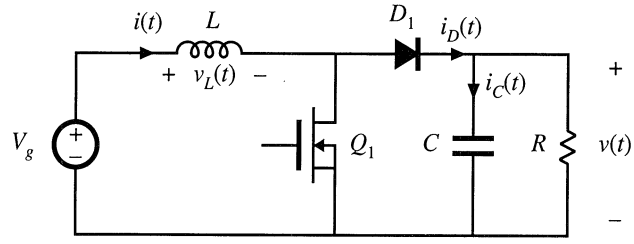

Fig. 5.12 Boost converter example.

$$\begin{aligned} I &> \Delta i_L \quad \text{for CCM} \\ I &< \Delta i_L \quad \text{for DCM} \end{aligned} \tag{5.30}$$

which is identical to the results for the buck converter. Substitution of the CCM solutions for I and Δi_L, Eqs. (2-39) and (2-43), yields

$$\frac{V_g}{D'^2 R} > \frac{DT_s V_g}{2L} \quad \text{for CCM} \tag{5.31}$$

This equation can be rearranged to obtain

$$\frac{2L}{RT_s} > DD'^2 \quad \text{for CCM} \tag{5.32}$$

which is in the standard form

$$\begin{aligned} K &> K_{crit}(D) \quad \text{for CCM} \\ K &< K_{crit}(D) \quad \text{for DCM} \end{aligned} \tag{5.33}$$

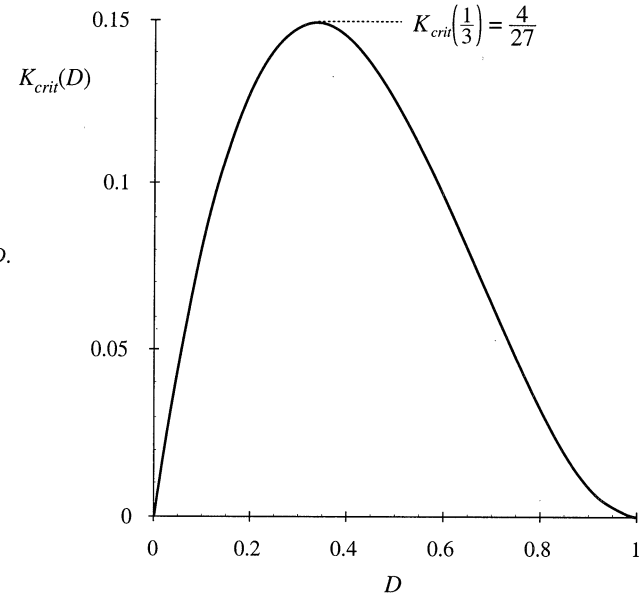

Fig. 5.13 Boost converter $K_{crit}(D)$ vs. D.

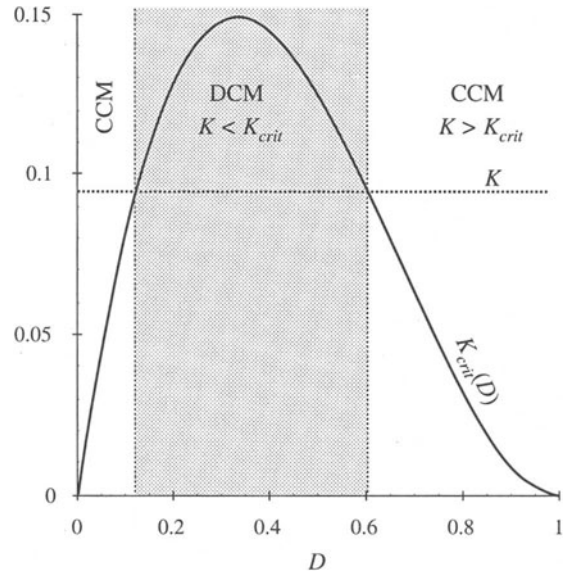

Fig. 5.14 Comparison of K with $K_{crit}(D)$.

where

$$K = \frac{2L}{RT_s} \quad \text{and} \quad K_{crit}(D) = DD'^2$$

The conditions for operation in the continuous or discontinuous conduction modes are of similar form to those for the buck converter; however, the critical value $K_{crit}(D)$ is a different function of the duty cycle D. The dependence of $K_{crit}(D)$ on the duty cycle D is plotted in Fig. 5.13. $K_{crit}(D)$ is zero at $D = 0$ and at $D = 1$, and has a maximum value of 4/27 at $D = 1/3$. Hence, if K is greater than 4/27, then the converter operates in the continuous conduction mode for all D. Figure 5.14 illustrates what happens when K is less than 4/27. The converter then operates in the discontinuous conduction mode for some intermediate range of values of D near $D = 1/3$. But the converter operates in the continuous conduction mode near $D = 0$ and $D = 1$. Unlike the buck converter, the boost converter must operate in the continuous conduction mode near $D = 0$ because the ripple magnitude approaches zero while the dc component I does not.

Next, let us analyze the conversion ratio $M = V/V_g$ of the boost converter. When the transistor conducts, for the subinterval $0 < t < D_1T_s$, the converter circuit reduces to the circuit of 5.15(a). The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g \\ i_C(t) &= -\frac{v(t)}{R} \end{aligned} \tag{5.34}$$

Use of the linear ripple approximation, to ignore the output capacitor voltage ripple, leads to

$$\begin{aligned} v_L(t) &\approx V_g \\ i_C(t) &\approx -\frac{V}{R} \end{aligned} \tag{5.35}$$

During the second subinterval $D_1T_s < t < (D_1 + D_2)T_s$, the diode conducts. The circuit then reduces to

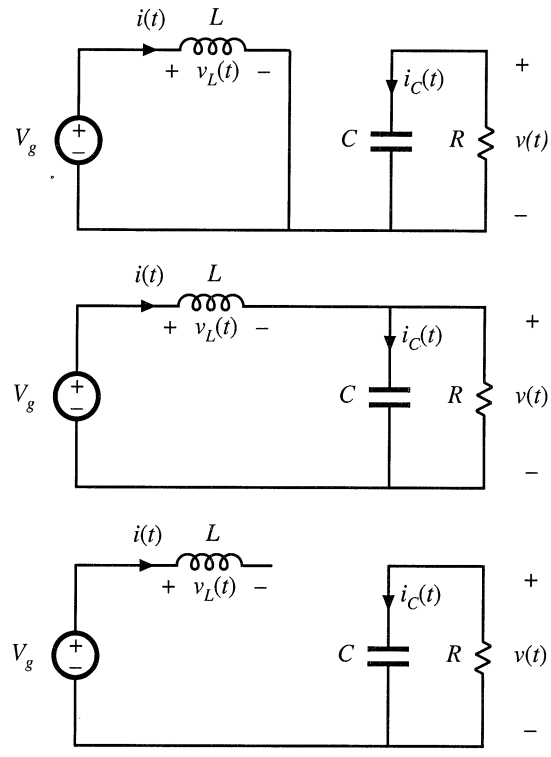

Fig. 5.15 Boost converter circuits: (a) during subinterval 1, $0 < t < D_1T_s$, (b) during subinterval 2, $D_1T_s < t < (D_1 + D_2)T_s$, (c) during subinterval 3, $(D_1 + D_2)T_s < t < T_s$.

Fig. 5.15(b). The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g - v(t) \\ i_C(t) &= i(t) - \frac{v(t)}{R} \end{aligned} \tag{5.36}$$

Neglect of the output capacitor voltage ripple yields

$$\begin{aligned} v_L(t) &\approx V_g - V \\ i_C(t) &\approx i(t) - \frac{V}{R} \end{aligned} \tag{5.37}$$

The inductor current ripple has not been neglected.

During the third subinterval, $(D_1 + D_2)T_s < t < T_s$, both transistor and diode are in the off state, and Fig. 5.15(c) is obtained. The network equations are:

$$\begin{aligned} v_L &= 0, \quad i = 0 \\ i_C(t) &= -\frac{v(t)}{R} \end{aligned} \tag{5.38}$$

Use of the small-ripple approximation yields

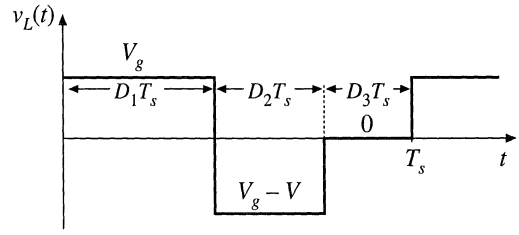

Fig. 5.16 Inductor voltage waveform $v_L(t)$, boost converter operating in discontinuous conduction mode.

$$\begin{aligned} v_L(t) &= 0 \\ i_C(t) &= -\frac{V}{R} \end{aligned} \tag{5.39}$$

Equations (5.35), (5.37), and (5.39) are now used to sketch the inductor voltage waveform as in Fig. 5.16. By volt-second balance, this waveform must have zero dc component when the converter operates in steady state. By equating the average value of this $v_L(t)$ waveform to zero, one obtains

$$D_1 V_g + D_2\left(V_g - V\right) + D_3(0) = 0 \tag{5.40}$$

Solution for the output voltage V yields

$$V = \frac{D_1 + D_2}{D_2} V_g \tag{5.41}$$

The diode duty cycle D_2 is again an unknown, and so a second equation is needed for elimination of D_2 before the output voltage V can be found.

We can again use capacitor charge balance to obtain the second equation. The connection of the output capacitor to its adjacent components is detailed in Fig. 5.17. Unlike the buck converter, the diode in the boost converter is connected to the output node. The node equation of Fig. 5.17 is

$$i_D(t) = i_C(t) + \frac{v(t)}{R} \tag{5.42}$$

where $i_D(t)$ is the diode current. By capacitor charge balance, the capacitor current $i_C(t)$ must have zero dc component in steady state. Therefore, the diode current dc component $\langle i_D \rangle$ must be equal to the dc component of the load current:

$$\langle i_D \rangle = \frac{V}{R} \tag{5.43}$$

So we need to sketch the diode current waveform, and find its dc component.

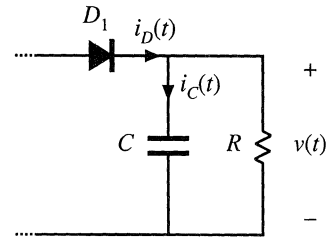

Fig. 5.17 Connection of the output capacitor to adjacent components in the boost converter.

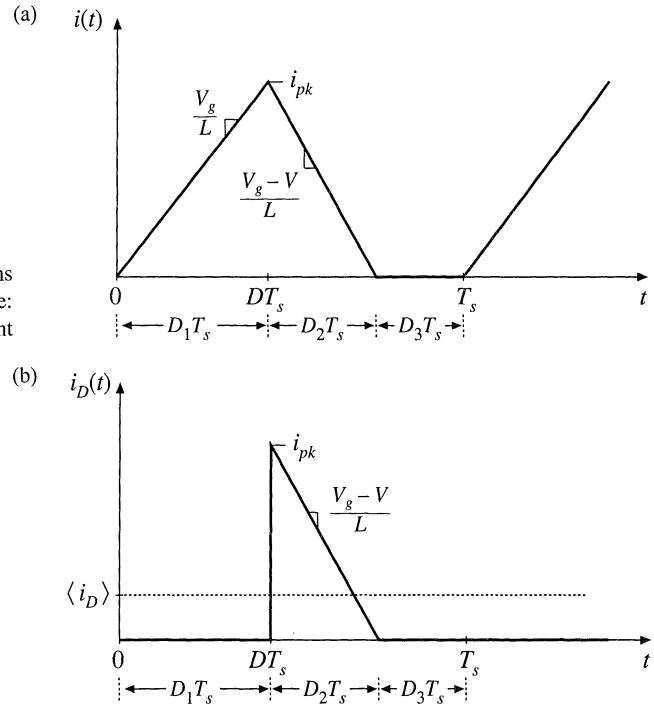

Fig. 5.18 Boost converter waveforms in the discontinuous conduction mode: (a) inductor current $i(t)$, (b) diode current $i_D(t)$.

The waveforms of the inductor current $i(t)$ and diode current $i_D(t)$ are illustrated in Fig. 5.18. The inductor current begins at zero, and rises to a peak value i_{pk} during the first subinterval. This peak value i_{pk} is equal to the slope V_g/L, multiplied by the length of the first subinterval, D_1T_s:

$$i_{pk} = \frac{V_g}{L} D_1 T_s \tag{5.44}$$

The diode conducts during the second subinterval, and the inductor current then decreases to zero, where it remains during the third subinterval. The diode current $i_D(t)$ is identical to the inductor current $i(t)$ during the second subinterval. During the first and third subintervals, the diode is reverse-biased and hence $i_D(t)$ is zero.

The dc component of the diode current, $\langle i_D \rangle$, is:

$$\langle i_D \rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t) dt \tag{5.45}$$

The integral is the area under the $i_D(t)$ waveform. As illustrated in Fig. 5.18(b), this area is the area of the triangle having peak value i_{pk} and base dimension D_2T_s:

$$\int_0^{T_s} i_D(t) dt = \frac{1}{2} i_{pk} D_2 T_s \tag{5.46}$$

Substitution of Eqs. (5.44) and (5.46) into Eq. (5.45) leads to the following expression for the dc component of the diode current:

$$\langle i_D \rangle = \frac{1}{T_s}\left(\frac{1}{2} i_{pk} D_2 T_s\right) = \frac{V_g D_1 D_2 T_s}{2L} \tag{5.47}$$

By equating this expression to the dc load current as in Eq. (5.43), one obtains the final result

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R} \tag{5.48}$$

So now we have two unknowns, V and D_2. We have two equations: Eq. (5.41) obtained via inductor volt-second balance, and Eq. (5.48) obtained using capacitor charge balance. Let us now eliminate D_2 from this system of equations, and solve for the output voltage V. Solution of Eq. (5.41) for D_2 yields

$$D_2 = D_1 \frac{V_g}{V - V_g} \tag{5.49}$$

By inserting this result into Eq. (5.48), and rearranging terms, one obtains the following quadratic equation:

$$V^2 - V V_g - \frac{V_g^2 D_1^2}{K} = 0 \tag{5.50}$$

Use of the quadratic formula yields

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + \frac{4D_1^2}{K}}}{2} \tag{5.51}$$

The quadratic equation has two roots: one of the roots of Eq. (5.51) is positive, while the other is negative. We already know that the output voltage of the boost converter should be positive, and indeed, from Eq. (5.41), it can be seen that V/V_g must be positive since the duty cycles D_1 and D_2 are positive. So we should select the positive root:

$$\frac{V}{V_g} = M(D_1, K) = \frac{1 + \sqrt{1 + \frac{4D_1^2}{K}}}{2} \tag{5.52}$$

where $K = 2L/RT_s$

valid for $K < K_{crit}(D)$

This is the solution of the boost converter operating in the discontinuous conduction mode.

The complete boost converter characteristics, including both continuous and discontinuous conduction modes, are

$$M = \begin{cases} \dfrac{1}{1-D} & \text{for } K > K_{crit} \\ \dfrac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2} & \text{for } K < K_{crit} \end{cases} \tag{5.53}$$

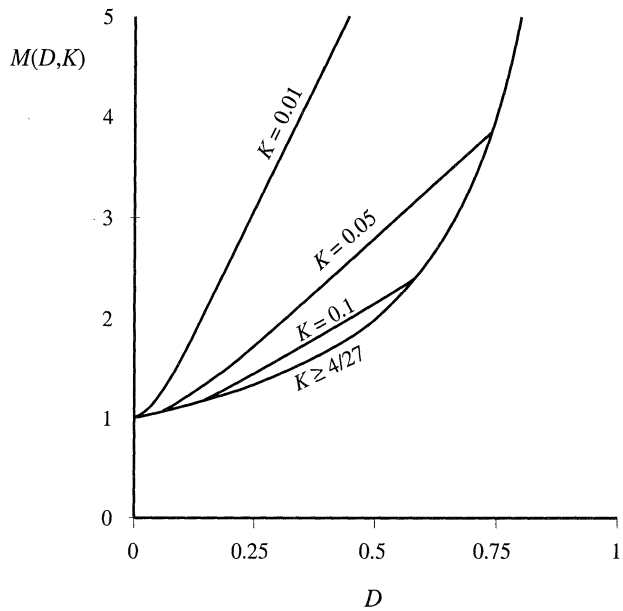

Fig. 5.19 Voltage conversion ratio $M(D, K)$ of the boost converter, including both continuous and discontinuous conduction modes

These characteristics are plotted in Fig. 5.19, for several values of K. As in the buck converter, the effect of the discontinuous conduction mode is to cause the output voltage to increase. The DCM portions of the characteristics are nearly linear, and can be approximated as

$$M \approx \frac{1}{2} + \frac{D}{\sqrt{K}} \tag{5.54}$$

5.4 SUMMARY OF RESULTS AND KEY POINTS

The characteristics of the basic buck, boost, and buck-boost are summarized in Table 5.2. Expressions for $K_{crit}(D)$, as well as for the solutions of the dc conversion ratios in CCM and DCM, and for the DCM diode conduction duty cycle D_2, are given.

The dc conversion ratios of the DCM buck, boost, and buck-boost converters are compared in

Table 5.2 Summary of CCM-DCM characteristics for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	DCM $M(D, K)$	DCM $D_2(D, K)$	CCM $M(D)$
Buck	$(1 - D)$	$\frac{2}{1 + \sqrt{1 + 4K/D^2}}$	$\frac{K}{D} M(D, K)$	D
Boost	$D(1 - D)^2$	$\frac{1 + \sqrt{1 + 4D^2/K}}{2}$	$\frac{K}{D} M(D, K)$	$\frac{1}{1 - D}$
Buck–boost	$(1 - D)^2$	$-\frac{D}{\sqrt{K}}$	$\sqrt{K}$	$-\frac{D}{1 - D}$

with $K = 2L/RT_s$, DCM occurs for $K < K_{crit}$.

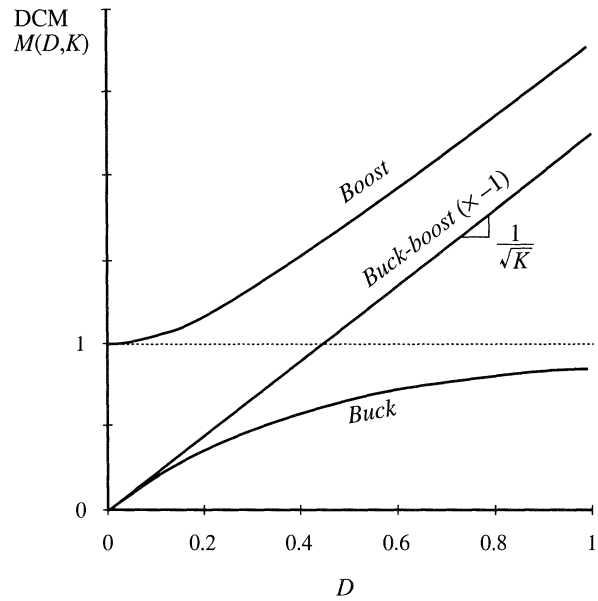

Fig. 5.20 Comparison of dc conversion ratios of the buck–boost, buck, and boost converters operated in the discontinuous conduction mode.

Fig. 5.20. The buck-boost characteristic is a line with slope $1/\sqrt{K}$. The characteristics of the buck and the boost converters are both asymptotic to this line, as well as to the line $M = 1$. Hence, when operated deeply into the discontinuous conduction mode, the boost converter characteristic becomes nearly linear with slope $1/\sqrt{K}$, especially at high duty cycle. Likewise, the buck converter characteristic becomes nearly linear with the same slope, when operated deeply into discontinuous conduction mode at low duty cycle.

The following are the key points of this chapter:

1. The discontinuous conduction mode occurs in converters containing current- or voltage-unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse polarity.
2. Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and dc components cause the switch on state current or off state voltage to reverse polarity.
3. The dc conversion ratio M of converters operating in the discontinuous conduction mode can be found by application of the principles of inductor volt-second and capacitor charge balance.
4. Extra care is required when applying the small-ripple approximation. Some waveforms, such as the output voltage, should have small ripple which can be neglected. Other waveforms, such as one or more inductor currents, may have large ripple that cannot be ignored.
5. The characteristics of a converter changes significantly when the converter enters DCM. The output voltage becomes load-dependent, resulting in an increase in the converter output impedance.

PROBLEMS

5.1 The elements of the buck-boost converter of Fig. 5.21 are ideal: all losses may be ignored. Your results for parts (a) and (b) should agree with Table 5.2.

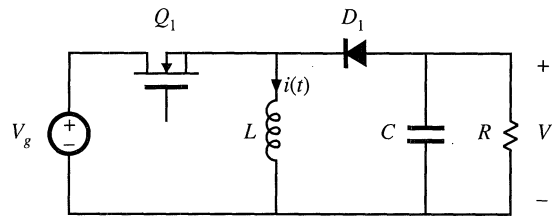

Fig. 5.21 Buck–boost converter of Problems 5.1 and 5.13.

(a) Show that the converter operates in discontinuous conduction mode when $K < K_{crit}$, and derive expressions for K and K_{crit}.

(b) Derive an expression for the dc conversion ratio V/V_g of the buck–boost converter operating in discontinuous conduction mode.

(c) For $K = 0.1$, plot V/V_g over the entire range $0 \le D \le 1$.

(d) Sketch the inductor voltage and current waveforms for $K = 0.1$ and $D = 0.3$. Label salient features.

(e) What happens to V at no load ($R \to \infty$)? Explain why, physically.

5.2 A certain buck converter contains a synchronous rectifier, as described in Section 4.1.5.

(a) Does this converter operate in the discontinuous conduction mode at light load? Explain.

(b) The load resistance is disconnected ($R \to \infty$), and the converter is operated with duty cycle 0.5. Sketch the inductor current waveform.

5.3 An unregulated dc input voltage V_g varies over the range $35\text{ V} \le V_g \le 70\text{ V}$. A buck converter reduces this voltage to 28 V; a feedback loop varies the duty cycle as necessary such that the converter output voltage is always equal to 28 V. The load power varies over the range $10\text{ W} \le P_{load} \le 1000\text{ W}$. The element values are:

$L = 22\ \mu\text{H}$ $C = 470\ \mu\text{F}$ $f_s = 75\text{ kHz}$

Losses may be ignored.

(a) Over what range of V_g and load current does the converter operate in CCM?

(b) Determine the maximum and minimum values of the steady-state transistor duty cycle.

5.4 The transistors in the converter of Fig. 5.22 are driven by the same gate drive signal, so that they turn on and off in synchronism with duty cycle D.

(a) Determine the conditions under which this converter operates in the discontinuous conduction mode, as a function of the steady-state duty ratio D

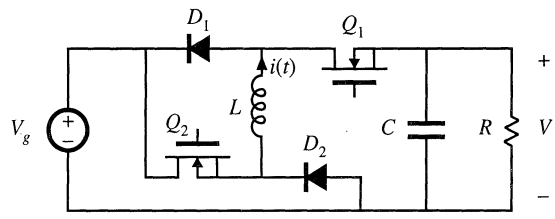

Fig. 5.22 Watkins-Johnson converter of Problem 5.4.

and the dimensionless parameter $K = 2L/RT_s$.

(b) What happens to your answer to Part (a) for $D < 0.5$?

(c) Derive an expression for the dc conversion ratio $M(D, K)$. Sketch M vs. D for $K = 10$ and for $K = 0.1$, over the range $0 \le D \le 1$.

5.5 DCM mode boundary analysis of the Ćuk converter of Fig. 5.23. The capacitor voltage ripples are small.

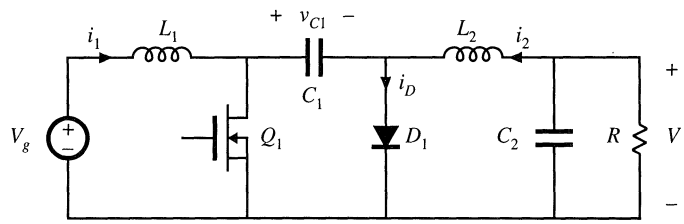

Fig. 5.23 Ćuk converter, Problems 5.5, 5.6, 5.11, and 5.12

(a) Sketch the diode current waveform for CCM operation. Find its peak value, in terms of the ripple magnitudes Δi_{L1}, Δi_{L2}, and the dc components I_1 and I_2, of the two inductor currents $i_{L1}(t)$ and $i_{L2}(t)$, respectively.

(b) Derive an expression for the conditions under which the Ćuk converter operates in the discontinuous conduction mode. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.6 DCM conversion ratio analysis of the Ćuk converter of Fig. 5.23.

(a) Suppose that the converter operates at the boundary between CCM and DCM, with the following element and parameter values:

$D = 0.4$	$f_s = 100$ kHz
$V_g = 120$ V	$R = 10\ \Omega$
$L_1 = 54\ \mu$H	$L_2 = 27\ \mu$H
$C_1 = 47\ \mu$F	$C_2 = 100\ \mu$F

Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$. Label the magnitudes of the ripples and dc components of these waveforms.

(b) Suppose next that the converter operates in the discontinuous conduction mode, with a different choice of parameter and element values. Derive an analytical expression for the dc conversion ratio $M(D, K)$.

(c) Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$, for operation in the discontinuous conduction mode.

5.7 DCM mode boundary analysis of the SEPIC of Fig. 5.24

(a) Sketch the diode current waveform for CCM operation. Find its peak value, in terms of the ripple magnitudes Δi_{L1}, Δi_{L2}, and the dc components I_1 and I_2, of the two inductor currents $i_{L1}(t)$ and $i_{L2}(t)$, respectively.

(b) Derive an expression for the conditions under which the SEPIC operates in the discontinuous conduction mode. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.8 DCM conversion ratio analysis of the SEPIC of Fig. 5.24.

(a) Suppose that the converter operates at the boundary between CCM and DCM, with the follow-

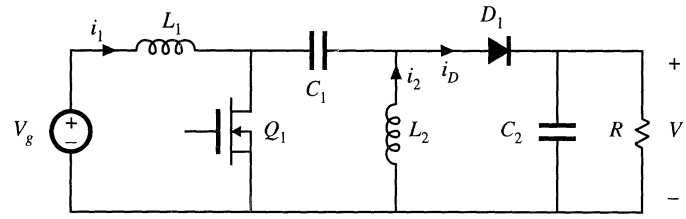

Fig. 5.24 SEPIC, Problems 5.7 and 5.8.

ing element and parameter values:

$D = 0.225$	$f_s = 100$ kHz
$V_g = 120$ V	$R = 10\ \Omega$
$L_1 = 50\ \mu$H	$L_2 = 75\ \mu$H
$C_1 = 47\ \mu$F	$C2 = 200\ \mu$F

Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$. Label the magnitudes of the ripples and dc components of these waveforms.

(b) Suppose next that the converter operates in the discontinuous conduction mode, with a different choice of parameter and element values. Derive an analytical expression for the dc conversion ratio $M(D, K)$.

(c) Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$, for operation in the discontinuous conduction mode.

5.9 An L–C input filter is added to a buck converter as illustrated in Fig. 5.25. Inductors L_1 and L_2 and capacitor C_2 are large in value, such that their switching ripples are small. All losses can be neglected.

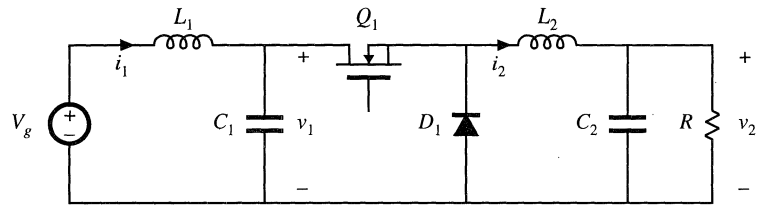

Fig. 5.25 Buck converter with input filter, Problems 5.9 and 5.10.

(a) Sketch the capacitor C_1 voltage waveform $v_1(t)$, and derive expressions for its dc component V_1 and peak ripple magnitude Δv_1.

(b) The load current is increased (R is decreased in value) such that Δv_1 is greater than V_1.

(i) Sketch the capacitor voltage waveform $v_1(t)$.

(ii) For each subinterval, determine which semiconductor devices conduct.

(iii) Determine the conditions under which the discontinuous conduction mode occurs. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.10 Derive an expression for the conversion ratio $M(D, K)$ of the DCM converter described in the previous problem. Note: D is the transistor duty cycle.

5.11 In the Cuk converter of Fig. 5.23, inductors L_1 and L_2 and capacitor C_2 are large in value, such that their switching ripples are small. All losses can be neglected.

(a) Assuming that the converter operates in CCM, sketch the capacitor C_1 voltage waveform $v_{C1}(t)$, and derive expressions for its dc component V_1 and peak ripple magnitude Δv_{C1}.

(b) The load current is increased (R is decreased in value) such that Δv_{C1} is greater than V_1.

(i) Sketch the capacitor voltage waveform $v_{C1}(t)$.

(ii) For each subinterval, determine which semiconductor devices conduct.

(iii) Determine the conditions under which the discontinuous conduction mode occurs. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.12 Derive an expression for the conversion ratio $M(D, K)$ of the DCM Ćuk converter described in the previous problem. Note: D is the transistor duty cycle.

5.13 A DCM buck-boost converter as in Fig. 5.21 is to be designed to operate under the following conditions:

$$136 \text{ V} \le V_g \le 204 \text{ V}$$
$$5 \text{ W} \le P_{load} \le 100 \text{ W}$$
$$V = -150 \text{ V}$$
$$f_s = 100 \text{ kHz}$$

You may assume that a feedback loop will vary to transistor duty cycle as necessary to maintain a constant output voltage of – 150 V.

Design the converter, subject to the following considerations:

- The converter should operate in the discontinuous conduction mode at all times
- Given the above requirements, choose the element values to minimize the peak inductor current
- The output voltage peak ripple should be less than 1V.

Specify:

(a) The inductor value L

(b) The output capacitor value C

(c) The worst-case peak inductor current i_{pk}

(d) The maximum and minimum values of the transistor duty cycle D

5.14 A DCM boost converter as in Fig. 5.12 is to be designed to operate under the following conditions:

$$18 \text{ V} \le V_g \le 36 \text{ V}$$
$$5 \text{ W} \le P_{load} \le 100 \text{ W}$$
$$V = 48 \text{ V}$$
$$f_s = 150 \text{ kHz}$$

You may assume that a feedback loop will vary to transistor duty cycle as necessary to maintain a constant output voltage of 48 V.

Design the converter, subject to the following considerations:

- The converter should operate in the discontinuous conduction mode at all times. To ensure an adequate design margin, the inductance L should be chosen such that K is no greater than 75% of K_{crit} at all operating points.
- Given the above requirements, choose the element values to minimize the peak inductor current.
- The output voltage peak ripple should be less than 1V.

Specify:

(a) The inductor value L

(b) The output capacitor value C

(c) The worst-case peak inductor current i_{pk}

(d) The maximum and minimum values of the transistor duty cycle D.

(e) The values of D, K and K_{crit} at the following operating points: (*i*) $V_g = 18$ V and $P_{load} = 5$ W; (*ii*) $V_g = 36$ V and $P_{load} = 5$ W; (*iii*) $V_g = 18$ V and $P_{load} = 100$ W; (*iv*) $V_g = 36$ V and $P_{load} = 100$ W.

5.15 In dc–dc converters used in battery-powered portable equipment, it is sometimes required that the converter continue to regulate its load voltage with high efficiency while the load is in a low-power "sleep" mode. The power required by the transistor gate drive circuitry, as well as much of the switching loss, is dependent on the switching frequency but not on the load current. So to obtain high efficiency at very low load powers, a variable-frequency control scheme is used, in which the switching frequency is reduced in proportion to the load current.

Consider the boost converter system of Fig. 5.26(a). The battery pack consists of two nickel-cadmium cells, which produce a voltage of $V_g = 2.4$ V ± 0.4 V. The converter boosts this voltage to a regulated 5 V. As illustrated in Fig. 5.26(b), the converter operates in the discontinuous conduction mode, with constant transistor on-time t_{on}. The transistor off-time t_{off} is varied by the controller to regulate the output voltage.

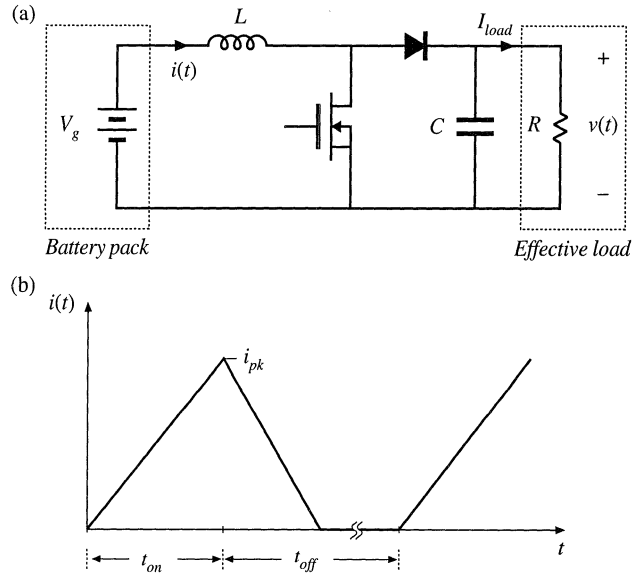

Fig. 5.26 Boost converter employed in portable battery-powered equipment with sleep mode, Problem 5.15: (a) converter circuit, (b) inductor current waveform.

(a) Write the equations for the CCM-DCM boundary and conversion ratio $M = V/V_g$, in terms of t_{on}, t_{off}, L, and the effective load resistance R.

For parts (b) and (c), the load current can vary between 100 μA and 1 A. The transistor on time is fixed: $t_{on} = 10$ μs.

(b) Select values for L and C such that:

- The output voltage peak ripple is no greater than 50 mV,
- The converter always operates in DCM, and
- The peak inductor current is as small as possible.

(c) For your design of part (b), what are the maximum and minimum values of the switching frequency?