Chapter 13: Switching Circuits

Overview

Prerequisites:
- Knowledge of basic circuit analysis

Objectives of Section 13.1:
- Understand the functionality of a semiconductor transistor switch
- Characterize the operation of a transistor switch by differentiating between the ground-side pull-down switch (NMOS transistor) and the power-side pull-up switch (PMOS transistor)
- Appreciate the value of MOSFET threshold voltage
- Solve simple switching circuits

Objectives of Section 13.2:
- Become familiar with simple switching motor controllers and load controller switches
- Track the operation of the H-bridge and the half H-bridge motor controllers
- Obtain initial exposure to pulse-width modulation (PWM) and motor speed control

Objectives of Section 13.3:
- Establish the relation between symbols for logic gates and underlying electric circuits on transistor level
- Review basic logic gates
- Obtain initial exposure to Boolean algebra and logic circuit analysis and synthesis
- Understand the functionality of a semiconductor memory cell

Application Examples:
- PWM motor controller
- Logic gate motor controller

S.N. Makarov et al., *Practical Electrical Engineering*, DOI 10.1007/978-3-319-21173-2_13

Keywords:

Electronic switch, Switch control voltage, Ground-side switch, Power-side switch, Series switch, Pull-down switch, Pull-up switch, Metal-oxide-semiconductor (MOS) transistors, NMOS transistors, PMOS transistors, Complementary transistors, CMOS circuits, Switching transistors, Switching diagram, Transistor threshold voltage, Matched switching transistors, Control switching circuits, Switching quadrants, Half H-bridge, Full H-bridge, Motor speed controller, Motor control states (forward mode, reverse mode, free run to a stop, motor brake), One-quadrant switch, Forbidden states, Pulse-width modulation (PWM), Duty cycle of PWM, Average supply voltage of PWM, Logic inverter, NOT gate, Truth table, NOR gate, OR gate, NAND gate, AND gate, Switching algebra, Boolean algebra, Boolean expressions, Laws of Boolean algebra (commutative law of addition, commutative law of multiplication, associative law of addition, associative law of multiplication, distributive law), De Morgan's laws, Exclusive OR (XOR) gate, Exclusive NOR (XNOR) gate, Logic circuit analysis, Logic circuit synthesis, Hardware description language (HDL), Sum-of-products approach, Product-of-sums approach, Karnaugh maps, Static random access memory (SRAM), Latch, Static RAM cell, Access transistors

Section 13.1 Principle of Operation

The manual switch used in electric circuits long ago and shown in Fig. 13.1a was first replaced by electromechanical relays and later on by transistor switches. Still, both the mechanical switch and the solenoid are widely used today: the mechanical switch finds its numerous applications in household electronics, whereas the relay is employed for switching high-power, high-current loads in power electronics. However, it is the transistor *electronic* switch that made possible digital systems, computers, control circuits, and modern communication circuits. Applications of the current switching technology range from toggle switches used in many simple circuits, including perhaps your laboratory kit, to power transistors used in power electronics and motor controllers and to literally billions of low-power switching transistors used in your computer. In the present section, we introduce the meaning of the transistor switch and explain its operation based on simple examples.

13.1.1 Switch Concept

An *electronic switch* shown in Fig. 13.1b is a circuit block that connects or disconnects two nodes *a* and *b* in a circuit depending on the voltage V_{in} (*switch control voltage*) supplied to a control terminal of the switch.

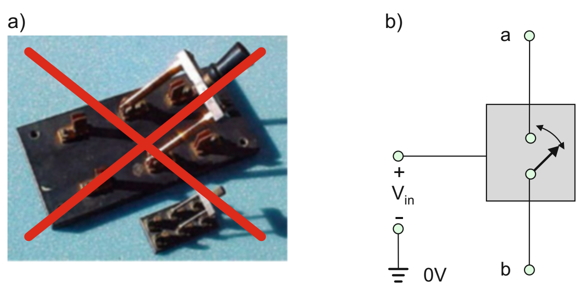


Fig. 13.1. Left—a mechanical copper switch. The background image is from Nicholas Gessler's website, Duke University (NC) and Umea University, Sweden. Right—schematic of a basic electronic switch with a control voltage V_{in}.

Therefore, any electronic switch should have at least *three terminals*: the control terminal V_{in} referenced to ground and two line terminals *a* and *b*. We note the following:

1. An electronic switch is typically a transistor switch. The transistor is a semiconductor device. This is in contrast to an electromechanical switch such as a *relay.*
2. The electronic switch always has a small but *finite* resistance (resistance between terminals *a* and *b*). The goal of a circuit designer is to reduce this resistance and the associate power loss in the switch. This can be done using proper circuit optimization, without modifying the transistor itself.

3. The electronic switch may use two distinct transistor types: the so-called metal-oxide-semiconductor field-effect transistors (MOSFETs) studied in Chapter 18 and the bipolar junction transistors (BJTs) studied in Chapter 17, respectively.
4. In this chapter, we will always implement MOSFET transistors since they are specifically used in digital circuits including microprocessors and computers.
5. The most important feature of the switch is that it consumes virtually *no* input power. Namely, the input current I_{in} into the control terminal in Fig. 13.1b is zero or close to zero, in contrast to the control voltage V_{in}.

An electronic switch is an important part of many analog circuits including power conversion circuits (DC to DC, AC to DC, etc.), DC and AC motor drives, etc. The switch is capable of turning on and off large line currents between terminals *a* and *b*. For example, a properly designed electronic switch may in principle allow us to turn on a 1-MW power plant with a single 9-V battery. On the other hand, an electronic switch is also the heart of any digital circuit. We could in principle build low-power switches using operational amplifiers studied in Chapter 5. However, a powerful, simple, versatile, and by far the fastest switch is a single-transistor switch.

13.1.2 Switch Position in a Circuit

Depending on the switch position in a circuit, we distinguish between:

1. A *ground-side switch*
2. A *power-side switch*
3. A *series switch*

All three switching configurations are quite intuitive; they are shown in Fig. 13.2. Resistor R_L designates a load. The switch position dictates the type of transistor to be used and the acceptable values of control voltages. The details are given in the following text. For example, the ground-side switch is implemented with an n-type transistor (MOSFET or BJT). Such a transistor conducts by *negative* carriers—electrons. The switch is *normally open* (which means that it is open at zero control voltage), but is closed at higher control voltage values. In contrast to that, the power-side switch is implemented with a p-type transistor (MOSFET or BJT). Such a transistor conducts by *positive* carriers—holes. The switch is *normally closed* (closed at zero control voltage), but is open at such control voltage values that are close to the supply voltage. The series switch (the switch between two power blocks of a larger circuit) may use either transistor type. However, the control voltage must be higher than the voltage to be switched. From the viewpoint of a simple resistive load R_L in Fig. 13.2, it really does not matter where the control switch is exactly located: on the ground side or on the power side. Hence, either type of the switch may be chosen. However, more sophisticated loads such as motors or solenoids are controlled by several switches that are located both on the ground side and on the power side and, thus, have quite distinct features.

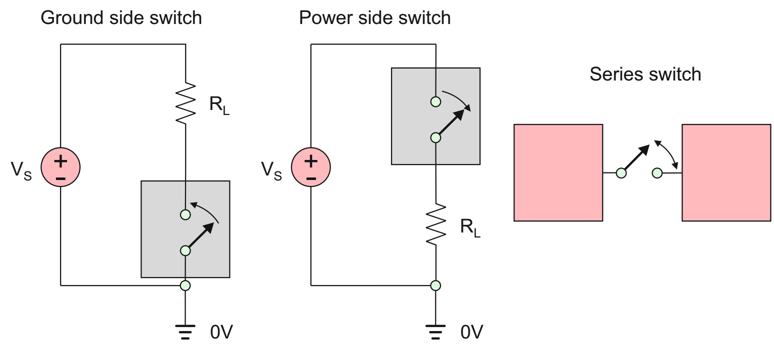


Fig. 13.2. Switch positions in a circuit.

13.1.3 MOSFET Switches and Threshold Voltage

Among a variety of transistor types and switches, the switches based on *metal-oxide-semiconductor (MOS) transistors* are most widely used in modern analog switching applications. The MOS transistor switches almost entirely dominate the digital circuitry; they serve about 98 % of those circuits. Overall, about 90 % of the electronic market works with MOSFETs. Two of such switches—the ground-side switch (normally open) and the power-side switch (normally closed)—are shown in Fig. 13.3.

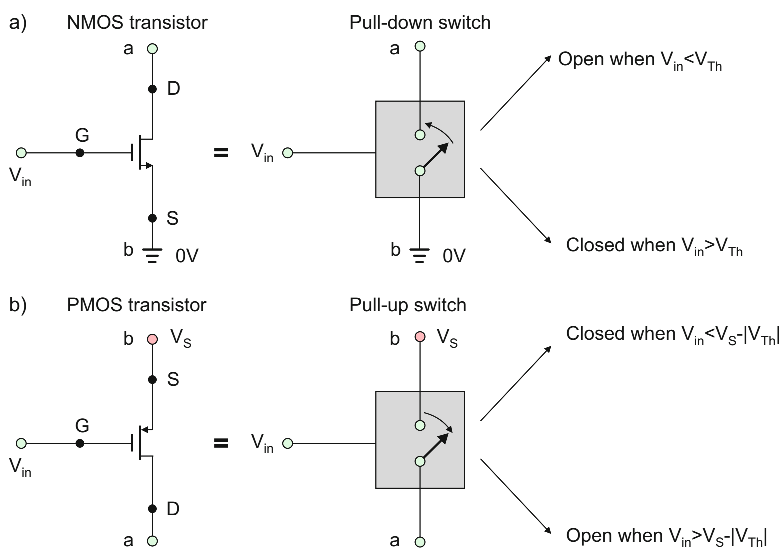


Fig. 13.3. Two types of electronic switches on the basis of field-effect transistors: the pull-down or ground-side switch (normally open) and the pull-up or power-side switch (normally closed).

We will assume that both switches operate with a supply voltage V_S. Sometimes, the ground-side switch is also called the *pull-down switch*, whereas the power-side switch is called the *pull-up switch*. This is indicated in Fig. 13.3. The abbreviation *NMOS* in

Fig. 13.3 means n-type or n-channel MOS transistor, whereas the abbreviation *PMOS* in Fig. 3 corresponds to a p-type or p-channel MOS transistor. The arrow in the (simplified) transistor symbols always indicates the (normal) current direction. Transistor terminals in Fig. 13.3 are called *drain* (D), *gate* (G), and *source* (S). An important feature of the switches in Fig. 13.3 is that:

1. All NMOS transistors should be connected either to ground or to another NMOS transistor—see Fig. 13.3a. This is the ground-side switch.
2. Similarly, all PMOS transistors should be connected either to the voltage source V_S or to another PMOS transistor—see Fig. 13.3b. This is the power-side switch.

Both transistors (NMOS and PMOS) are often called *complementary transistors* or simply complements. *CMOS* (complementary MOS) *circuits* use both of them. Figure 13.4 shows a typical *switching diagram* for the two transistor switches. We indicate the switch state *as a function of the control voltage* V_{in}. We assume in this chapter that the transistor switch is precisely an open circuit when it is OFF and that it is a short circuit of zero resistance when it is ON. Such an assumption corresponds to an *ideal switch*. It is acceptable during the initial study, but it may be a crude approximation to reality when the accurate results are required.

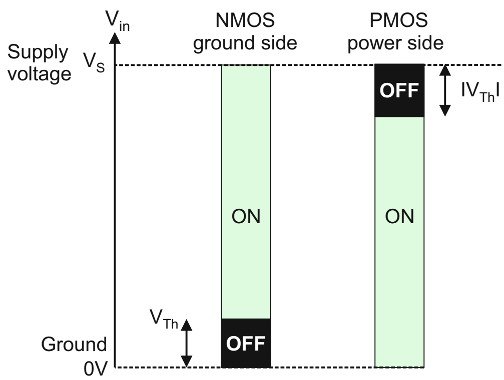


Fig. 13.4. Switching diagram for two MOSFET transistors.

It is seen from Figs. 13.3 and 13.4 that the switching behavior is determined by the so-called transistor threshold voltage. The NMOS transistor has a threshold voltage $V_{Tn} > 0$; the PMOS transistor has a threshold voltage $V_{Tp} < 0$. The two *switching transistors* in Figs. 13.3 and 13.4 are said to be *matched* when their threshold voltages coincide in terms of the absolute values:

$$V_{Tn} = \left|V_{Tp}\right| = V_{Th} \tag{13.1}$$

where V_{Th} is the common threshold voltage. We will only consider the matched transistors. The meaning of transistor threshold voltage is quantified in Chapter 18. With reference to Fig. 13.4, the NMOS transistor is OFF when the control voltage V_{in} is less than the threshold voltage V_{Th}. It is ON for all other control voltages. Conversely, the PMOS transistor is OFF when the control voltage V_{in} is close to the supply voltage: $V_{\text{in}} > V_{\text{S}} - |V_{\text{Th}}|$. It is ON for all other control voltages. The typical values are $0.4\ \text{V} \le V_{\text{Th}} \le 4\ \text{V}$. There is no current into the gate of the transistor (control terminal), either in ON or OFF state. Therefore, virtually no input power is needed to turn the transistor switch ON or OFF. The mid-region of operation (when both transistors are ON) in Fig. 13.4 corresponds to the *saturation state* of MOSFETs where the power loss in the switches themselves becomes significant (transistors will heat up). It also corresponds to the undefined digital CMOS voltages—see below. Therefore, the mid-region should be possibly *avoided*.

Exercise 13.1: A switching circuit driven by a 10-V power supply uses both NMOS and PMOS transistor switches. The threshold voltage is $V_{\text{Tn}} = 2\ \text{V}$ for the NMOS transistor and $|V_{\text{Tp}}| = 2\ \text{V}$ for the PMOS transistor. What are the acceptable values of the control voltage V_{in} to have one switch ON and another OFF?

Answer: $8\ \text{V} \le V_{\text{in}} \le 10\ \text{V}$ and $0\ \text{V} \le V_{\text{in}} \le 2\ \text{V}$.

In digital circuits, the supply voltage V_{S} may vary from 5 V (0.8-μm CMOS) all the way down to 1.4 or 1.2 V for a modern 45-nm CMOS process. The transistor threshold voltages in digital circuits may vary from about 700 mV (0.8 μm CMOS) all the way down to 200 mV. In analog circuits, the supply voltage may vary widely; it is typically 12 V or some multiples of this number. The transistor threshold voltages (power transistors are used) are higher, about 2–4 V. Remember again that both switches in Fig. 13.3 or Fig. 13.4 require *zero input current* and thus consume *zero input power*: the input resistance of two switches is therefore infinite with a high degree of accuracy. However, they could source or sink a significant power to a load. For example, the NMOS transistor may sink a significant load current and discharge a load capacitor down to zero volts (this is the reason for the name *pull down*). Similarly, the PMOS transistor may source a significant current into a load (i.e., *pull up* the load voltage).

13.1.4 Sketch of Transistor Physics

The theory and the basic circuit design for MOS field-effect transistors (MOSFETs) are studied in Chapter 18. Here, we discuss a simplified transistor model in Fig. 13.5 representing an n-channel MOSFET. The transistor is a semiconductor device; the NMOS transistor includes two metal electrodes, drain (D) and source (S), with a weakly conducting semiconductor material (Si or GaAs) between them—a channel. A third electrode (gate or G) with voltage V_{in} is attached to the channel *through an insulator*. When the input voltage V_{in} versus ground is close to zero, the channel is virtually an open circuit, with a very low conductivity—see Fig. 13.5a.

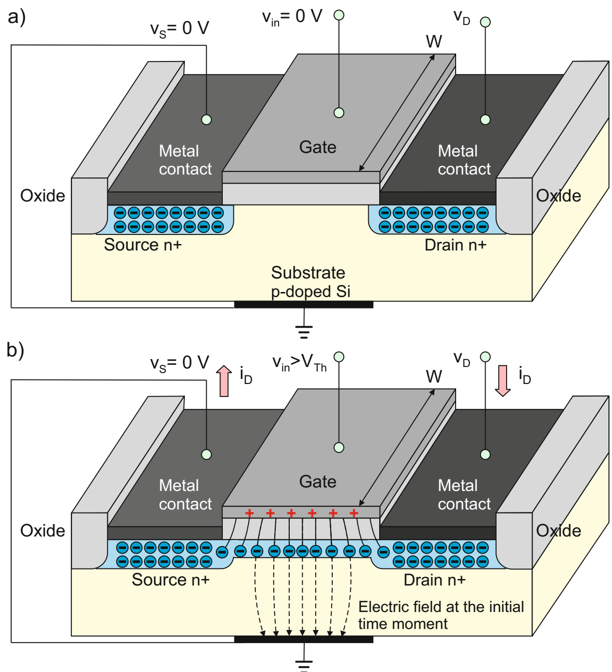


Fig. 13.5. Simplified diagram of transistor conduction for an n-channel MOSFET: (**a**) zero control voltage and (**b**) control voltage approaching the threshold value.

When the input voltage V_{in} versus ground is close to zero, the channel is virtually an open circuit, with a small concentration of charge carriers and a very low conductivity—see Fig. 13.5a. The switch is thus open (normally open). When a positive voltage V_{in} is applied to the control terminal, the corresponding electric field *attracts* more negative electron carriers to the channel from the drain and source semiconductor regions with the rich electron concentration, thus making the channel more conducting. The dependence of the conductivity on V_{in} is exponential, i.e., very sharp. When V_{in} reaches the threshold voltage V_{Tn} or exceeds it, the channel becomes conducting, i.e., resembles a wire—see Fig. 13.5b. The switch becomes closed. The intrinsic threshold voltage V_{Tn} of the NMOS transistor depends on transistor geometry and doping concentrations. The PMOS transistor operates in an opposite way. It is closed when the control voltage V_{in} is close to zero and opens when V_{in} reaches the difference between the source voltage V_{S} and the magnitude of the intrinsic *threshold* voltage for the PMOS transistor, $|V_{\text{Tp}}|$.

Example 13.1: Two circuits in Fig. 13.6 operate with a source $V_{\text{S}} = 5$ V. The transistor threshold voltages are $V_{\text{Tn}} = \left|V_{\text{Tp}}\right| = 1$ V. Find the output voltage V_{out} to each circuit if (a) $V_{\text{in}} = 0.0\text{V}$, (b) $V_{\text{in}} = 0.5\,\text{V}$, (c) $V_{\text{in}} = 4.5\,\text{V}$, and (d) $V_{\text{in}} = 5.0\,\text{V}$.

Example 13.1 (cont.):

Solution: We use Fig. 13.4 as a reference and fill out Table 13.1 that follows. The transistor switch is replaced by a short circuit when it is ON and by an open circuit when it is OFF.

Table 13.1. Output voltages to the circuits from Fig. 13.6.

Input voltage	Switch state and output voltage—NMOS switch	Switch state and output voltage—PMOS switch
0 V	OFF (V_{out} is determined by the rest of circuit)	ON $V_{out} = 5$V
0.5 V	OFF (V_{out} is determined by the rest of circuit)	ON $V_{out} = 5$ V
4.5 V	ON $V_{out} = 0$ V	OFF (V_{out} is determined by the rest of circuit)
5.0 V	ON $V_{out} = 0$ V	OFF (V_{out} is determined by the rest of circuit)

The NMOS switch sets the output voltage equal to zero at all high input voltages, whereas the PMOS switch sets the output voltage equal to 5 V at all low input voltages. This will allow us to use both switches in digital logic circuits.

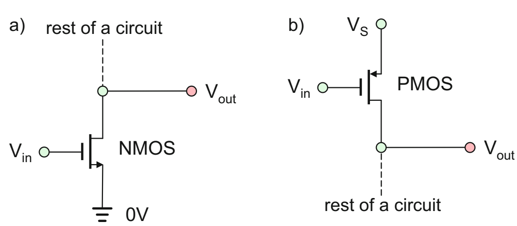


Fig. 13.6. Transistor switch operation at different values of the input voltage.

We should also mention alternative circuit symbols for the switches shown in Fig. 13.7.

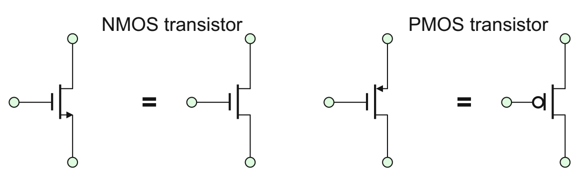


Fig. 13.7. Alternative circuit symbols for the transistor switches from Fig. 13.3.

Section 13.2 Power Switching Circuits

13.2.1 Switching Quadrants

In this section, we introduce and describe the principle of operation for some standard *control switching circuits* for motor loads including:

1. A single-transistor switch (one-quadrant switch)
2. A *half H-bridge* switch with two transistors (two-quadrant switch)
3. A *full H-bridge* switch with four transistors (four-quadrant switch)
4. A *motor speed controller* using pulse-width modulation (PWM)

The *switching quadrants* of load voltage/current are shown in Fig. 13.8. For a *resistive* load (a DC heater), the load voltage V_L and the load current I_L are always positive, i.e., are in the first quadrant or at zero. Therefore, the one-quadrant switch or a single-transistor switch considered next is quite sufficient.

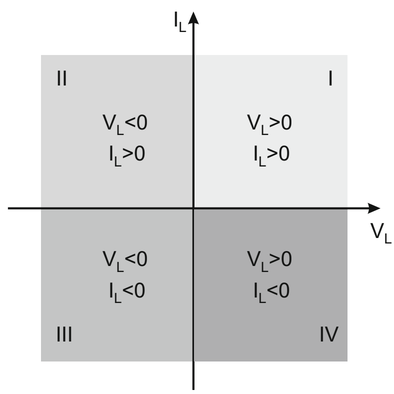


Fig. 13.8. Quadrants of load voltage and load current.

Instead of one simple switching option for a resistive load, the *motor switching* generally requires four different states:

- *Forward mode* (the motor spins clockwise—quadrant I)
- *Reverse mode* (the motor spins counterclockwise—quadrant III)
- *Free run to a stop* (the motor stops slowly)
- *Motor brake* (the motor stops suddenly, using the brake effect of the Lorentz force studied in Chapter 7)

A more involved transistor switch is therefore necessary. Such a switch (the *H-bridge*) will be studied step by step. Also, we wish to control the motor speed in a continuous fashion, which requires pulse-width modulation and the H-bridge modifications studied next. The motor may also operate as a generator, i.e., in the second and fourth quadrants in Fig. 13.8. Switching between motor and generator functions requires additional efforts.

13.2.2 Switching a Resistive Load

A switching circuit with one NMOS transistor (the ground-side switch) is shown in Fig. 13.9 for a resistive load R_L. The circuit always operates in the first quadrant in Fig. 13.8. In practice, the circuit must include a current-limiting resistor.

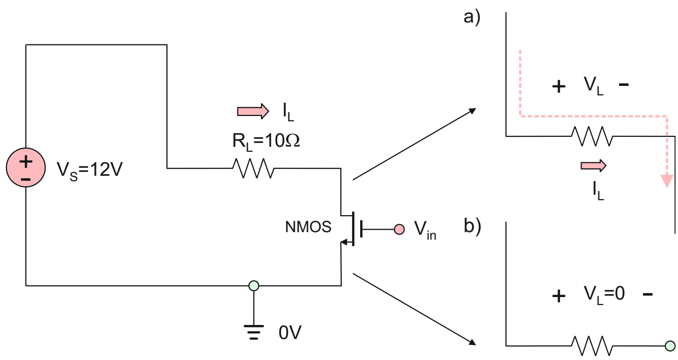


Fig. 13.9. Switching circuit for a resistive load operating in the first quadrant.

Example 13.2: In Fig. 13.9, an IRF510 n-channel power MOSFET is used with $V_{Tn} = 3.5$ V. Establish power delivered to the resistive load when the control voltage V_{in} switches from 0 V to 9 V.

Solution: When the control voltage is 0 V, the NMOS transistor switch is OFF according to the switching chart in Fig. 13.4. The load is disconnected from the source; the load power is zero. When $V_{in} = 9$ V, the switch closes. In the ideal approximation of zero switch resistance, the load voltage is the source voltage, and we obtain the load power of 14.4 W. In reality, the switch in Fig. 13.9 has to be carefully optimized to avoid losses in the transistor. For the present example (with the circuit parameters from Fig. 13.9), the more accurate analysis predicts the load power of 12.8 W and the transistor resistance of 0.6 Ω. We will learn in Chapter 18 that this value can be reduced by increasing the control voltage signal V_{in}.

13.2.3 Switching a DC Motor

A motor load requires a more involved treatment compared to the simple resistive load.

In order to proceed further, we should recall the *motor model* at DC steady state. This model shown in Fig. 13.10 includes the induced emf, E (the dependent voltage source), and the armature resistance, R_M.

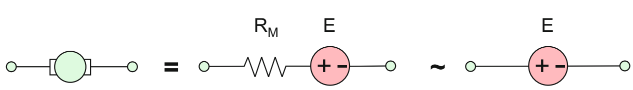


Fig. 13.10. Motor model and its simplification.

In order to perform a qualitative analysis of switching circuits, the (small) armature resistance R_M may be ignored. This leads us to a simplified motor model with no armature resistance also shown in Fig. 13.10. We will use this model in what follows. When the motor in Fig. 13.11a operating in the forward mode is disconnected from the main source by virtue of a top switch, one should distinguish between two different states—see Fig. 13.11b, c, respectively. The first state is shown in Fig. 13.11a. The second switch is left disconnected. Then, one of motor terminals is left disconnected. Therefore, the current through the motor, I_a, is exactly zero just after switching. The motor torque T is also zero. However, the motor angular speed, ω, is not zero, i.e.,

$$I_a = 0 \Rightarrow T = K_T I_a = 0, \quad \omega \neq 0 \tag{13.2a}$$

The motor speed slowly decreases toward zero depending on its internal friction. We call this state *free run to a stop*. The second state is shown in Fig 13.11b. The motor is disconnected from the main source, but its terminals are shorted out so that the induced emf E is exactly equal to zero just after switching. The motor speed is also zero. However, the motor torque is not zero; it actually has an opposite sign and quickly decelerates the load, due to current I_a fed back into the motor, i.e.,

$$E = 0 \Rightarrow \omega = E/K_V = 0, \quad T \neq 0 \tag{13.2b}$$

We call this state *motor brake*.

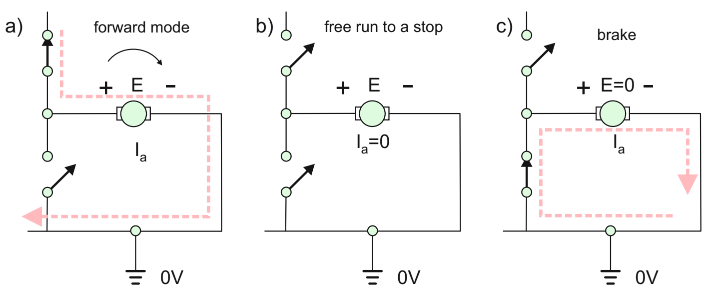


Fig. 13.11. Two possible motor states after disconnecting the power source.

Note that for a purely resistive load, the states in Fig.13.11b, c will be identical. Both current through the load and the voltage across the load are zero just after disconnecting the top switch. The same treatment of Fig. 13.11 holds for a reverse mode of operation, when the supply current through the motor flows in the opposite direction. We could also define two similar switching states for this mode—free run to stop and a brake.

13.2.4 One-Quadrant Switch for a DC Motor

A simple switching circuit—the *one-quadrant switch*—for a DC motor is shown in Fig. 13.12. It operates in the first quadrant. When the transistor switch is closed, the motor operates in the forward mode—see Fig. 13.12a. When the switch opens, the motor will operate in a free run to a stop mode—see Fig. 13.12b. No other modes of operation are possible. Note that in Fig. 13.12 we use different notations compared to Fig. 13.9: $V_L \to E, I_L \to I_a$. Those notations are common in the theory of electric machines. E stands for the induced emf and I_a stands for an armature current of a motor.

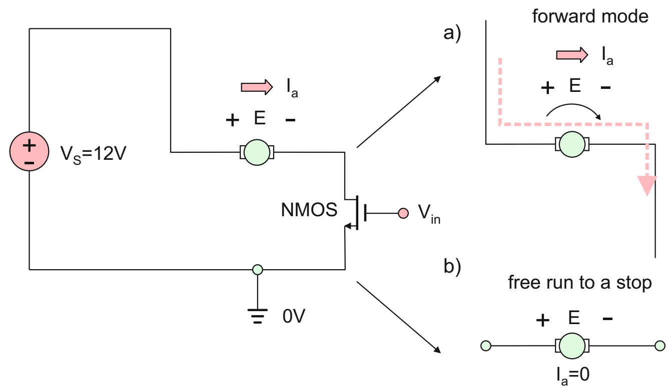


Fig. 13.12. Switching circuit for a DC motor operating in the first quadrant.

Example 13.3: Consider a switching circuit with a power NMOS transistor shown in Fig. 13.12. The IRF510 n-channel power MOSFET from Vishay Siliconix with $V_{Tn} = 3.5$ V is used again; the switching voltage V_{in} is either 0 V or 9 V. We wish to describe motor behavior when switch opens.

Solution: When the control voltage V_{in} in Fig. 13.12 is 9 V, the NMOS transistor switch is ON according to the switching chart in Fig. 13.4. The motor is in the forward mode in Fig. 13.12a. The term *forward mode* means that the first quadrant in Fig. 13.8 is used. When V_{in} in Fig. 13.12 switches to 0 V at $t = 0$, the switch opens. The motor current becomes exactly zero and that the motor does not create any extra torque. However, the induced emf or the voltage across the motor E continues to stay the same. Then, it slowly decreases in time. So does the motor velocity. Such a state shown in Fig. 13.12b is called *free run to a stop*. This state is useful, but it may be not quite sufficient if we also wish to implement a true *brake*, i.e., suddenly stop the motor. To do so, the circuit in Fig. 13.12 needs to be modified as described in the following text.

13.2.5 Half H-Bridge for a DC Motor

We aim to modify the circuit in Fig. 13.12 in order to implement the motor brake option, which was impossible with the previous circuit. The new circuit is shown in Fig. 13.13. The circuit has the name of a *half H-bridge* for an obvious reason. It uses two switches: the ground-side NMOS transistor and the power-side PMOS transistor. Under no circumstances shall both transistors be turned on simultaneously.

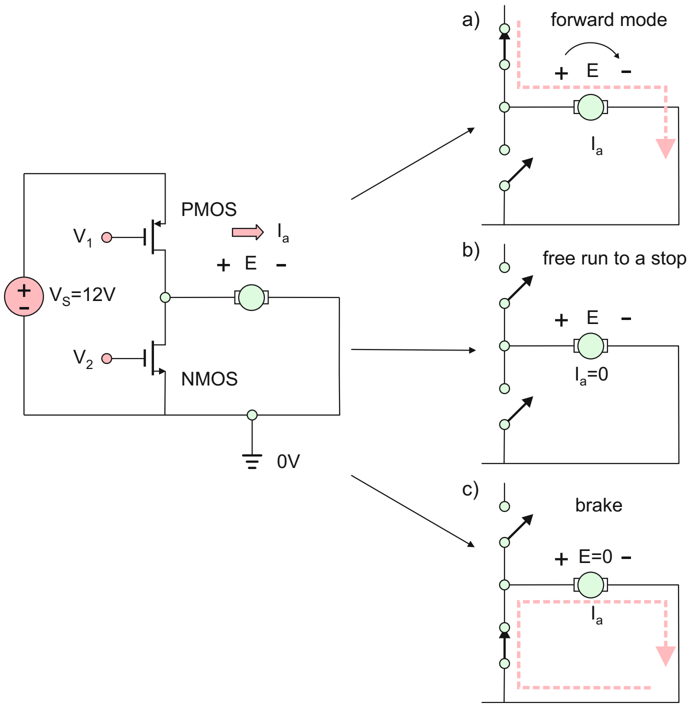


Fig. 13.13. Half H-bridge transistor switch with three motor functions.

Example 13.4: We consider the switching circuit with power NMOS/PMOS transistors shown in Fig. 13.13. We use an IRF520 n-channel power MOSFET and its complement, an IRF9520 p-channel power MOSFET, both from Vishay Siliconix. We assume that $V_{Tn} = |V_{Tp}| = 3.5\,\text{V}$; the switching voltages $V_{1,2}$ are either 0 V or 9 V. The circuit behavior is studied when two control voltages are given by
(i) $V_1 = 0\,\text{V}, V_2 = 0\,\text{V}$, (ii) $V_1 = 9\,\text{V}, V_2 = 0\,\text{V}$, and (iii) $V_1 = 9\,\text{V}, V_2 = 9\,\text{V}$.

Solution: In case (i), the PMOS switch is ON; the NMOS switch is OFF. The motor is in the forward mode shown in Fig. 13.13a.

In case (ii), both switches are OFF. The motor is disconnected from the circuit; the motor current is zero but not the motor voltage E, which slowly decreases toward zero while the motor slows down. This is free run to a stop—a state in Fig. 13.13b that is also achievable with only one transistor as described in the previous subsection. In case (iii), however, the situation changes. The PMOS switch is OFF whereas the NMOS switch is ON too. The motor is not only disconnected from the power source, but it is also shorted out. This means that the motor voltage or induced emf E is exactly zero just after the motor is shorted out. Then, from Eq. (13.2b), one has $\omega = 0$ for the angular speed. In other words, the motor should stop suddenly. Such a state is the motor brake shown in Fig. 13.13c. An experimental demonstration of the brake option in laboratory might be a quite valuable addition to this analysis. Now, how about spinning the motor in the opposite direction? In order to do so, we should further modify the switching transistor circuit as described further.

13.2.6 Full H-Bridge for a DC Motor

The circuit in Fig. 13.13 is further modified in order to implement the *reverse mode* of operation, i.e., spin the motor in the opposite direction. In that case, the motor should operate in the third quadrant of Fig. 13.8. The modified circuit is shown in Fig. 13.14. Compared to Fig. 13.13, the circuit includes the second (missing) half of the full H-bridge. The circuit in Fig. 13.14 has *four* control voltages V_1, V_2, V_3, V_4 and *sixteen* possible control states. Under no circumstances shall both transistors in either side of the bridge be turned on simultaneously (the *forbidden stages*).

Example 13.5: Determine forbidden states (short-circuited states) for the H-bridge in Fig. 13.14. Use an IRF520 n-channel power MOSFET and its complement, an IRF9520 p-channel power MOSFET, and assume that $V_{Tn} = |V_{Tp}| = 3.5\,\text{V}$; the switching voltages $V_{1,2,3,4}$ are either 0 V or 9 V.

Solution: The forbidden states correspond to a short circuit on either side of the bridge. Thus, they are:

i. $V_1 = 0\text{V}, V_2 = 9\text{V};\quad V_3, V_4$ are arbitrary
ii. $V_3 = 0\text{V}, V_4 = 9\text{V};\quad V_1, V_2$ are arbitrary

There are totally seven independent forbidden combinations. If we denote the 0-V control voltage by 0 (low) and the 9-V control voltage by 1 (high), the forbidden control voltages $V_{1,2,3,4}$ in the digital form are:
0100 0001 0101 1001 0110 1101 0111

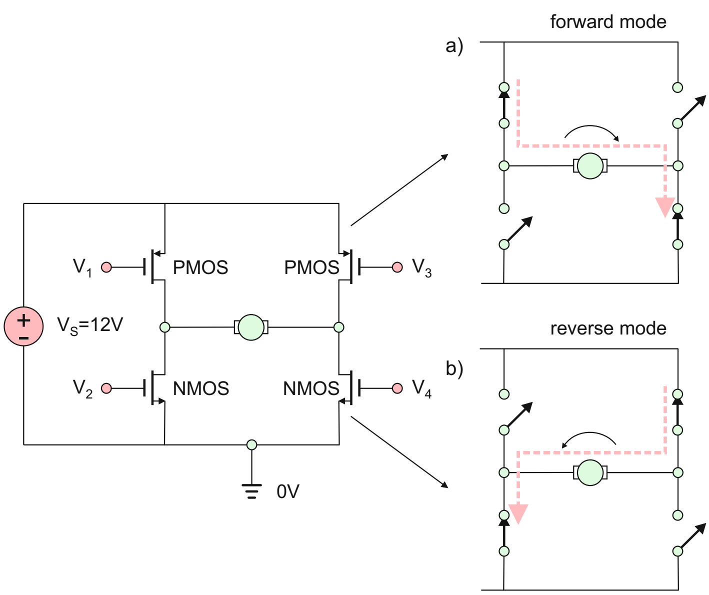


Fig. 13.14. Full H-bridge transistor switch with four motor functions.

Example 13.6: The H-bridge in Fig. 13.14 has the switching voltages $V_{1,2,3,4}$ that are either 0 V or 9 V. The power MOSFETS with $V_{Tn} = |V_{Tp}| = 3.5\,V$ are considered. Determine all meaningful states of the control voltages.

Solution: We need to realize two directions of rotations (forward mode and stop mode), plus free run to a stop and a brake for each direction. The corresponding states for $V_{1,2,3,4}$ in the digital form are those from Table 13.2. For illustration, Fig. 13.15 shows how two first free run to a stop states have been calculated.

Table 13.2. Allowed states of the control voltages $V_{1,2,3,4}$ for the circuit in Fig. 13.14.

Forward mode—see Fig. 13.7a	0011
Reverse mode—see Fig. 13.7b	1100 (inverse of the above)
Free run to a stop (reverse or forward mode—five combinations)	1110 0010 1011 1000 1010 (all off)
Brake (reverse or forward mode—two combinations)	1111 0000

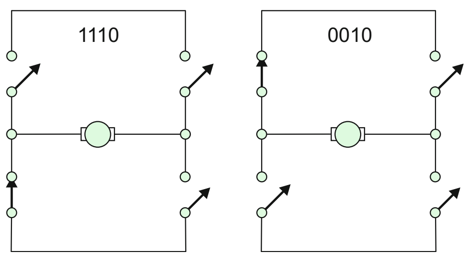


Fig. 13.15. Identification of two possible free run to a stop states. Two next states (1011 and 1000) are obtained by permutation.

One may note a great similarity in the above bridge and the Wheatstone bridge made of four resistors. Another bridge, the diode rectifying bridge from Chapter 16, is also very similar to the present design. What makes those three circuits look so similar even though they function quite differently? The answer is ability to control current direction using two distinct current paths—two sides of the bridge. By this point, we have implemented the motor forward/reverse mode, free run to a stop, and the brake options. And yet, how about spinning the motor at a given speed, i.e., doing the complete speed control? In order to do so, we should further modify the switching transistor circuit as described next.

13.2.7 Application Example: Pulse-Width Modulation (PWM) Motor Controller PWM Voltage Form

If someone needs speed control, an obvious way may be to vary load voltage using a voltage divider with a variable resistor. For example, a 12-V Mabuchi DC motor RS-380PH-3270 may operate at supply voltages from 4.5 V to 15 V, not necessarily at exactly the nominal voltage of 12 V. However, this method results in higher losses in the divider circuit. This method might also result not only in the decrease of the motor speed but also the motor current I_a and the instantaneous motor torque. Another way of controlling the speed is the *pulse-width modulation* (PWM). In that case, the supply voltage to the motor is varied as a rectangular periodic waveform shown in Fig. 13.16.

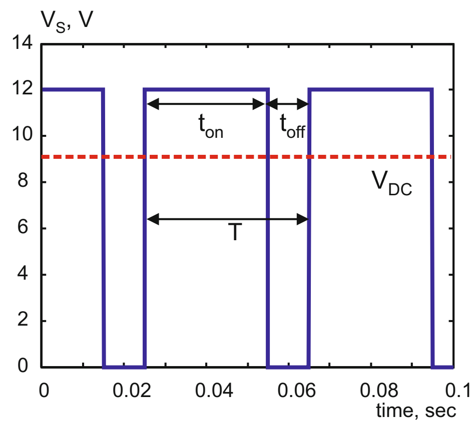


Fig. 13.16. Pulse-width modulation of the supply voltage to the motor.

The motor operates at its nominal voltage (12 V in Fig. 13.16) during the ON phase (with the duration t_{on}). The power supply is disconnected from the motor during the OFF phase with the duration t_{off}. The *period* of the periodic waveform in Fig. 13.16 is given by

$$T = t_{on} + t_{off} \tag{13.3}$$

The frequency (measured in hertz, $1\,\text{Hz} = 1/\text{s}$) of the waveform is given by

$$f = \frac{1}{T} \quad [\text{Hz}] \tag{13.4}$$

The *duty cycle d* (fraction) or *D* (percentage) of the periodic wave form is given by

$$d = \frac{t_{on}}{T}, \quad D = \frac{t_{on}}{T} \times 100\,\% \tag{13.5}$$

When both ON and OFF phases are equal, the duty cycle is said to be exactly 50 %. The *average supply voltage* V_{DC} of PWM in Fig. 13.16 is given by

$$V_{DC} = \frac{t_{on}}{T} V_S = dV_S \quad (13.6)$$

This is the voltage that will be actually applied to a motor. Thus, the PWM also decreases the average supply voltage but in the lossless way.

Example 13.7: Determine all parameters of the PWM voltage in Fig. 13.16 including period, frequency, duty cycle d, and the average voltage V_{DC}.

Solution: From Fig. 13.16 by observation, $t_{on} = 30$ ms, $t_{off} = 10$ ms. Therefore, $T = 40$ ms, $f = 1/0.04 = 25$ Hz. We further find the duty cycle and the average voltage in the form

$$d = t_{on}/T = 0.75, \quad V_{DC} = dV_S = 0.75 \times 12 = 9 \text{ V} \quad (13.7)$$

Thus, varying the duty cycle changes the output voltage V_{DC} in Fig. 13.16.

According to the equivalent motor circuit, one can write for the motor angular speed ω (again neglecting the motor armature and brush resistance R_M and using the *voltage constant* of the DC motor, K_V):

$$\omega = \frac{E}{K_V} \approx \frac{V_{DC}}{K_V} \quad (13.8)$$

Equation (13.8) says that applying the PWM with $d = 0.75$ shown in Fig. 13.16 to a 12-V DC motor results in the average supply voltage of 9 V and the motor speed reduction of 25 %.

PWM Realization

Commercial PWM controllers use the PWM applied directly to four transistors of the H-bridge shown in Fig. 13.14 at the frequencies of approximately 10–20 kHz. A laboratory setup that could be driven by a simple function generator is shown in Fig. 13.17. This setup uses one more NMOS transistor as a switch controlling the PWM but still keeps the full functionality of the H-bridge. The NMOS switch is normally OFF (OFF at zero gate voltage). Therefore, the control signal applied to the transistor gate from a function generator is *identical* in form to the PWM supply voltage. However, the supply voltage in Fig. 13.17 has indeed the peak value of 12 V, whereas the control signal may have different peak values of 9 V, 10 V, 12 V, etc. Note that the use of both PMOS and NMOS transistors is intuitively very appealing. However, the present CMOS design of the H-bridge might have higher losses in the PMOS power transistors. Therefore, an *H-bridge with the only NMOS transistors* is typically used since it has a lower loss (Fig. 13.18).

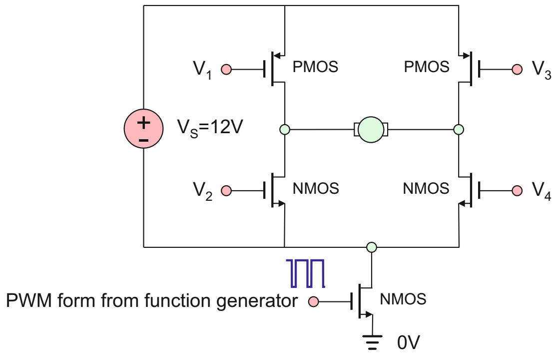


Fig. 13.17. Realization of the PWM with one more switching transistor added to the H-bridge. The control signal to the transistor gate is supplied by a function generator.

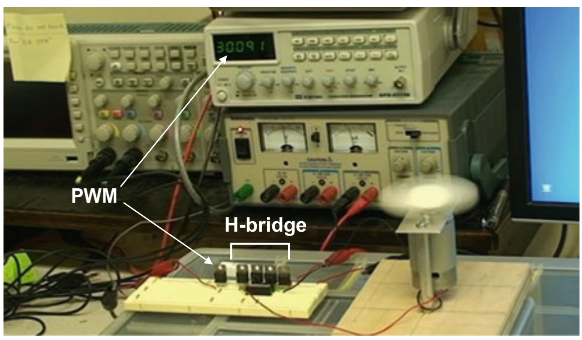


Fig. 13.18. PWM motor controller in undergraduate laboratory. The H-bridge is controlled by a DIP switch. The PWM control signal to the transistor gate is supplied by a function generator.

Section 13.3 Digital Switching Circuits

A digital circuit is the same electric circuit except for the fact that it performs a different function. For example, previously we have used transistors to control the motor. Now, we will use the same transistors and even in a similar configuration, in order to perform logic operations and arithmetic operations. An immediate question to ask is how an electric circuit may be used to operate with numbers because we used to think that the circuit operates with voltages and currents only. The simple answer here is that virtually any digital circuit, including the computer that you are using right now, employs electric voltages as a carrier of information. A digital circuit consists of logic gates. A logic gate is a switching circuit that we shall study in this section. Any logic gate is an extension or a generalization of a *logic inverter*, which is considered first.

13.3.1 NOT Gate or Logic Inverter

Consider the circuit shown in Fig. 13.19. It includes the PMOS transistor (normally ON) as the power-side switch and the NMOS transistor (normally OFF) as a ground-side switch. The circuit is powered by a 5-V power supply. The two transistors are matched and have equal (absolute) threshold voltages $\left|V_{\mathrm{Tp}}\right| = V_{\mathrm{Tn}} = 1\ \ \mathrm{V}$. The circuit is identical to the half H-bridge considered in the previous section, but it serves a different purpose.

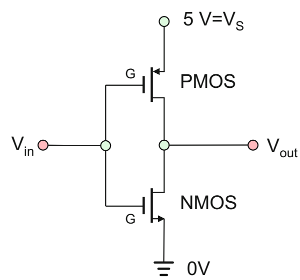


Fig. 13.19. CMOS *logic inverter* or *NOT gate*.

The input voltage to the circuit follows the first column of Table 13.3. Further, we shall use the chart from Fig. 13.4 of Section 13.1 in order to study the circuit behavior. When the input voltage is low (0 V), the NMOS switch is OFF and the PMOS switch is ON. The output voltage is 5 V. When the input voltage is high (5 V), the situation changes to the opposite: the NMOS switch is ON and the PMOS switch is OFF. The output voltage is 0 V. Hence the output voltage follows the second column of Table 13.3.

Table 13.3. Output voltage of the logic inverter versus the input voltage.

V_{in}	V_{out}
0 V	5 V
5 V	0 V

If we denote the 0-V voltage by value 0 (low or false) and the 5-V voltage by value 1 (high or true), Table 13.3 is converted to the so-called truth table—Table 13.4.

Table 13.4. Truth table for the logic circuit in Fig. 13.19—the logic inverter. We substitute 0 instead of 0 V and 1 instead of 5 V.

V_{in}	V_{out}
0	1
1	0

The circuit thus performs logic inversion (substitutes zero instead of one or false instead of true and vice versa). The symbol for this is the *logic NOT* gate shown in Fig. 13.20.

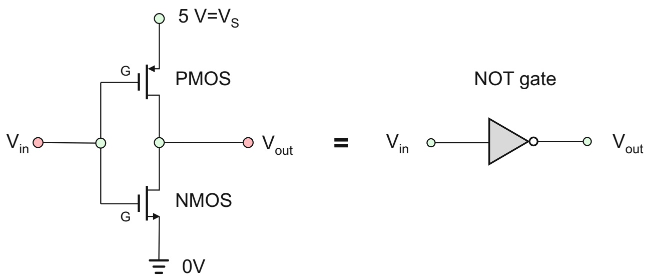


Fig. 13.20. Symbol for the NOT gate along with the corresponding circuit diagram.

Note that the input voltage may slightly vary around zero volts or around five volts. As long as these variations do exceed 1 V (do not exceed threshold voltages of the transistors), the circuit shall still output exactly the results shown in Tables 13.3 and 13.4. The corresponding task is suggested as a homework problem. This property of the NOT gate is critical—it means that the present logic operation is *immune* to electric noise.

13.3.2 NOR Gate and OR Gate

NOR Gate

Consider the circuit with four transistors shown in Fig. 13.21. This circuit may be considered as an extension of the logic inverter shown in Fig. 13.19. Now, one has two input voltages V_1 and V_2 instead of one input voltage V_{in}. The circuit is powered by a 5-V power supply. All four transistors (two PMOS and two NMOS transistors) are matched and have equal threshold voltages $|V_{Tp}| = V_{Tn} = 1\ \text{V}$.

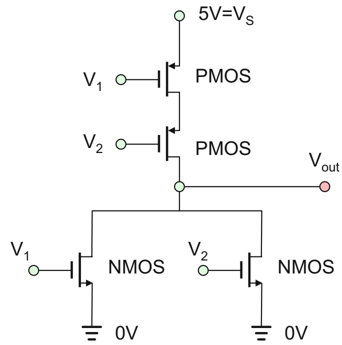


Fig. 13.21. CMOS NOR logic gate.

The input voltages to the circuit follow the first columns of Table 13.5. Further, we shall use the chart from Fig. 13.4 of Section 13.1 in order to study the circuit behavior. When the input voltages V_1 and V_2 are both low (0 V), the NMOS switches are OFF and the PMOS switches are ON. The output voltage is therefore 5 V. When the input voltage V_1 is high (5 V), irrespectively of the value of the input voltage V_2, the leftmost NMOS transistor is ON, so that the output voltage is always 0 V. A similar situation occurs when V_2 is high (5 V). The output voltage is always 0 V. Hence the output voltage follows the last column of Table 13.5.

Table 13.5. Output voltage of the NOR gate versus the input voltages.

V_1	V_2	V_{out}
0 V	0 V	5 V
0 V	5 V	0 V
5 V	0 V	0 V
5 V	5 V	0 V

If we again denote the 0-V voltage by value 0 (low or false) and the 5-V voltage by value 1 (high or true), Table 13.5 is converted to the truth table—Table 13.6.

Table 13.6. Truth table for the logic circuit in Fig. 13.21—the NOR gate.

V_1	V_2	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

It follows from Table 13.6 that this circuit does not perform the logic OR operation (outputs true when at least one input is true). Rather, it does exactly the opposite.

Therefore, this circuit is called NOT OR or simply the NOR logic gate. Its symbol is shown in Fig. 13.22.

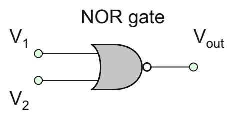


Fig. 13.22. Symbol for the NOR gate.

Note that the input voltages V_1 and V_2 may slightly vary around zero volts or around five volts. As long as these variations do not exceed 1 V (do not exceed threshold voltages of the transistors), the circuit shall still output exactly the results shown in Tables 13.5 and 13.6. The corresponding task is suggested as a related homework problem. This property of the NOR logic gate (and of all other logic gates) is critical—it shows us that arbitrary logic operations with voltages are immune to electric noise.

OR Gate

How to construct the gate that performs an OR operation? One way is to contemplate the corresponding circuit diagram, which will include a number of PMOS and NMOS transistors. Yet another way is to mention that the OR gate is simply obtained by a series combination of the NOR gate and the NOT gate—see Fig. 13.23. The corresponding truth table is Table 13.7. Further, we may substitute the real circuits from Fig. 13.19 and Fig. 13.21 instead of symbols in Fig. 13.23 and obtain the resulting circuit for the OR gate. It will include six transistors total. Generally, the way of constructing logic circuits outlined in Fig. 13.23 is simple and powerful.

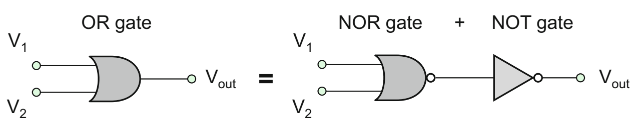


Fig. 13.23. Construction of the OR gate from NOR gate and NOT gate.

Table 13.7. Truth table for the OR gate.

V_1	V_2	V_{out}
0	0	0
0	1	1
1	0	1
1	1	1

Note that the NOR (and OR) gate may have an arbitrary number of inputs as shown in Fig. 13.24. The resulting circuit shall be a straightforward modification of the circuit in Fig. 13.21. The corresponding task is suggested as a homework problem.

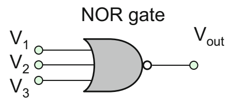


Fig. 13.24. The NOR gate with three inputs.

Example 13.8: An oxygen sensor outputs high voltage (5 V) when the oxygen concentration in a room is not sufficient. Otherwise, its output is low (0 V). A temperature sensor outputs high voltage (5 V) when the temperature in a room is too high. Otherwise, its output is low (0 V). Construct a logic circuit that outputs high voltage (5 V) and lights up a red indicator when either of the sensor readings is high.

A. Present the symbolic circuit diagram.
B. Present the electric circuit diagram including individual transistors.

Solution: The input to the logic circuit will consist of two voltages V_1 and V_2—sensor outputs. The logic circuit itself is the OR gate with two inputs shown in Fig. 13.23. According to Table 13.7, it does output the high voltage when either of its inputs is high. The electric circuit diagram is the transistor circuit in Fig. 13.21 in series with the circuit from Fig. 13.19.

13.3.3 NAND Gate and AND Gate

NAND Gate

Consider again the circuit with four transistors shown in Fig. 13.25. The difference from the NOR gate circuit in Fig. 13.21 is that the PMOS transistors are now in parallel, but the NMOS transistors are in series. The circuit has two input voltages, V_1 and V_2, similar to the NOR gate. The circuit is powered by a 5-V power supply. All four transistors (two PMOS and two NMOS transistors) are matched and have equal threshold voltages $|V_{Tp}| = V_{Tn} = 1\ \text{V}$.

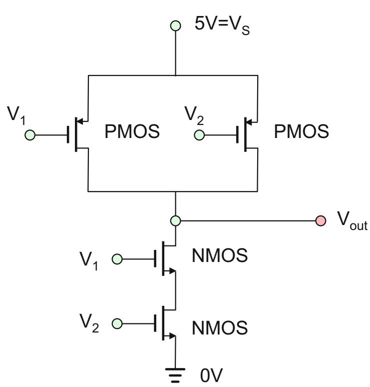


Fig. 13.25. CMOS NAND logic gate.

The input voltages to the circuit follow the first columns of Table 13.8. Then, we use the chart from Fig. 13.4 of Section 13.1 in order to determine the circuit behavior. When either of the input voltages V_1 and V_2 is low (0 V), one of the PMOS switches is always ON, so that the output voltage is always high (5 V). Only when both input voltages are high, both PMOS switches are OFF, but the NMOS switches are ON. The output becomes low (0 V). Hence the output voltage follows the last column of Table 13.8.

Table 13.8. Output voltage of the NAND gate versus the input voltages.

V_1	V_2	V_{out}
0 V	0 V	5 V
0 V	5 V	5 V
5 V	0 V	5 V
5 V	5 V	0 V

If we again denote the 0-V voltage by value 0 (low or false) and the 5-V voltage by value 1 (high or true), Table 13.8 is converted to the truth table—Table 13.9.

Table 13.9. Truth table for the logic circuit in Fig. 13.25—the NAND gate.

V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

It follows from Table 13.9 that this circuit does not perform the logic AND operation (outputs true only when both inputs are true). Rather, it does exactly the opposite. Therefore, this circuit is called NOT AND or simply the NAND logic gate. Its symbol is shown in Fig. 13.26.

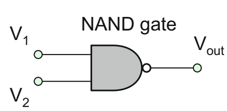


Fig. 13.26. Symbol for the NAND gate.

AND Gate

How to construct the gate that performs an AND operation? Similar to the OR gate from the previous subsection, the AND gate is simply obtained by a series combination of the NAND gate and the NOT gate shown in Fig. 13.27.

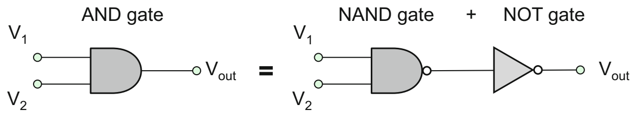


Fig. 13.27. Construction of the AND gate from NAND gate and NOT gate.

The corresponding voltage table is Table 13.10; the truth table is Table 13.11. Further, we may substitute the real circuits from Figs. 13.25 and 13.19 instead of symbols in Fig. 13.26 and obtain the resulting circuit for the AND gate. It will include total six transistors.

Table 13.10. Output voltage of the AND gate versus the input voltages.

V_1	V_2	V_{out}
0 V	0 V	0 V
0 V	5 V	0 V
5 V	0 V	0 V
5 V	5 V	5 V

Table 13.11. Truth table for the AND gate.

V_1	V_2	V_{out}
0	0	0
0	1	0
1	0	0
1	1	1

Note that the NAND (and AND) gate may have an arbitrary number of inputs—see Fig. 13.28. The resulting circuit will be a straightforward modification of the circuit in Fig. 13.27. The corresponding task is suggested as a homework problem.

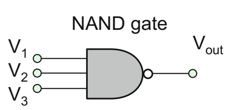


Fig. 13.28. The NAND gate with three inputs.

Example 13.9: We study the operation of the AND gate one more time and perform a simple experiment. Please open your calculator and type 0. Apart from an intermediate circuitry, you've just sent 0 V to input V_1 in Table 13.10. Now type the multiplication sign. You've chosen the AND gate. Then type 0 again. You've sent 0 V to input V_2 in Table 13.10. Then hit ENTER. Your result is zero or $V_{out} = 0$ V. Thus, the calculator multiplication $0 \times 0 = 0$ relates to voltage operations by

$0 \times 0 = 0$ is equivalent to→	V_1	V_2	V_{out}
	0 V	0 V	0 V

The calculator multiplication $0 \times 1 = 0$ relates to voltage operations by

$0 \times 1 = 0$ is equivalent to→	V_1	V_2	V_{out}
	0 V	5 V	0 V

The calculator multiplication $1 \times 0 = 0$ relates to voltage operations by

$1 \times 0 = 0$ is equivalent to→	V_1	V_2	V_{out}
	5 V	0 V	0 V

Finally, the calculator multiplication $1 \times 1 = 1$ relates to voltage operations by

$1 \times 1 = 1$ is equivalent to→	V_1	V_2	V_{out}
	5 V	5 V	5 V

Thus, with one logic gate, we can accomplish the multiplication of ones and zeros. This is not much, but a digital circuit may include a large number (thousands and even millions) of such logic gates.

Example 13.10: A humidity sensor outputs high voltage (5 V) when the humidity percentage in a room is too high. Otherwise, its output is low (0 V). A temperature sensor outputs high voltage (5 V) when the temperature in a room is too high. Otherwise, its output is low (0 V). Construct a logic circuit that outputs high voltage (5 V) and lights up a red indicator only when both sensor readings are high.

A. Present the symbolic circuit diagram.
B. Present the electric circuit diagram including individual transistors.

Solution: The input to the logic circuit will consist of two voltages V_1 and V_2—sensor outputs. The logic circuit itself is the AND gate with two inputs shown in Fig. 13.27. According to Table 13.10, it outputs the high voltage if and only if both inputs are high. The electric circuit diagram is the transistor circuit in Fig. 13.25 in series with the circuit from Fig. 13.19.

13.3.4 Simple Combinational Logic Circuits: Switching Algebra

The primary purpose of the logic gates is to serve as a building block of a complex digital system. At the same time, they are also useful as stand-alone components in the form of so-called logic circuits. Logic circuits consist of individual logic gates. Logic circuits are classified into two types: "combinational" and "sequential." A *combinational logic circuit* is one whose outputs depend only on its current inputs. In other words, the combinational logic circuit has no memory. A combinational logic circuit may contain an arbitrary number of logic gates, but no feedback loops. Such a circuit is studied next. In contrast to the analog circuits, logic circuits are not described by KVL and KCL. Instead, they are described in terms of the *switching algebra* or *Boolean algebra* named in honor of George Boole, an English mathematician. The switching algebra uses only two values (states):

0 or voltage low
1 or voltage high

There are three basic Boolean operations: NOT, AND, and OR. They exactly correspond to the three logic gates described in the previous subsections. If A and B are two *logic or Boolean variables* (inputs to the gates), which can only assume values 0 and 1, then we could describe those operations with the help of Table 13.12 that follows.

Historical: George Boole (1815–1864) invented his two-value algebraic system in 1854. He was the first who replaced the operation of multiplication by the word AND and addition by the word OR. In 1938, Claude Shannon showed how to use this system to describe simple digital circuits.

Table 13.12. Basic logic operations and their symbols.

Operation	Symbol	Gate	Result
Logic inversion	$\overline{A}$	NOT	$\overline{0} = 1$ $\overline{1} = 0$
Logic multiplication	$A \cdot B$	AND	$0 \cdot 0 = 0$ $0 \cdot 1 = 0$ $1 \cdot 0 = 0$ $1 \cdot 1 = 1$
Logic addition	$A + B$	OR	$0 + 0 = 0$ $0 + 1 = 1$ $1 + 0 = 1$ $1 + 1 = 1$

Boolean variables form *Boolean expressions* (the logic circuits), which satisfy a number of fundamental laws and rules:

$$A + B = B + A \quad \text{commutative law of addition} \tag{13.9a}$$

$$A \cdot B = B \cdot A \quad \text{commutative law of multiplication} \tag{13.9b}$$

$$A + (B + C) = (A + B) + C \quad \text{associative law of addition} \tag{13.9c}$$

$$A \cdot (B \cdot C) = (A \cdot B) \cdot C \quad \text{associative law of multiplication} \tag{13.9d}$$

$$A \cdot (B + C) = A \cdot B + A \cdot C \quad \text{distributive law} \tag{13.9e}$$

$$\begin{gathered} A + 0 = A, \quad A + 1 = 1, \quad A \cdot 0 = 0, \quad A \cdot 1 = 1, \quad A + A = A, \quad A + \overline{A} = 1, \\ A \cdot A = A, \quad A \cdot \overline{A} = 0, \quad \overline{\overline{A}} = A \end{gathered} \tag{13.9f}$$

Exercise 13.2: Simplify the Boolean expression $A + A \cdot B$ (AND gate and OR gate applied to inputs A and B).

Answer: $A + A \cdot B = A$.

13.3.5 Universal Property of NAND Gates: De Morgan's Laws

When looking for logic gates in the form of integrated circuits (ICs), you will probably encounter a large number of NAND gate chips, with up to four gates per chip. A typical example is a MM74HC00 *quad* NAND gate from Fairchild Semiconductor that currently costs $0.50 (a 14-pin DIP package). Why are the other gates not so popular? The reason for such a selection is simple: the NAND gate is a *universal gate* so that all other gates (NOT, AND, OR, and NOR) can be constructed from NAND gates when necessary. Furthermore, the NAND gate is faster (has a smaller number of transistor and a *smaller propagation delay*) than an AND gate or an OR gate. The above statement is proved for OR (and NOR) gates using *De Morgan's laws*. These laws are given by two *Boolean expressions*, for two (or more) Boolean variables X and Y, which are

$$A + B = \overline{\overline{A} \cdot \overline{B}} \tag{13.10a}$$

$$A \cdot B = \overline{\overline{A} + \overline{B}} \tag{13.10b}$$

Equation (13.10a) states that any OR gate may be constructed from a NAND gate with the inverted inputs. Vice versa, Eq. (13.10b) states that any AND gate may be constructed from a NOR gate with the inverted inputs. Interestingly, the NOR gate is also a universal gate: all other gates could in principle be constructed from the NOR gates. De Morgan's laws are employed to simplify and transform Boolean expressions, so that you can use one sort of gate, generally only using NAND or NOR gates. This leads to cheaper and faster hardware.

Exercise 13.3: Using De Morgan's laws, present the equivalent representation of the OR gate with two inverted inputs, $\overline{A} + \overline{B}$, in terms of the NAND gate(s).

Answer: $\overline{A} + \overline{B} = \overline{A \cdot B}$. Therefore, the OR gate with inverted inputs is exactly equivalent to one NAND gate and vice versa.

Exercise 13.4: *Exclusive OR* or XOR *gate*, which symbol is shown in Fig. 13.29, is formed by a combination of other gates. However, because of its fundamental importance, this gate is often treated as a basic logic element. The output of the XOR gate is given by $C = A \cdot \overline{B} + \overline{A} \cdot B$ where A and B are the inputs. Give an alternative expression for the output that involves the OR gate in the form $(A + B)$.

Answer: $C = (A + B) \cdot \overline{A \cdot B}$.

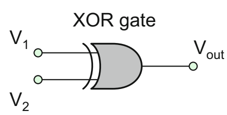


Fig. 13.29. Exclusive OR or XOR gate.

13.3.6 Logic Circuit Analysis and Application Example: Logic Gate Motor Controller

Logic circuit analysis implies finding the behavior of the logic circuit for various input combinations. Given a logic diagram for a combinational circuit, we obtain a formal description of its operation, either in the form of a truth table or as a timing diagram if time dependence is involved. As an example, we consider an H-bridge controller from the previous section built in the laboratory and shown in Fig. 13.30c.

Obtaining Truth Table of the Logic Circuit

The H-bridge in Fig. 13.30a controls a DC motor placed at its center using four power MOSFETs and four control voltages V_1, V_2, V_3, V_4 applied to their gates. Similar to the Boolean algebra considered in this section, the control voltages could only have high and low values. The motor has four meaningful states: forward and reverse rotation, free run to a stop, and brake. On the other hand, four control voltages V_1, V_2, V_3, V_4 provide 16 total possible switching combinations. Some of them are forbidden states (shorting out the circuit), yet some others are redundant states. Do we really need four independent control voltages to achieve the meaningful states? The answer is indeed no. Two independent control voltages would exactly suffice since they provide four independent control combinations, 00, 01, 10, and 11, each of which could be assigned to a particular meaningful state. Therefore, it is desired to control the H-bridge in Fig. 13.30a not with four independent switches but with only *two* independent switches shown in Fig. 13.30b. In order to accomplish this task, a logic circuit can be constructed as shown in Fig. 13.30c. This logic circuit has two inputs and four outputs. Its analysis results in a truth table which is Table 13.13 that follows.

Determining Motor State

Further, we use the MOSFET operation chart—see Fig. 13.4 in Section 13.2 of this chapter—and arrive at Table 13.14, which employs the data of Table 13.13 for control voltages V_1, V_2, V_3, V_4 in order to determine the particular transistor state and finally establish the motor state.

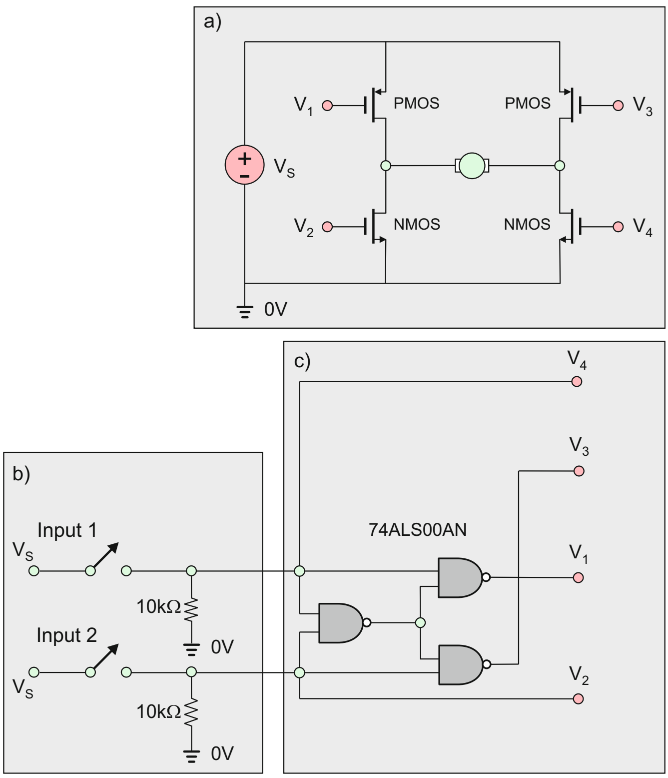


Fig. 13.30. A simple manual two-switch motor controller with three NAND gates.

Table 13.13. Truth table for the logic circuit in Fig. 13.30c.

Input1	Input2	V_1	V_2	V_3	V_4
0	**0**	1	0	1	0
0	**1**	1	1	0	0
1	**0**	0	0	1	1
1	**1**	1	1	1	1

Table 13.14. Motor states calculated from Table 13.13 and using the MOSFET switching behavior.

Input1	Input2	V_1	V_2	V_3	V_4	Trans. state (1,2,3,4)	Motor state
0	**0**	1	0	1	0	OFF/OFF/OFF/OFF	Free run to a stop
0	**1**	1	1	0	0	OFF/ON/ON/OFF	Reverse mode
1	**0**	0	0	1	1	ON/OFF/OFF/ON	Forward mode
1	**1**	1	1	1	1	OFF/ON/OFF/ON	Brake

Thus, the analysis of the logic circuit established the usefulness of the motor controller in Fig. 13.30c. This controller replaces four switches by two switches while preserving the full functionality of the H-bridge. Furthermore, it protects the H-bridge against the forbidden states (short circuits). The controller may be implemented in the laboratory with one low-cost quad NAND IC—see Fig. 13.31. It is important to note two resistors to ground in Fig. 13.30b, which are called the *pull-down resistors*. These resistors assure that the control voltage does go to zero when the switch is disconnected (no static charge). When switches "Input1" and "Input2" in Fig. 13.30b operate as functions of time, one may obtain the corresponding *timing diagram* for the logic circuit. This task is suggested in a number of homework problems at the end of this section.

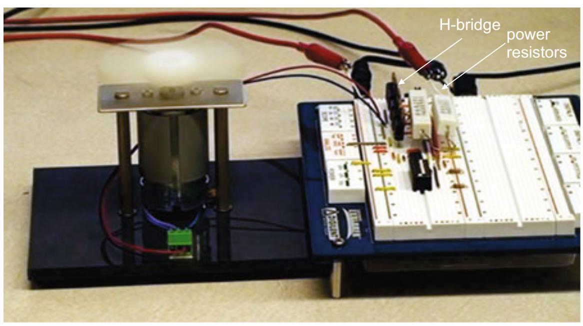


Fig. 13.31. Manual two-switch H-bridge motor controller from Fig. 13.30 implemented in an undergraduate laboratory using Digilent Electronics Explorer board with built-in NAND 74HC00 IC.

13.3.7 Logic Circuit Synthesis

Logic circuit design is mostly a *synthesis of a logic circuit*. We start with a verbal description of the circuit (or function that it should perform) and proceed to the circuit diagram, which includes a number of logic gates. In modern digital design, the word description is translated into a program in a so-called hardware description language (HDL). The HDL synthesizes a logic circuit for such a program so that the designer never gets involved into the real design process. However, there are still many situations where the logic circuit is designed and/or modified "by hand." When a truth table is available, there is always a way to design the logic circuit using the *sum-of-products* approach or the *product-of-sums approach*. Both these methods are studied in digital circuit design classes. However, the established logic circuits may be way too cumbersome and expensive. They often need further minimization. This is accomplished based on *Karnaugh maps*, which provide a graphic representation of the truth table. The logic circuit design then becomes an exciting engineering design journey, which is beyond the scope of the present text.

Example 13.11: A county board is composed of three commissioners. Each commissioner votes on measures presented to the board by pressing a 5-V button indicating whether the commissioner votes for or against a measure. If two or more commissioners vote for a measure, it passes. You are asked to help with a logic circuit that takes the three votes as inputs and lights a green LED (outputs 5 V) to indicate that a measure passed. You can use OR and/or AND logic gates, as many of them as you need.

Solution: First, we may want to translate the description of the desired operation into a truth table. The truth table has three logic inputs A, B, C and one output, M. The output M is one as long as any combination of A, B, C has at least two ones and is zero otherwise. One straightforward Boolean expression for the output has the form:

$$M = A \cdot B + A \cdot C + B \cdot C \tag{13.11a}$$

The corresponding hardware solution includes three AND gates connected to an OR gate with three inputs. Another possible Boolean expression for the output has the form:

$$M = (A + B) \cdot (A + C) \cdot (B + C) \tag{13.11b}$$

The corresponding hardware solution includes three OR gates connected to an AND gate with three inputs. The hardware realization of either logic circuit may be implemented with only NAND gates. The LED will light up at high output voltage (5 V or close) and be off at low output voltage (0 V or close).

13.3.8 The Latch

Most of the transistors today are used in semiconductor memories. Memory devices are embedded in digital integrated circuits. Memory can occupy most of the area of a computer processor chip. There are several types of semiconductor memories. We will describe the topology of a unit cell for one such memory type—the static RAM (SRAM) or the *static random access memory*. RAM means that every data bit is accessible any time unlike hard disk memory. All RAM memories are *volatile*, which means that they require a continuous presence of a power supply. SRAM cells provide the fastest operation among all other memories. SRAM cells are used as cache memory embedded in a processing unit where speed is critical. The basic memory element, *the latch*, is shown in Fig. 13.32. It consists of two cross-coupled inverters connected input to output. The latch has two stable states listed in Table 13.15. All other states are unstable, which means that they contradict the operation of the two logic gates. Thus, any arbitrary initial voltage distribution will be very quickly transformed to one of the stable states. As long as power is present, the latch can remain in any of the stable states indefinitely long. In other words, the latch circuit *memorizes* the initial state, due to the effect of the positive feedback.

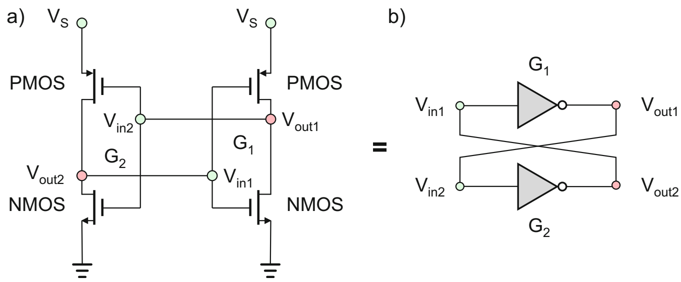


Fig. 13.32. Basic latch consisting of two inverters.

Table 13.15. Stable states of the latch circuit. Note the inversion of all voltages for two different states.

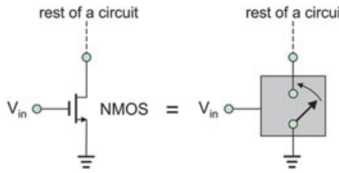
State	V_{in1}	V_{in2}	V_{out1}	V_{out2}
#1	1	0	0	1
#2	0	1	1	0

With the two stable states, the latch circuit is capable of storing one bit of data. One state is then designated as 0 (LOW) and another as 1 (HIGH). It now remains to design a mechanism by which the state can be written and read. This is accomplished in a *static RAM memory cell*, which uses two additional *access* (or *pass*) NMOS transistors.

Summary

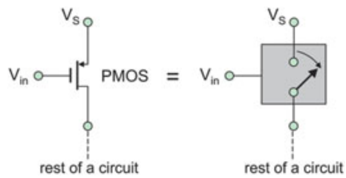
Transistor switches

Ground-side NMOS transistor switch (normally OFF)—pull down switch



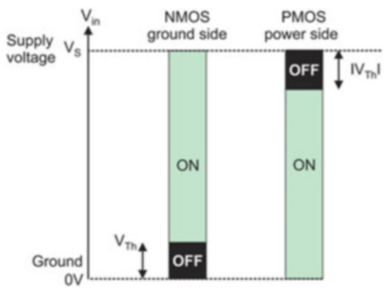
A. Closes when $V_{in} > V_{tn}$;
B. For efficient operation, the control voltage V_{in} must be as high as possible in the ON position;
C. Complement to PMOS switch

Power-side PMOS transistor switch (normally ON)—pull up switch



A. Opens when $V_{in} > V_S - |V_{tp}|$;
B. For efficient operation, the control voltage V_{in} must be as low as possible in the ON position;
C. Complement to NMOS switch

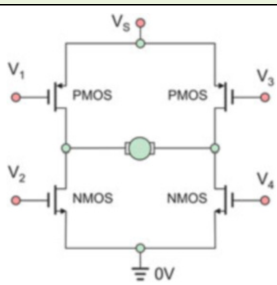
Transistor switching diagram



A. V_{in}—control voltage;
B. Assume $V_{tn} = V_{Th}$;
C. Assume $|V_{tp}| = V_{Th}$;
D. Typical values of V_{Th} are in the range from 0.4 to 4 V
E. V_{Th} depends on transistor geometry and composition

Transistor motor controllers

H-bridge



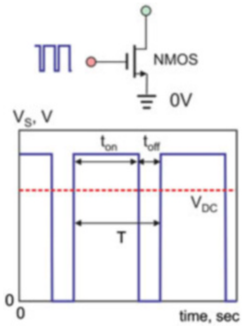
Controls a DC motor load enabling:
- Forward mode;
- Reverse mode;
- Free run to a stop;
- Brake states

Available commercially as an H-bridge IC.
Simpler modification—half H-bridge

V_1	V_2	V_3	V_4	**State**
0	0	0	0	Brake
0	0	0	1	Forbidden
0	0	1	0	Free run to a stop
0	0	1	1	Forward mode
0	1	0	0	Forbidden
0	1	0	1	Forbidden
0	1	1	0	Forbidden
0	1	1	1	Forbidden
1	0	0	0	Free run to a stop
1	0	0	1	Forbidden
1	0	1	0	Free run to a stop
1	0	1	1	Free run to a stop
1	1	0	0	Reverse mode
1	1	0	1	Forbidden
1	1	1	0	Free run to a stop
1	1	1	1	Brake

(continued)

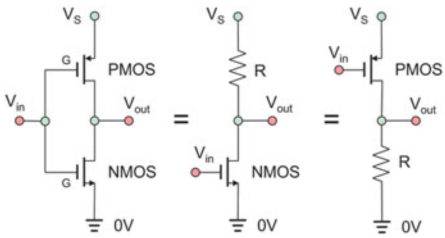
Basic pulse width modulation (PWM) waveform

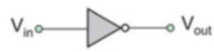


Period (sec) $T = t_{on} + t_{off}$
Frequency (Hz) $f = 1/T$
Duty cycle $d = \frac{t_{on}}{T}, \quad D = \frac{t_{on}}{T} \times 100\,\%$
Average supply voltage $V_{DC} = dV_S$

Basic logic gates and switching (Boolean) algebra

Logic inverter (NOT gate)

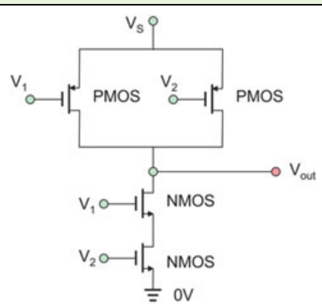


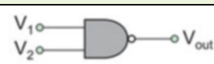


V_{in}	V_{out}
0	1
1	0

For single-transistor design, resistance R should be very large

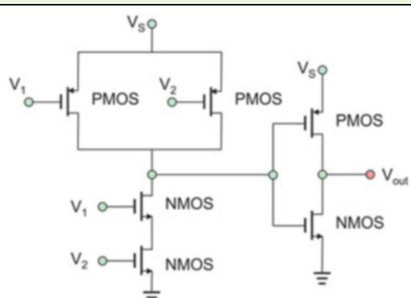
NAND gate

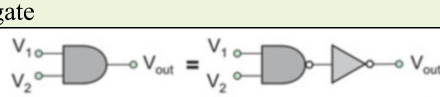




V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

AND gate

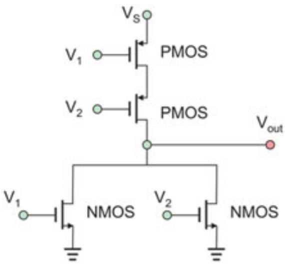


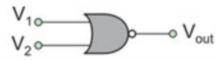


V_1	V_2	V_{out}
0	0	0
0	1	0
1	0	0
1	1	1

(continued)

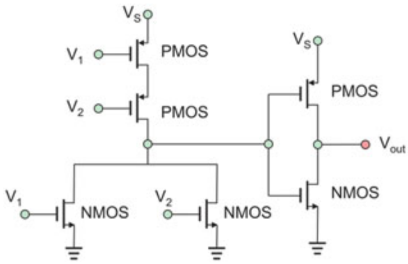
NOR gate

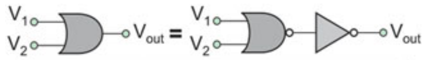




V_1	V_2	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

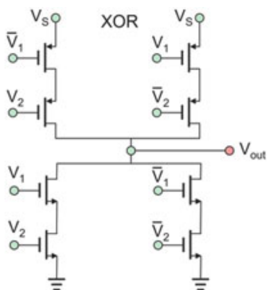
OR gate

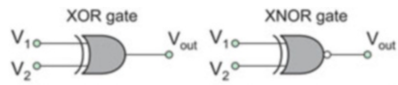




V_1	V_2	V_{out}
0	0	0
0	1	1
1	0	1
1	1	1

Exclusive OR (XOR) gate and exclusive NOR (XNOR) gates





V_1	V_2	V_{out} (XOR)	V_{out} (XNOR)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Switching (Boolean) algebra

Operation	Symbol	Gate	Result
Logic inversion	$\overline{A}$	NOT	$\overline{0}=1$ $\overline{1}=0$
Logic multiplication	$A\cdot B$	AND	$0\cdot 0=0$ $0\cdot 1=0$ $1\cdot 0=0$ $1\cdot 1=1$
Logic addition	$A+B$	OR	$0+0=0$ $0+1=1$ $1+0=1$ $1+1=1$

$A+B=B+A$

$A\cdot B=B\cdot A$

$A+(B+C)=(A+B)+C$

$A\cdot(B\cdot C)=(A\cdot B)\cdot C$

$A\cdot(B+C)=A\cdot B+A\cdot C$

$A+0=A,\ \ A+1=1,\ \ A\cdot 0=0,$

$A\cdot 1=1,\ \ A+A=A,\ \ A+\overline{A}=1,$

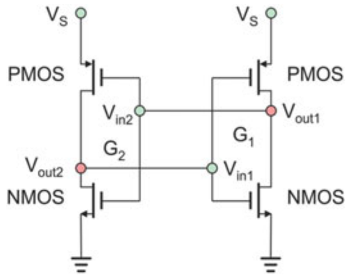
$A\cdot A=A,\ \ A\cdot\overline{A}=0,\ \ \overline{\overline{A}}=A$

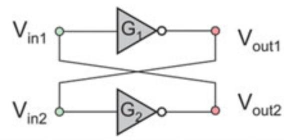
De Morgan's laws:

$A+B=\overline{\overline{A}\cdot\overline{B}},\ A\cdot B=\overline{\overline{A}+\overline{B}}$

(continued)

Latch (Transistor memory)





State	V_{in1}	V_{in2}	V_{out1}	V_{out2}
#1	1	0	0	1
#2	0	1	1	0

Problems

13.1 Principle of Operation

13.1.1 Switch Concept

13.1.2 Switch Position in a Circuit

13.1.3 MOSFET Switches

13.1.4 Sketch of Transistor Physics

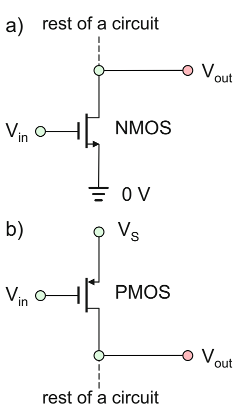
Problem 13.1. Describe the function and major properties of an electronic switch in your own words.

Problem 13.2.

A. Describe the meaning of the ground-side switch, the power-side switch, and the series switch. Why do we distinguish between those switch types?

B. Draw the circuit symbol for a switching NMOS transistor used in the ground-side switch. Draw the circuit symbol for a PMOS transistor used in the power-side switch. Designate the line current direction in both cases.

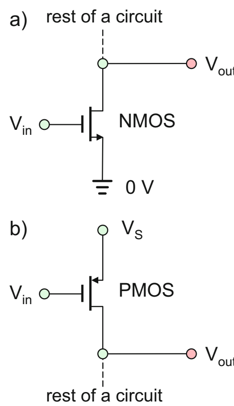
Problem 13.3. Two digital circuits shown in the following figure operate with a single-supply voltage $V_S = 1.8$ V. The transistor threshold voltages are $V_{\text{Tn}} = |V_{\text{Tp}}| = 0.5$ V, which correspond to a 0.18-μm CMOS process. Note: Every "CMOS process" is a manufacturing process for tiny MOSFETs used in digital circuits. A 0.18-μm CMOS means that the channel length (gate width) of the MOSFET in Fig. 13.5 is greater than or equal to 0.18 μm.



Find the output voltage V_{out} to each circuit if:

i. $V_{\text{in}} = 0.0\,\text{V}$
ii. $V_{\text{in}} = 0.2\,\text{V}$
iii. $V_{\text{in}} = 1.6\,\text{V}$
iv. $V_{\text{in}} = 1.8\,\text{V}$

Problem 13.4. Two digital circuits shown in the figure below operate with a single-supply voltage $V_{\text{S}} = 5.0$ V. The transistor threshold voltages are $V_{\text{Tn}} = |V_{\text{Tp}}| = 1.0$ V.

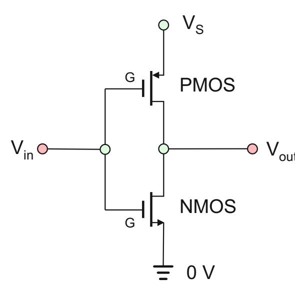


Find the output voltage V_{out} to each circuit if:

i. $V_{\text{in}} = 0.0\,\text{V}$
ii. $V_{\text{in}} = 0.7\,\text{V}$
iii. $V_{\text{in}} = 5\,\text{V}$
iv. $V_{\text{in}} = 4.6\,\text{V}$

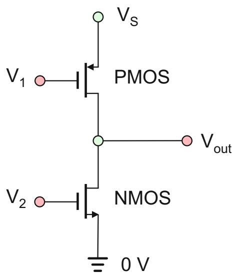
Problem 13.5. For the circuit shown in the figure below, $V_{\text{S}} = 2.5$ V and $V_{\text{Tn}} = |V_{\text{Tp}}| = 0.5$ V (0.25-μm CMOS process). Determine the output voltage V_{out} when:

A. $V_{\text{in}} = 0.0$ V
B. $V_{\text{in}} = 0.2$ V
C. $V_{\text{in}} = 2.3$ V
D. $V_{\text{in}} = 2.5$ V
E. $V_{\text{in}} = 1.0$ V



Problem 13.6. For the circuit shown in the figure below, $V_S = 2.5$ V and $V_{Tn} = |V_{Tp}| =$ 0.5 V (0.25-μm CMOS process). Determine the output voltage V_{out} when:

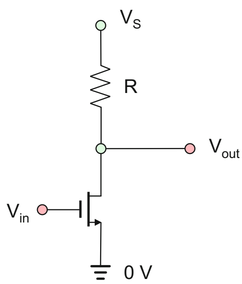
A. $V_1 = 0.0$ V, $V_2 = 0.0$ V
B. $V_1 = 0.7$ V, $V_2 = 0.2$ V
C. $V_1 = 2.3$ V, $V_2 = 2.3$ V
D. $V_1 = 2.3$ V, $V_2 = 0.0$ V
E. $V_1 = 1.0$ V, $V_2 = 1.0$ V



Problem 13.7. For the circuit shown in the figure below, $V_S = 2.5$ V and $V_{Tn} = 0.5$ V. Determine the output voltage V_{out} when:

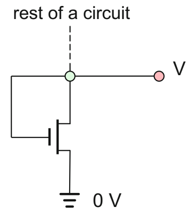
A. $V_{in} = 0.0$ V
B. $V_{in} = 0.2$ V
C. $V_{in} = 2.3$ V
D. $V_{in} = 2.5$ V

The output terminal is disconnected (current cannot flow into this terminal).

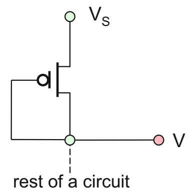


Problem 13.8. Draw two alternative circuit symbols for an NMOS switch. Repeat for the PMOS switch.

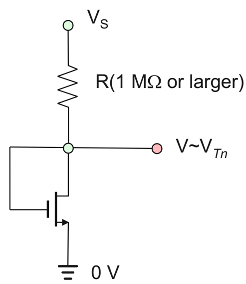
Problem 13.9. For the circuit shown in the following figure, determine all possible values of the voltage V. The transistor's threshold voltage is 0.5 V.



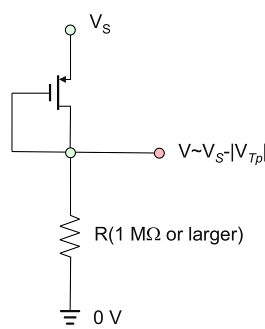
Problem 13.10. For the circuit shown in the figure below, determine all possible values of the voltage V. The transistor's threshold voltage is $|V_{Tp}| = 0.5$V; the supply voltage is 2.5 V.



Problem 13.11. A circuit shown in the figure below is used to measure the threshold voltage of the NMOS transistor. Could you explain why? *Hint:* Determine all possible values of the voltage V.



Problem 13.12. A circuit shown in the figure below is used to measure the threshold voltage of the PMOS transistor. Could you explain why? *Hint:* Determine all possible values of the voltage V.



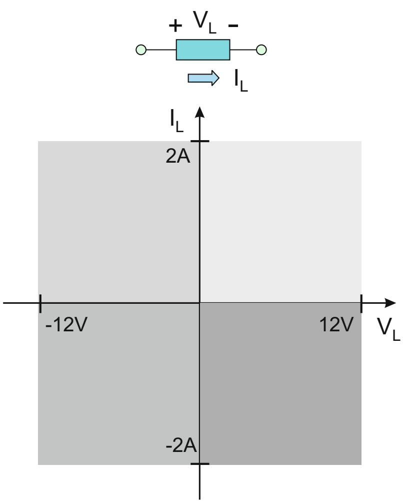
13.2 Power Switching Circuit

13.2.1 Switching Quadrants

13.2.2 Switching a Resistive Load

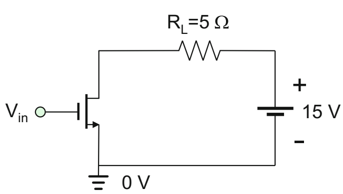
Problem 13.13. For a load shown in the figure below, determine the quadrant of operation when:

A. $V_L = -6\ \text{V}, I_L = -1\ \text{A}$
B. $V_L = 6\ \text{V}, I_L = 1\ \text{A}$
C. $V_L = 6\ \text{V}, I_L = -1\ \text{A}$
D. $V_L = -12\ \text{V}, I_L = -2\ \text{A}$



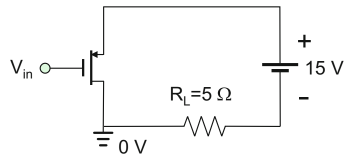
Problem 13.14. In a switching circuit shown in the figure that follows, an IRF510 n-channel power MOSFET with $V_{Tn} = 3.5\ \text{V}$ is used. Assuming zero switch resistance, determine the power delivered to the load when the control voltage is:

A. 0 V
B. 3 V
C. 12 V
D. 14 V



Problem 13.15. In a switching circuit shown in the following figure, a power MOSFET with $|V_{Tp}| = 3.5\ \text{V}$ is used. Assuming zero switch resistance, determine the power delivered to the load when the control voltage V_{in} is

A. 0 V
B. 2 V
C. 15 V
D. 12 V



13.2.3 Switching a DC Motor

13.2.4 One-Quadrant Switch for a DC Motor

Problem 13.16. Explain in your own words how switching a motor is different compared to switching a simple resistor load.

Problem 13.17. Explain in your own words the difference between the "free run to a stop" and "brake" states of a DC motor.

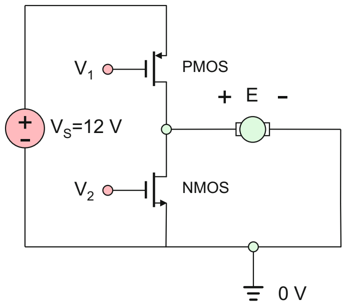
Problem 13.18. Prove that a DC motor load operates as a motor (passive load) in quadrants I and III in Fig. 13.8 and as a generator (active load) in quadrants II and IV.

13.2.5 Half H-Bridge for a DC Motor

13.2.6 Full H-Bridge for a DC Motor

Problem 13.19. For a half H-bridge shown in the following figure, $V_S = 12\ \text{V}$ and $V_{Tn} = |V_{Tp}| = 3.5\ \text{V}$. The control voltages V_1, V_2 may switch from 0 V to 12 V. Establish the values of two control voltages that ensure the following motor operations:

A. Motor is in forward mode (current direction through the motor is from left to right).
B. Motor suddenly stops (motor terminals are shorted out, which creates the braking effect).
C. Motor runs freely to a stop (motor is disconnected from the power supply).



Problem 13.20. In the half H-bridge circuit shown in the figure to the previous problem, the control voltages V_1, V_2 are either 0 V or 12 V. If we denote the 0-V control voltage by 0 (low) and the 12-V control voltage by 1 (high), all possible combinations of the control voltages are covered by the table that follows (the table in fact lists all *binary numbers* from 0 to 3). Fill out the table using four states:

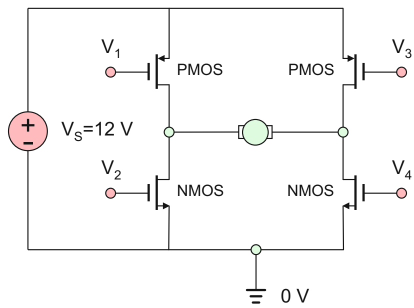
A. Forward mode (current direction is from left to right)
B. Brake
C. Free run to a stop
D. Forbidden (short circuit)

V_1	V_2	State
0	0	
0	1	
1	0	
1	1	

Problem 13.21. Suggest and sketch a schematic of the half H-bridge where three switching states (ON, brake, free run to a stop) are realized with only NMOS transistors.

Problem 13.22. For the H-bridge shown in the following figure, $V_S = 12$ V and $V_{Tn} = |V_{Tp}| = 3.5$ V. The control voltages may switch from 0 V to 12 V. Establish at least one set of particular values for four control voltages V_1, V_2, V_3, V_4 that ensures the following motor operations:

A. Motor is in forward mode (current direction through the motor is from left to right).
B. Motor is in reverse mode (current direction through the motor is from right to left).
C. Motor suddenly stops (motor terminals are shorted out, which creates the braking effect).
D. Motor runs freely to a stop (motor is disconnected from the power supply).



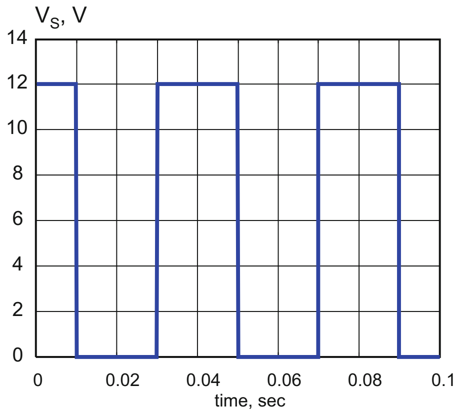
Problem 13.23. In the H-bridge circuit shown in the figure to the previous problem, the control voltages V_1, V_2, V_3, V_4 are either 0 V or 12 V. If we denote the 0-V control voltage by digit 0 (low) and the 12-V control voltage by digit 1 (high), all possible combinations of the control voltages are covered by the table that follows (the table in fact lists all *binary numbers* from 0 to 15). Fill out the table using five states:

A. Forward mode (current direction is from left to right)
B. Reverse mode (current direction is from right to left)
C. Brake
D. Free run to a stop
E. Forbidden (short circuit)

13.2.7 Application Example: Pulse-Width Modulation (PWM) Motor Controller

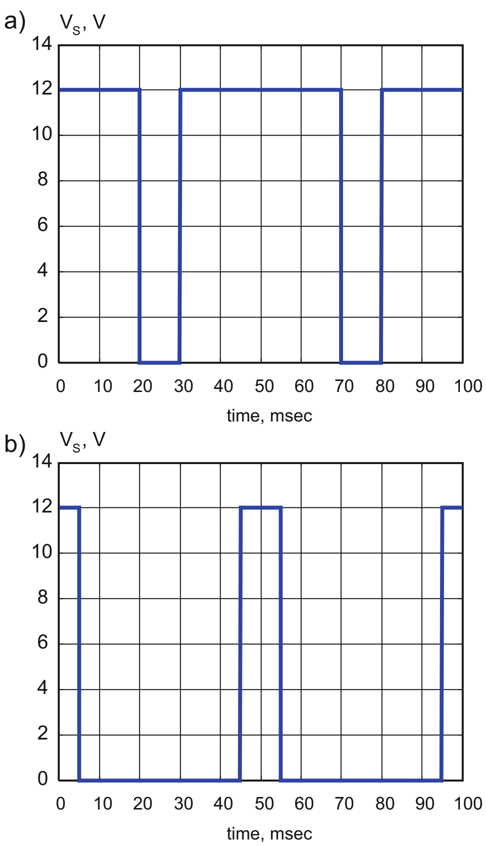
Problem 13.24. For a PWM form shown in the following figure, determine:

A. Period, T (show units)
B. Frequency, f (show units)
C. Duty cycle, d (also give its percentage D)
D. Average supply voltage, V_{DC}



Problem 13.25. For a PWM form shown in the following figure, determine

A. Period, T (show units)
B. Frequency, f (show units)
C. Duty cycle, d (also give its percentage D)
D. Average supply voltage, V_{DC}



Problem 13.26*

A. Compile a MATLAB script to generate the figure to Problem 13.24 above. Attach the script and the figure to the homework.
B. Compile two MATLAB scripts to generate the two figures to Problem 13.25 above. Attach the scripts and the figures to the homework.

13.3 Digital Switching Circuits

13.3.1 NOT Gate or Logic Inverter

13.3.2 NOR Gate and OR Gate

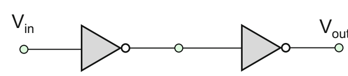
13.3.3 NAND Gate and AND Gate

Problem 13.27

A. Draw the symbol for the logic inverter (NOT gate).
B. Draw the corresponding circuit diagram.
C. Given the input voltage to the NOT gate, fill out the table that follows. The transistors used in the circuit are matched and have equal threshold voltages $|V_{Tp}| = V_{Tn} = 1$ V.

V_{in}	V_{out}
0.5 V	
4.7 V	

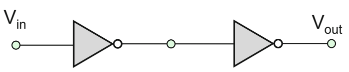
Problem 13.28. For the circuit shown in the figure, fill out the table that follows. The transistors used in the circuit are matched and have equal threshold voltages $|V_{Tp}| = V_{Tn} = 1$ V.



V_{in}	V_{out}
0 V	
5 V	

Problem 13.29. For the circuit shown in the figure, fill out the table that follows. The transistors used in the circuit are matched

and have equal threshold voltages $|V_{Tp}| = V_{Tn} = 1\text{V}$.

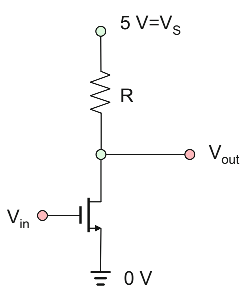


V_{in}	V_{out}
0.3 V	
4.2 V	

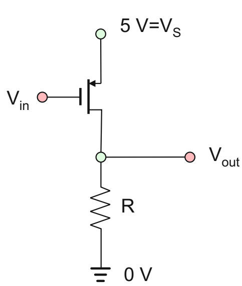
Problem 13.30. The circuit shown in the following figure is a logic gate. However, it utilizes only one transistor. The current cannot flow into the output terminal (it is disconnected in the figure). Construct:

A. Table of V_{out} versus $V_{in} = 0,\ 0.5,\ 4.5,\ 5\ \text{V}$
B. The truth table

given that the source voltage is 5 V and the threshold voltage is 1 V. What logic gate is it? What value of the resistor *R* would you choose to minimize circuit loss and the load impact?



Problem 13.31. Repeat the previous problem for the circuit shown in the following figure.



Problem 13.32. Draw the symbol for the logic OR gate and present the corresponding truth table.

Problem 13.33. Draw the symbol for the logic NOR gate and present the corresponding truth table.

Problem 13.34. Draw the circuit diagram:

A. For the NOR gate
B. For the OR gate

Problem 13.35. For the NOR gate with input voltages V_1 and V_2, fill out the table that follows. The transistors used in the circuit are matched and have equal threshold voltages $|V_{Tp}| = V_{Tn} = 1\ \text{V}$.

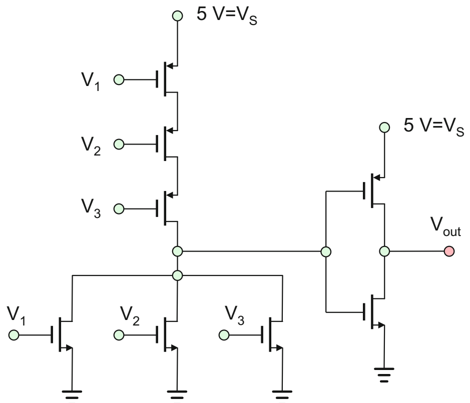
V_1	V_2	V_{out}
0.1 V	0.7 V	
0.5 V	4.9 V	
4.5 V	0.1 V	
4.1 V	4.4 V	

Problem 13.36. For the OR gate with input voltages V_1 and V_2, fill out the table that follows. The transistors used in the circuit are matched and have equal threshold voltages $|V_{Tp}| = V_{Tn} = 1\ \text{V}$.

V_1	V_2	V_{out}
0.3 V	0.1 V	
0.2 V	4.1 V	
4.1 V	−0.1 V	
5.3 V	4.4 V	

Problem 13.37. The following figure is an internal electric circuit of a logic gate. It has three inputs and one output.

1. Fill out the truth table.
2. Draw the symbol of the corresponding logic gate.



Problem 13.38. A freshman ECE student attends class if at least one of the following conditions is satisfied:

1. He/she feels that this lecture might be useful.
2. The lecture is not early in the morning.
3. His/her friends might be present there too.

Every morning he/she "votes" by simultaneously pushing any appropriate combination of three 5-V buttons (V_1, V_2, and V_3) placed in parallel. A logic circuit is needed that lights a green LED (outputs 5 V) when there is time to go to the lecture.

A. Draw the corresponding logic circuit in the symbolic form (in the form of logic gates).
B. Draw the MOSFET representation of that logic circuit.
C. Present the corresponding truth table.

Problem 13.39. Draw the symbol for the logic AND gate and present the corresponding truth table.

Problem 13.40. Draw the symbol for the logic NAND gate and present the corresponding truth table.

Problem 13.41. Draw the MOSFET representation

A. For the NAND gate
B. For the AND gate

How many transistors are we using in every case?

Problem 13.42. For the NAND gate with input voltages V_1 and V_2, fill out the table that follows. All transistors used in the circuit are matched and have equal threshold voltages $|V_{\text{Tp}}| = V_{\text{Tn}} = 1$ V.

V_1	V_2	V_{out}
0.9 V	0.9 V	
0.1 V	5.1 V	
4.1 V	–0.1 V	
4.5 V	4.7 V	

Problem 13.43. For the AND gate with input voltages V_1 and V_2, fill out the table that follows. The transistors used in the circuit are matched and have equal threshold voltages $|V_{\text{Tp}}| = V_{\text{Tn}} = 1$ V.

V_1	V_2	V_{out}
0.1 V	0.1 V	
0.2 V	4.2 V	
5.1 V	–0.1 V	
5.0 V	4.6 V	

Problem 13.44. A senior ECE student attends class if *all* of the following conditions are satisfied:

1. He/she feels that this lecture might be useful.
2. The lecture is not early in the morning.
3. His/her friends might be present there too.

Every morning he/she "votes" by simultaneously pushing any appropriate combination of three 5-V buttons (V_1, V_2, and V_3) placed in parallel. A logic circuit is needed that lights a green LED (outputs 5 V) when there is time to go to the lecture.

A. Draw the corresponding logic circuit in the symbolic form (in the form of logic gates).
B. Draw the MOSFET representation of that logic circuit.
C. Present the corresponding truth table.

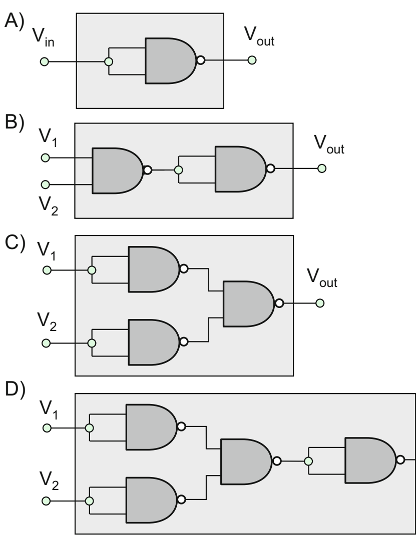
13.3.4 Simple Combinational Logic Circuits. Switching Algebra
13.3.6 Logic Circuit Analysis. Application Example: Logic Gate Motor Controller
13.3.7 Logic Circuit Synthesis

Problem 13.45. Draw a logic circuit with only NAND and NOT gate(s) that realizes an OR gate. Confirm your answer by using the corresponding truth table.

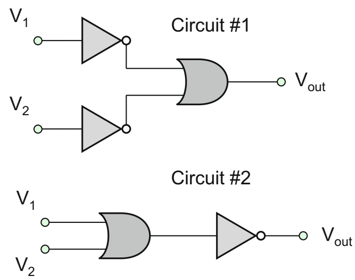
Problem 13.46. Draw a logic circuit with only NAND gate(s) that realizes an OR gate. Confirm your answer by using the corresponding truth table.

Problem 13.47. Draw a logic circuit with only NAND gate(s) that realizes a NOT gate. Confirm your answer by using the corresponding truth table.

Problem 13.48. Four logic circuits shown in the figure below use *only* the NAND gates. By constructing the truth table for every circuit, establish the equivalence of circuits A,B, C, and D to other logic gates studied in this section.

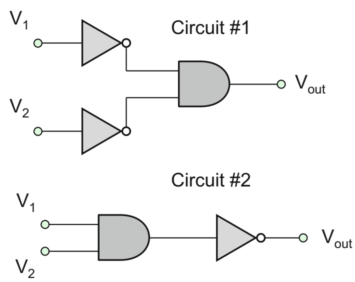


Problem 13.49. The following figure shows two logic circuits.



Are they equivalent? Prove your answer by constructing the two corresponding truth tables.

Problem 13.50. The following figure shows two logic circuits.



Are they equivalent? Prove your answer by constructing the two corresponding truth tables.

Problem 13.51. Using laws and rules of Boolean algebra, simplify the Boolean expressions

A. $A \cdot B + A \cdot (B + C) + B \cdot (B + C)$

B. $\left(A \cdot \overline{B} \cdot (C + B \cdot D) + \overline{A} \cdot \overline{B}\right) \cdot C$

Problem 13.52. Using laws and rules of Boolean algebra, simplify the Boolean expressions

A. $A + \overline{A} \cdot B$

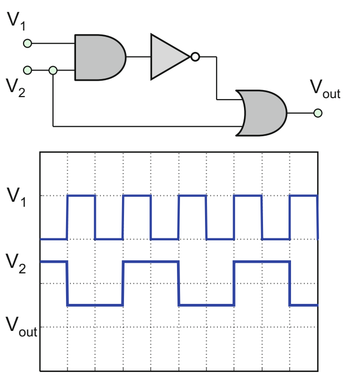
B. $(A + B) \cdot (A + C)$

Problem 13.53. The output of the XOR gate is given by $C = A \cdot \overline{B} + \overline{A} \cdot B$. Using De Morgan's theorems and laws and rules of Boolean algebra, express the output of the exclusive NOR gate, $\overline{C}$, in a similar form.

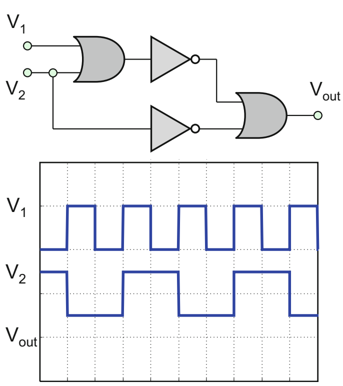
Problem 13.54. If AND gates are substituted in place of NAND gates in the logic circuit in Fig. 13.30c, will the motor controller still function properly? Explain why yes or why no.

Problem 13.55. If NOR gates are substituted in place of NAND gates in the logic circuit in Fig. 13.30c, will the motor controller still function properly? Explain why yes or why no.

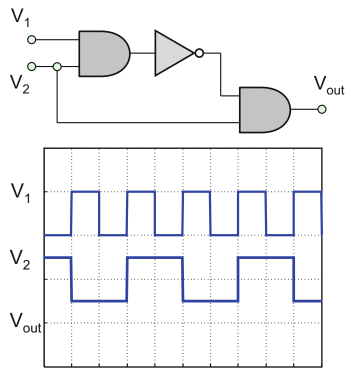
Problem 13.56. Given the logic circuit and the input waveforms in the following figure, draw the output waveform on the same figure. *Hint:* Construct the truth table of the logic circuit first.



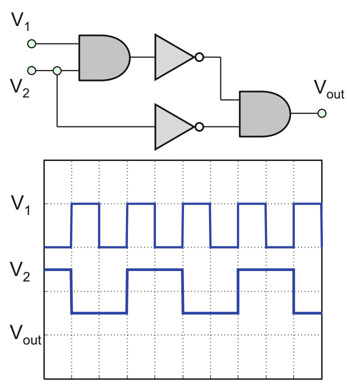
Problem 13.57. Given the logic circuit and the input waveforms in the following figure, draw the output waveform on the same figure. *Hint:* Construct the truth table of the logic circuit first.



Problem 13.58. Given the logic circuit and the input waveforms in the following figure, draw the output waveform on the same figure. *Hint:* Construct the truth table of the logic circuit first.



Problem 13.59. Given the logic circuit and the input waveforms in the following figure, draw the output waveform on the same figure. *Hint:* Construct the truth table of the logic circuit first.



Problem 13.60. A small county board is composed of three commissioners. Each commissioner votes on measures presented to the board by pressing a 5-V button indicating whether the commissioner votes for or against a measure. If two or more commissioners vote for a measure, it passes. You are asked to help with a logic circuit that takes the three votes as inputs and

lights a green LED (outputs 5 V) to indicate that a measure passed. You can use AND, NAND, and NOT logic gates, as many of them as you need.

A. Present the corresponding logic circuit in the symbolic form (in the form of logic gates).
B. Present the corresponding truth table.
C. How many transistors does your circuit include?

Problem 13.61. A small county board is composed of three commissioners. Each commissioner votes on measures presented to the board by pressing a 5-V button indicating whether the commissioner votes for or against a measure. If two or more commissioners vote for a measure, it passes. You are asked to help with a logic circuit that takes the three votes as inputs and lights a green LED (outputs 5 V) to indicate that a measure passed. You can use OR, NOR, and NOT logic gates, as many of them as you need.

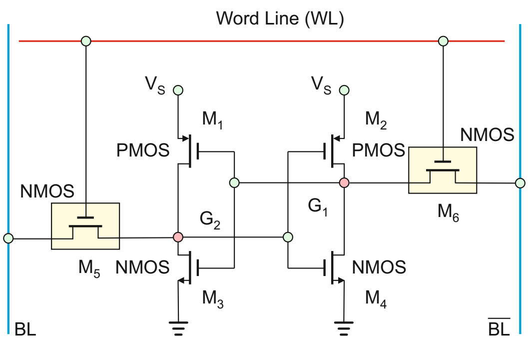
A. Present the corresponding logic circuit in the form of logic gates.
B. Present the corresponding truth table.
C. How many transistors does your circuit include?

13.3.8 The Latch

Problem 13.62. Draw the circuit diagram of a basic latch and explain its operation in your own words.

Problem 13.63. Most of the transistors are used in semiconductor memories. There are several types of semiconductor memories. One of them is the static RAM (SRAM) or the *static random access memory*. RAM means that every data bit is accessible any time unlike hard disk memory. SRAM cells provide the fastest operation among all other memories. The figure that follows shows a SRAM memory cell including:

1. The latch with four transistors.
2. A *word line* WL connected through two *access* NMOS *transistors* M_5, M_6. They are *always* turned on (become the short circuit) when the selected cell's word line is raised high (to V_S or another high voltage).
3. A *bit line* BL and its counterpart, another bit line $\overline{\text{BL}}$.



The following figure shows another attempt to design the SRAM memory cell with only four NMOS transistors. Will this design function? Why yes or why no?