Chapter 18
Power Conversion and Energy Management for Mission-Critical Systems

Andrei-Stefan Savu, Adrian-Ioan Lita, Constantin Radoi, Adriana Florescu, Sergiu Oprea and Ioan Lita

Abstract The need for high power density has been the trend of the power conversion industry for many years. The key to obtain a high power density is to increase system's efficiency. In the case of space applications, there is the same need for high power density but with the very important note that the reliability of the system must not be compromised. In order to increase system's efficiency while maintaining reliability, the latest soft switching converter topologies, high power density packaging, improved heat extraction and planar magnetics are used. Other key parameters are: the digital loop control and the digital energy management through microcontrollers, and digital signal controllers.

Keywords Mission-critical systems · Planar transformer technology · Variable width winding method · Adiabatic point of load · Quasi resonant flyback · Two transistor forward and LLC converters · Intermediate bus converter · Very small satellites

A.-S. Savu · A.-I. Lita · C. Radoi · A. Florescu (✉) · S. Oprea
University Politehnica of Bucharest, Bucharest, Romania
e-mail: adriana.florescu@yahoo.com; adriana.florescu@upb.ro

A.-S. Savu
e-mail: savucfa@yahoo.com

A.-I. Lita
e-mail: adrian.lita@ieee.org

C. Radoi
e-mail: conrad_1944@yahoo.com

S. Oprea
e-mail: oprea_serg@yahoo.com

I. Lita
University of Pitesti, Pitesti, Romania
e-mail: ioan.lita@upit.ro

N. Bizon et al. (eds.), *Energy Harvesting and Energy Efficiency*,
Lecture Notes in Energy 37, DOI 10.1007/978-3-319-49875-1_18

List of Abbreviations and Acronyms used:

ASM	Assembly
BGA	Ball Grid Array
CT	Copper Thickness
DCM	Discontinuous Conduction Mode
DRIBA	Double Regulated Intermediate Bus Architecture
EMP	Electromagnetic Pulse
ESA	European Space Agency
ESR	Equivalent Series Resistance
FEA (FEM)	Finite Element Analysis (Finite Element Method)
GaN	Gallium Nitride
ICs	Integrated Circuits
LET	Linear Energy Transfer
MPPT	Maximum Power Point Tracking
MTBF	Mean Time Between Failures
ORING	OR-ing Output Logic Function
PCB	Printed Circuit Board
PI	Proportional Integral
PID	Proportional Integral Derivative
POL	Point Of Load
POU	Point Of Use
PWM	Pulse Width Modulation
RF	Radio Frequency
RMS	Root Mean Square
SEB	Single Event Burnout
SEBP	Single Event Burnout Phenomenon
SEE	Single Event Phenomenon
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SEU	Single Event Upset
SGEMP	System Generated EMP
SMPS	Switched Mode Power Supply
TID	Total Ionizing Doze
VRM	Voltage Regulated Module
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

A mission-critical system represents a system whose failure due to any part of it (a procedure, process, software, hardware such as an equipment, etc.) would compromise the whole mission and the organization as well. On Earth, examples of mission-critical systems are: the online banking system, railway and aircraft operating and control system, electric power systems, computer systems whose collapse would seriously affect the organization or, worse, the whole society.

In space, examples of a mission-critical system are: the navigation system for a space mission, or the electric power system (conversion and management).

Electrical energy is one of the vital elements in keeping a satellite operational in orbit. Solar panels convert solar energy into electrical energy. From there, the electrical energy is processed, stored, regulated and distributed to electronic loads which consist mainly of analog and digital semiconductors, RF, optical, sensors, lasers and electromechanical devices. To underline the importance of the electrical power system in space applications as a mission-critical system whose failure would compromise the whole mission of any satellite, European Space Agency (ESA) briefly states that "a satellite without electricity is nothing but space junk" [1].

In Chap. "Power Architectures and Power Conditioning Unit for Very Small Satellites", an introduction in very small satellites (characteristics, Earth orbits and eclipses, Cube Sats brief presentation and missions) was made and some blocks of the electrical power system were discussed (the solar array, batteries for space applications, space power architectures, maximum power point tracker) and developed (the flexible architecture of the power conditioning unit). In this chapter focused on space power conversion units and energy management strategies, a brief presentation of space requirements for power conversion is introduced and the advanced technology of planar transformers—as part of the power conversion units—is detailed. Then, all the other remaining blocks of the satellite's electrical power system from the above mentioned chapter (the intermediate bus converter and the adiabatic point of load power converter) are developed, together with the power management block that links all the component blocks in both chapters. In the end, the original prototype of the whole energy management system for a very small satellite application is exposed, as the best obtained variant of practical demonstrator for the architectures, technologies, algorithms, methods, devices etc. presented in both chapters.

18.1 Overview of Space Requirements for Power Conversion Units

The technology of power electronics for space applications has special peculiarities. The most remarkable difference between power electronics for space and the terrestrial environment one consists of space radiation. Power semiconductor devices such as MOSFET can fail after exposure to heavy ions due to SEGR (single event gate rupture) or SEBP (single event burnout phenomenon). Also controlling semiconductor integrated circuits (Ics) such as microcontrollers, microprocessors, analog to digital converters and sensors can suffer from heavy ions exposure, causing faulty data which may lead to catastrophic failure. To stress this even further, just considering one single bit alteration in the microcontroller's memory can lead to abnormal behavior of the control system, which can distort the control loop, which in the end may lead to damaging the electronic loads.

Converters are generally required to operate continuously in the radiation environment without damage and performance degradation with accumulative total ionizing doze (TID) in the range of 2–3 kiloradiatios (Krads) to 100 Krads or more. TID level is mission dependent. Also required is the converter's ability to survive and recover from singe event phenomena (SEE), e.g. single event upset (SEU), single event latch up (SEL) and single event burnout (SEB). The typical SEE level is linear energy transfer (LET) or 37–83 meV-cm^2/mg. SEE level is mission dependent, too. Other radiation requirements may include performance under neutron, proton, and high doze rate radiation. However, these requirements are unique to strategic weapon applications. Table 18.1 lists the typical requirements of a space DC-DC converter [2].

Unlike terrestrial applications, where mass and volume may not always be a big concern, space applications require the most compact and light design possible,

Table 18.1 Typical requirements of a space DC-DC converter

Parameter	Typical requirement
Electrical	
Input voltage	28 V unregulated; 50, 70 and 100 V regulated
Input inrush current	Required at the system level, but frequently flowed down
Output	Single, dual or triple
Output 1 (main)	+1.0 to +15 V
Output 2	+5 to +15 V, 5 to 15% of total output power
Output 3	−5 to −15 V, 5 to 15% of total output power
Output power	A few watts to 40 watts
Input-output isolation	Required
Output ripple	20 to 50 mVp-p typical, 1–5 mVp-p for some RF applications
Efficiency	50−70% for 5−15 W, and 70−90% for 15−40 W
EMI	Conducted emission (CE) and conducted susceptibility (CS) requirements modified versions of MIL-STD-461C/D/E
Overvoltage protection	Yes, shut down, limit 10−20% above Vnom (generally required for redundant applications)
Turn-on overshoot	<5% Vnom, output rises monotonically
Turn-on delay time	0.5 to 10 mS
Bus current telemetry	At the system level
Step load response	<2–5%, < 200–500 μS, half-load/full-load
Output telemetry	Yes
Temp telemetry	Required on some programs
Remote sense	Required for main output
Synchronization	Yes
Undervoltage lockout (UVLO)	Yes
Soft start	Yes

(continued)

Table 18.1 (continued)

Parameter	Typical requirement
On/Off command	Yes, bi-level or pulse command
On/Off status telemetry	Yes
Output voltage adjustment	Yes
Derating	NASA PPL-21/MIL-STD-1547/MIL-STD-975/ESA PSS-01-301
Mechanical/Environment	
Operating temp	−34 to +71 C qualification, program dependent, often has a wider temperature range for qualification level than acceptance requirement of flight hardware
Storage temp	−40 to +85 C, typical, program dependent
Random vibration	Dependent of launch platform
Pyrotechnic shock	Dependent of launch platform
Acceleration	Dependent of launch platform
Humidity	60–95% RH
Explosive atmosphere	Shall not cause ignition
Size	Key design requirement
Mass	Key design requirement
Qualification	MIL-PRF-38534, Class K
Package construction	Hermetically sealed thick film hybrid
Radiation	
Total ionizing dose (TID)	25 to 100 Krads, may be with shielding
Single event effect (SEE)	37–83 meV-cm^2/mg, shall not sustain permanent damage from cosmic ray or performance degradation from SEE: no SEU, no SEB, no SEGR, no SEL, no SET
Neutron	If required, shall be designed to withstand, without permanent performance degradation after exposure to neutron equivalent influence of $\leq 5 \times 10^{12}$ n/cm^2
Dose rate upset/recovery	Classified, x to y rad(si)/s, recover autonomously
Dose rate survival	If required, shall not sustain permanent damage or permanent performance degradation after exposure to dose rate of X $\leq$ rad(si)/s. The pulse has FWHM (full-width half-maximum) of 18–100 nS
Dose rate operate thru	If required, must operate thru after exposure to X $\leq$ rad(si)/s
Electromagnetic pulse (EMP)	If required, is designed to prevent EMP, hardening techniques are required
System-generated EMP (SGEMP) burnout	If required, is designed to prevent SGEMP burnout, hardening techniques are required
Enhanced low dose rate effects (ELDRS)	5 to 10 mrads/s, becoming a standard

which is also true for military and aerospace applications. Some aerospace power system designs are also suitable for satellite use. Specific power/energy per unit mass is defined as power-to-weight ratio.

Power system's thermal dissipation is a limiting parameter for power electronics design. Unlike the design for terrestrial applications, there is no atmosphere which leads to no convection process in outer space. Only conduction and radiation cooling can be used, which makes a lot of cooling methods unavailable in space applications.

Space power systems must be very reliable, must maintain their functionality and have failure isolation capability. Power system failures can be temporary or permanent. Temporary failures include overheating and non-damaging memory corruption due to radiation. Overheating can be addressed by the controller through power derating or temporary latch. Memory corruption can be addressed by a governing watchdog which reboots the process when corruption is detected. In order to prevent permanent failures, key system parameters are closely monitored by the controller. Such parameters include temperatures in key component areas, memory coherence, voltage and current levels and power levels. The controller makes judgments to implement predictive maintenance. The mean time between failures (MTBF) calculation of such a power systems should exceed the mission lifetime. To successfully implement this, the individual components' electrical and thermal derating levels must be kept lower than the terrestrial 80%.

Some electronic components are restricted for space usage due to their inherent small lifetime. Such components, especially electrolytic and film capacitors, must be replaced by ceramic, tantalum or mica capacitors. Optoelectronic devices are also restricted for space usage due to electroluminescent effects caused by radiation. For mechanical restrictions, vibrations and thermal cycles impose larger footprints and components that are not soldered underneath. For example, chip film resistors and ceramic capacitors have a minimum footprint of 0805. For controller ICs, the footprint should be SOIC, TQFP or larger. Accepted transistor footprints are TO-252 or larger.

18.2 Technological Trends of High Power Density Converters for Space Applications

For the last few decades the focus of power subsystems development and advancement has revolved around the needs and requirements of large high power missions, mainly for telecommunication applications. The challenges to increase efficiency and simultaneously to reduce mass and volume in this application are valid, but for small satellite missions these challenges have been overlooked. From the power system's perspective, it is safe to say that the power challenges and requirements are common across the full spectrum of small satellite missions. Small satellites can have a range of power requirements from as little as 1 or 2 W to a few kW. As a result, there is a need for the power systems' electronics to be compatible with a multitude of mission profiles and to be scalable in power handling capability.

The trends presented in this chapter are focused on planar magnetics and their variable width winding structures, which are very good candidates for various power supply applications, including space power converters.

18.2.1 Variable Width Winding Concept Summary

Power density (or volume power density, or volume specific power) is the amount of power (time rate of energy transfer) per unit volume. The trend toward high power density, high operating frequency, and low profile in power converters determined the appearance of limitations regarding the use of conventional wire-wound transformers. An alternative to conventional wire-wound transformers are planar transformers, which exhibit a unique set of advantages: good thermal characteristic, higher power density and low leakage inductance. The increase of power density is obtained by increasing the switching frequency which decreases the size of the passive components. However, this increase of the switching frequency creates a different set of problems regarding the skin and proximity effects of the transformer windings, especially with frequencies over 100 kHz [3]. The finite element analysis simplifies the computation of the DC and AC losses in the windings. Also analytical approach is presented in [4]. In [5] a comparison between simulation and analytical results for magnetic components is made. Windings with variable width turns are considered in [6], but they are not experimentally confirmed. The limitations of planar transformer designs are the subject of [7, 8].

In this chapter the DC and AC resistance of the windings have been analyzed via a finite element analysis, and a novel variable width winding concept is compared to the fixed with winding approach. The variable winding widths are chosen so the winding exhibits the same DC resistance per turn and so balancing the magnetic flux. This optimized variable width winding brings an improvement at DC and AC frequencies. Combined with a 10 W LLC application, the classical constant width and variable width windings are compared and the detailed experimental results are shown.

18.2.2 Design with Constant Width Planar Winding

The design process for a constant width planar winding is very straight forward. According to the desired application, the core size and type are chosen in the beginning. For a 10 W LLC converter, a Ferroxcube E32/6/20 3F3 core meets the requirements. The turn ratio of the transformer according to the input and output voltage needs are $N_p = 6$ turns for the primary and $N_s = 2$ turns for the secondary. The design has a 2 layer structure with the primary and secondary windings on separate layers.

For the E32/6/20 core, the winding window is 9.19 mm. The effective winding window is obtained by introducing 0.5 mm of tolerance in each side resulted from the ferrite core and PCB manufacturing tolerances. The resulted effective winding window is wind = 8.19 mm.

Building the transformer on a 2 layer structure assumes that the copper thickness (CT) should be set to a typical printed circuit board (PCB) manufacturer capability of 3 oz. This thickness dictates the distance between turns (x), which will be x = 0.3 mm. The primary winding width will be:

$$W_{prim} = \frac{wind - (N_p - 1) \cdot x}{N_p}, \tag{18.1}$$

which computes to W_{prim} = 1.115 mm.

Starting from (18.1), a similar equation for the secondary winding constant width can be found:

$$W_{sec} = \frac{wind - (N_s - 1) \cdot x}{N_s}, \tag{18.2}$$

resulting in W_{sec} = 3.945 mm.

Once the winding widths have been determined, in order to calculate the DC resistance, the windings length has to be determined. Due to the shape of the ferrite core, the winding has a rectangular shape. Additional parameters need to be defined the winding length calculation (Fig. 18.1) are: t—turn number, L—center core leg length, l—center core leg width, L_t—partial winding length, l_t—partial winding width.

The partial long length for a turn t is:

$$L_t = L + 2t \cdot w + (2t - 1) \cdot x \tag{18.3}$$

and for the short length t is:

$$l_t = l + 2t \cdot w + (2t - 1) \cdot x \tag{18.4}$$

Equations (18.3) and (18.4) apply for primary and secondary constant width windings and combining them the total length for t = 6 turns primary winding can be determined:

$$L_{totalprim} = 2 \cdot \left(\sum_{t=1}^{N_p} L_t + \sum_{t=1}^{N_p} l_t \right) \tag{18.5}$$

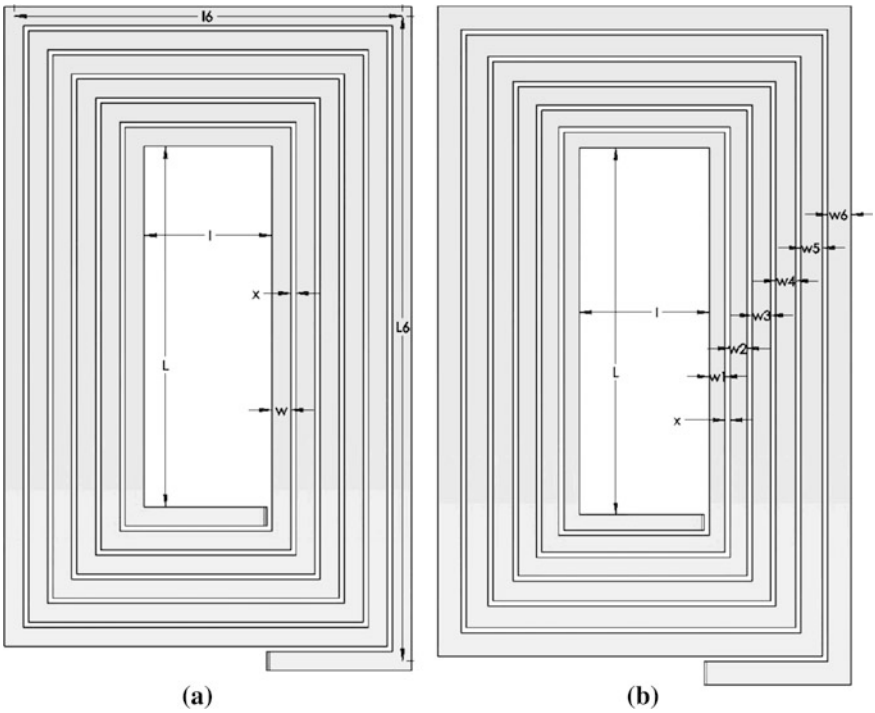


Fig. 18.1 Constant width primary winding (**a**), variable width primary winding (**b**)

The total length for t = 2 turns secondary winding is:

$$L_{totalsec} = 2 \cdot \left(\sum_{t=1}^{N_s} L_t + \sum_{t=1}^{N_s} l_t \right) \tag{18.6}$$

From (18.5) and (18.6) the following lengths are obtained: $L_{totalprim}$ = 549.45 mm and $L_{totalsec}$ = 188.81 mm.

Following the results from (18.1), (18.2), (18.5) and (18.6) the DC resistance of the windings is calculated considering the copper thickness CT:

$$R_{primcons} = \rho \cdot \frac{L_{totalprim}}{CT \cdot W_{prim}}, \tag{18.7}$$

where $\rho = 1.724 \cdot 10^{-8}$ Ωm is the copper resistivity. A similar equation is defined for the secondary winding:

$$R_{sec\ cons} = \rho \cdot \frac{L_{total\ sec}}{CT \cdot W_{sec}} \tag{18.8}$$

The DC resistances for the constant width design will be: $R_{primcons} = 59.727$ mΩ and $R_{sec\,cons} = 5.801$ mΩ.

18.2.3 Proposed Design with Variable Width Winding Method

The variable with winding design begins with the assumption that the resistance of each turn is equal to each other. By maintaining this assumption, the flux is balanced between the windings having the same current flowing through each turn. For simplicity only the primary winding will be a variable width. In Fig. 18.2 the complete transformer assembly is shown.

Step 1: Design starts by choosing the width of the first inner turn $w_1 = 0.9$ mm, according to [6]. This will be a temporary value and will be adjusted. In order to comply with the maximum winding space the following in equation must be fulfilled:

$$\left(N_p - 1\right) \cdot x + \sum_{t=1}^{6} w_t \leq wind, \tag{18.9}$$

meaning that the sum of all widths and winding distances must not exceed the maximum winding window. The relation between widths will be dictated by a multiplier coefficient y, as it follows:

$$\begin{cases} w_1 = 0.9 \text{ mm} \\ w_2 = w_1 y \\ \cdots \\ w_n = w_{n-1} y \end{cases}, \tag{18.10}$$

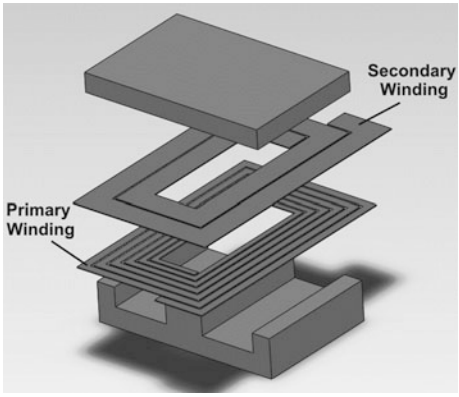


Fig. 18.2 Two layer transformer assembly

where $y = 1.085$ is chosen for N_p = 6 turns and winding window of wind = 8.19 mm to satisfy (18.9). Based on the calculations above the temporary winding widths can be determined.

Step 2: Is to calculate the winding lengths, using the same (18.3) and (18.4) as for the constant with design. Since the resistance of each turn needs to be calculated, the average length of each turn, which is a similar calculation to the (18.3)–(18.5) but with a variable with introduced, is calculated:

$$Lavg_t = 2 \cdot [L + 2t \cdot w_t + 2 \cdot (2t - 1) \cdot x + l_t + l + 2t \cdot w_t] \tag{18.11}$$

Having the widths and average lengths of each turn calculated the resistance per turn is:

$$R_t = \rho \cdot \frac{Lavg_t}{CT \cdot w_t} \tag{18.12}$$

Step 3: Is to equalize the resistances. The simplest way of doing this is by using a mathematical calculation program like Mathcad and use (18.9), (18.10), (18.11) and (18.12). Two parameters can be adjusted: the inner winding with w_1 and the multiplier coefficient y. When the two conditions are fulfilled (the resistance is the same per turn and the maximum winding window is not exceeded), the calculation is over. For a six turn variable winding, the winding resistances per turn results are as follows:

$$R_1 = 8.781\ \text{m}\Omega, \quad R_2 = 8.707\ \text{m}\Omega, \quad R_3 = 8.628\ \text{m}\Omega$$
$$R_4 = 8.545\ \text{m}\Omega, \quad R_5 = 8.458\ \text{m}\Omega, \quad R_6 = 8.368\ \text{m}\Omega$$

The total DC resistance for the variable with is be: $R_{primvar} = 57.487\ \text{m}\Omega$.

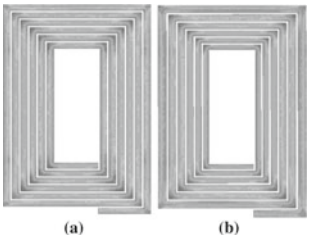
18.2.4 Comparisons Between Designs via FEA Simulations

As a result from subchapter above, the DC resistance of the proposed variable width design has a 3.5% lower resistance that the constant width design. A finite element analysis is performed on the constant width and variable width designs. An AC magnetostatic solver is used. The excitation is a sinusoidal current of 1A peak amplitude which applies to both primary and secondary windings.

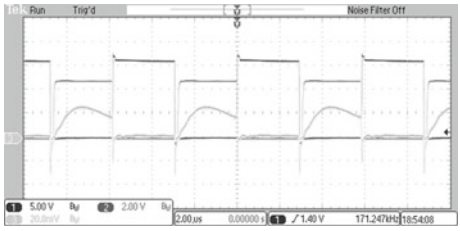
At a first instance to obtain the DC resistance of the windings, the solver frequency is set to 0 Hz. To solve for skin and proximity effects the solver frequency has to be the operating design frequency of the converter, in our case 170 kHz. The result is an impedance matrix containing the resistance, inductance and coupling at the solver frequency. Results of FEM simulations are provided in Table 18.2.

Table 18.2 DC resistance AC resistance inductance coupling

Symbol	Constant width primary	Variable width primary	Secondary
R_{DC} (mΩ)	61.4	59.3	6.06
R_{AC} (mΩ)	148.26	144.1	17.492
L_p (uH)	16.029	16.009	
k	0.96901	0.96931	



Current density plots for:
(a) constant width;
(b) variable width primary windings



(c) Key waveforms of an experimental half bridge 10W LLC converter with a variable winding planar transformer structure

Fig. 18.3 Design results for constant and variable width primary windings

In order to avoid the saturation of the core a small distributed air gap is introduced. The simulation results from Table 18.2 are performed with a core gap of 0.22 mm. To make a proper comparison between the two winding designs, it is critical that the windings have to be at the same distance to the core gap. If the winding is placed closer to the gap, the AC effects increase due to the magnetic field cutting into the copper.

Following the results of Table 18.2, a 2.8% improvement of the variable width design is noticed in the primary winding resistance at 170 kHz frequency compared to the constant width design. There is a good agreement between the simulated results and Chap. 2.2 theoretical results for the DC resistance. In Fig. 18.3 the current density plots of the primary windings for both designs are presented where almost no difference in current density for the variable width design is noticed, meaning that there are no strangulation points with the variable width turns.

18.3 Intermediate Bus and POL Architectures, Topologies and Control Mechanisms

18.3.1 Intermediate Bus and POL Architectures

The purpose of the intermediate bus converter is to be a buffer between the solar array, battery and point of load converters.

Figure 18.4 shows the relationship between the input stage DC-DC converter and the output stage DC-DC POL. The figure depicts three types of voltage relations between these two: (a) regulated intermediate bus, (b) unregulated intermediate bus and (c) double regulated intermediate bus [9]. In the case of regulated intermediate bus, the input stage converter regulates the bus voltage (Vib) via a feedback loop. The output stage converter operates at fixed parameters (duty cycle and frequency). In the case of unregulated intermediate bus, the input stage converters operate at fixed parameters (duty cycle and frequency) and the output stage converter regulates the load voltage via a feedback loop. In the case of double

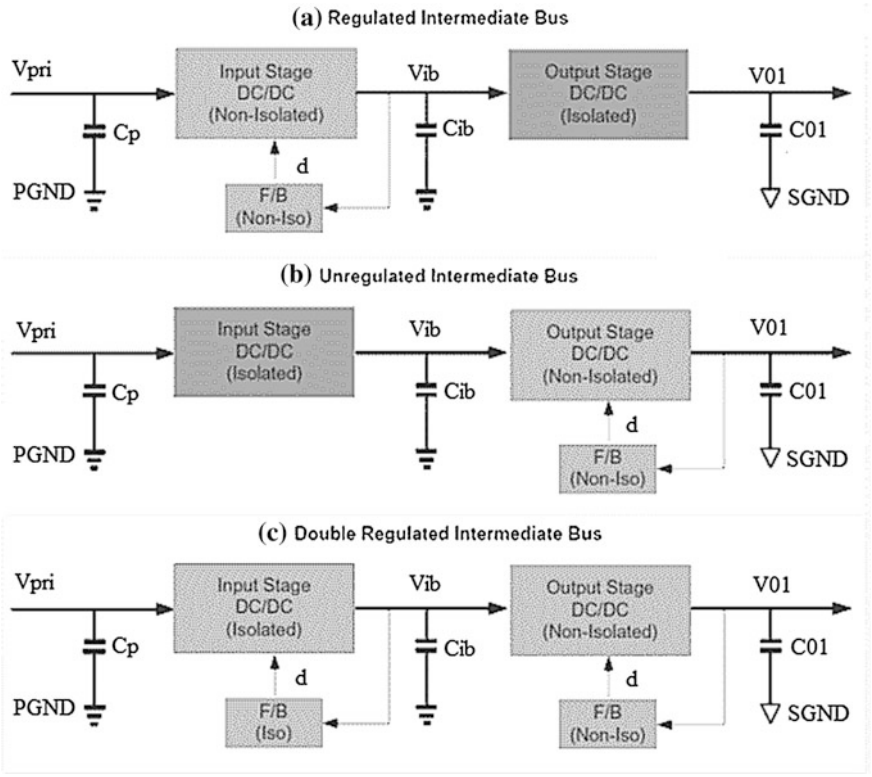


Fig. 18.4 Intermediate Bus and POL architectures

regulated intermediate bus the input stage converter regulates the voltage using a feedback loop and the output stage converter also regulates the load voltage using its own feedback loop. For output voltage requirements of ±10%, the regulated intermediate bus can be used, while the unregulated intermediate bus is capable of ±5% regulation. For a regulation of lower than ±5%, double regulated intermediate bus (DRIBA) is preferred, due to its increased transient capabilities.

Depending on the input voltage range and/or input voltage regulation or quasi-regulation, there are several possible topologies for this type of application and all of them are isolated DC-DC converters. The most used topology is the two Transistor Forward but new cutting edge topologies which obtains higher efficiency include Critical Conduction Flyback and LLC that will be also discussed further.

18.3.2 Two Transistor Forward Converter

The two switch forward converter is chosen as a classical candidate because it is considered to be one of the most reliable converters yet. Its benefits include the following: bulletproof operation (no timing issues or dead time requirements and no chance of shoot-through), no MOSFET body-diode conduction under any condition, no snubber circuitry required, the voltage stress on the main MOSFETs is limited to the maximum supplied voltage and simplicity of operation over a wide range of input voltages and load conditions.

Some of the few drawbacks of the two transistor forward topology are that it requires two transistors and two fast recovery diodes. It also requires a larger transformer and output inductor.

It is falsely stated in many application notes [9, 10] that this topology can't operate in zero-voltage switched (ZVS) mode. ZVS is easily achieved by controlling the amplitude of the primary magnetizing current. Slight modulation in switching frequency enables the control of the magnetizing current. The transfer function equation for the two transistor forward is:

$$V_{out} = Eff \cdot V_{in} \cdot D \cdot N, \tag{18.13}$$

where: V_{out}—the output voltage, Eff—the targeted efficiency, V_{in}—the input voltage, D—converter's duty cycle, N—the transformer turns ratio.

The popular power levels chosen for this converter are in the range of 150 to 750 W. The basic operation is as follows: Fig. 18.5a shows transistors Q1 and Q2, which turn on together transferring energy through the transformer's primary to the secondary. On the secondary side, the forward rectifying diode conducts, transferring energy into the output filter and load.

When transistors Q1 and Q2 are turned off, the transformer magnetizing current flows through the now forward biased diodes D1 and D2 and then back into the source, as shown by Fig. 18.5b. The diodes conduct until all the magnetizing energy in the primary along with energy stored in the leakage inductances is

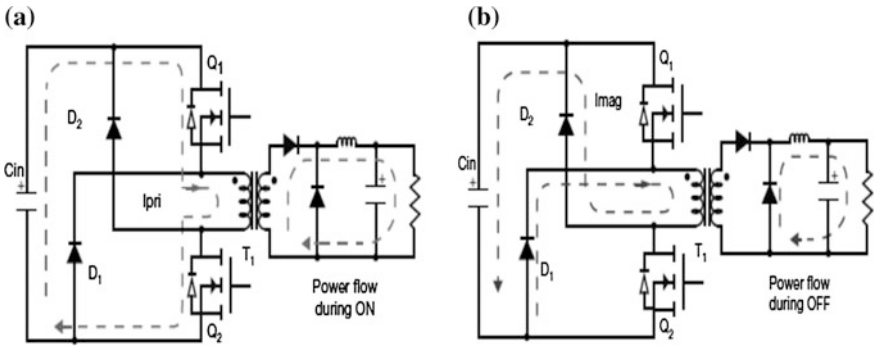


Fig. 18.5 **a** Power transfer stage of operation; **b** Power flow from output cap to power load

returned to the input supply. Since diodes D1 and D2 clamp the input voltage, no snubber circuits are required. On the secondary side, the forward rectifying diode conducts, transferring the output inductor stored energy into the load.

During the non-power delivery cycle of the primary, proper transformer reset time is achieved when the on-time is less than its off-time. As a result, the primary winding itself acts as the reset winding. Having the off-time longer than the on-time, the transformer will always reset. For this reason, the duty cycle of the two switch forward converter does not exceed 50%.

As for any isolated DC-DC converter, a proper design begins with the transformer, which is typically the main source of efficiency loss in the system. In the case of the two switches forward, the full input voltage is applied on the primary winding for a certain amount of time. In this case, the cross-section and core volume of the transformer have to be chosen in such a way to minimize core loss and copper loss. A good transformer design will have similar copper and core loss values. Transformer leakage inductance has to be minimized by winding interleaving techniques since the leakage is decreasing the effective duty cycle.

The output inductor contains in most of the cases only DC current since the AC current amplitude is small. As a result, the inductor flux swing is low and core loss is negligible. Copper losses can be optimized by carefully designing the inductor.

The two primary switches have conduction losses and switching losses. Switching losses are depending on the chosen switching frequency and imposes a limitation in increasing it. The two primary clamping diodes typically exhibit low conduction losses. The rectifier diodes in the secondary side exhibit conduction losses and reverse recovery losses. They can be replaced with synchronous rectifiers which increase the system efficiency but also complicate the driving circuitry. The output capacitors exhibit ESR conduction losses especially when there is a high AC current ripple in the output inductor.

18.3.3 Quasi Resonant Flyback Converter

The classical flyback topology has a fundamental advantage over all other isolated topologies: its ability to operate over large input voltage ranges. This may easily apply to our satellite power system since the solar panel output voltage varies with sunlight, eclipses and temperature. The typical power levels for this converter are in the range of 5 up to 150 W.

The flyback converter operating in continuous conduction mode has several fundamental problems, which are: the leakage inductance voltage spike occurring on the main primary switch, transformer with typically low efficiency due to high AC losses, high switching losses in the main switch and reverse recovery losses in the secondary rectifier. However, the small component count makes this topology very desirable, since the mass and volume, which are key parameters in satellite applications, are lower than for other topologies [11].

Figure 18.6a depicts the flyback converter schematic. To improve the converter's efficiency the converter is operated in discontinuous conduction mode (DCM). This flyback converter is called quasi-resonant flyback or variable frequency flyback or valley switching flyback, and this is largely used in low power switched mode power supply (SMPS) applications such as chargers, adapters and auxiliary supplies. This is also a good candidate for the intermediate bus converter.

The converter stores energy in the primary magnetizing inductance with the main switch is on. In the meantime, output voltage is supplied by the output capacitor and the energy from the secondary winding. When the energy in the secondary winding is depleted, the output voltage is supplied only by the output capacitors. During this period, because the primary switch is off and the secondary rectifier is not conducting, there will be a ringing between the transformer leakage inductance, transformer intra-winding capacitance and the switch's output capacitance, as in Fig. 18.6b.

The voltage across the main switch will experience a minimum valley point, whose minimum value will depend on the flyback reflected voltage. By turning on the main switch at this minimum valley, the flyback is called quasi-resonant or

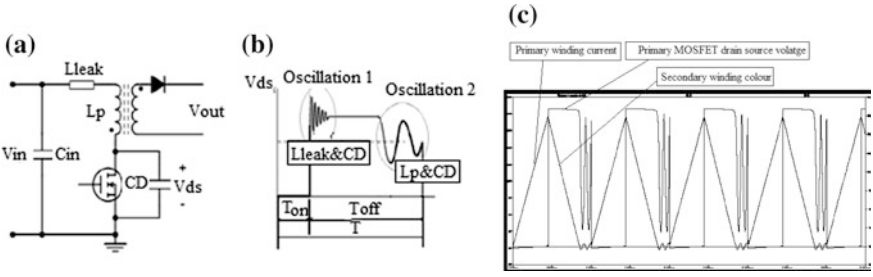


Fig. 18.6 **a** Flyback converter schematic, **b** VDS waveforms of a DCM flyback, **c** Ltspice operation waveforms for V_{in} = 50 V, P_{out} = 50 W

valley switching flyback. To maintain this operation mode, the frequency is adjusted depending on the load.

The transfer function equation of the DCM flyback is:

$$V_{out} = V_{in} \cdot N \cdot D \cdot \sqrt{\frac{R_{load}}{2 \cdot L_p \cdot f_{sw}}}, \tag{18.14}$$

where: V_{out}—the output voltage, V_{in}—the input voltage, N—the transformer turns ratio, D—converter's duty cycle, R_{load}—the converter load resistance, L_p—the primary inductance value, f_{sw}—the converter's switching frequency.

One of the most critical components in any flyback is the transformer design. Since the operation mode is slightly different from any other isolated converter, the transformer acts as a storage device and is delivering power to the output when the main switch is off. The secondary winding is exposed to the magnetic field created by the primary winding, thus having increased AC conduction losses. This applies also to the primary winding being in the magnetic field of the secondary winding, also creating AC conduction losses. The AC losses increase is more significant in the quasi-resonant design.

Minimizing the leakage inductance is a must in any flyback transformer design. This can be achieved by proper winding interleaving. The leakage inductance creates a voltage spike on the main primary switch. This is often dampened by the use of RCD snubbers.

The primary switch exhibits both conduction loss and switching loss. By turning on the switch at the minimum valley voltage, the switching losses decrease. This is one of the main advantages of using a quasi-resonant flyback. The secondary rectifier exhibits conduction losses and reverse recovery losses, the latter being eliminated by operation in quasi-resonant mode. The output capacitor exhibits ESR conduction losses.

Figure 18.7 shows the switching waveforms for a Flyback converter used as an intermediate bus converter.

18.3.4 LLC Converter

Operation at higher switching frequencies reduces the size of passive components such as transformers and filters. Switching losses have been the main obstacle to achieve high frequency operation. Switching losses are directly proportional with switching frequency. Resonant converters have been in the power supply industry for more than 20 years. One of the most successful resonant topology which emerged is the LLC type. Its main advantages are that it obtains Zero Voltage Switching (ZVS) on the primary side switches and Zero Current Switching (ZCS) on the secondary side rectifiers [12]. The typical power levels for the LLC converter can be between 50 W and 1KW.

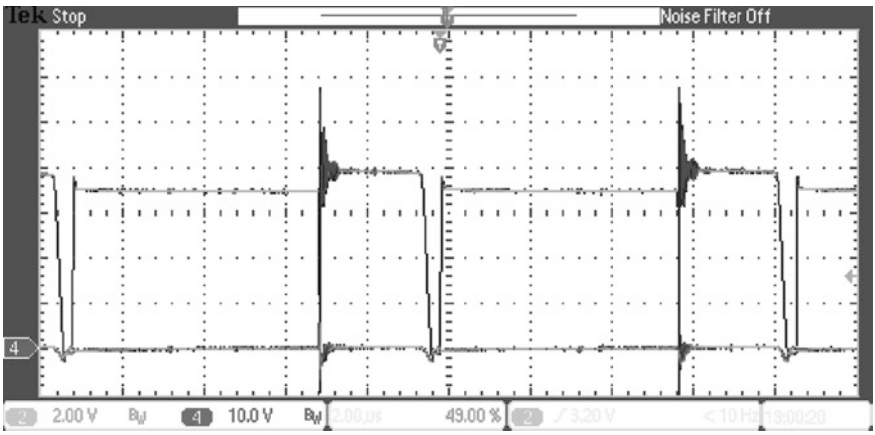


Fig. 18.7 ZVS switching waveforms for critical conduction flyback: CH_4 Mosfet drain, CH_2 Mosfet driving signal

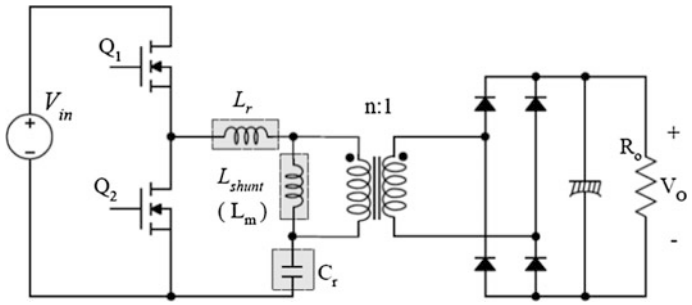


Fig. 18.8 Half-bridge LLC resonant converter

The power supply gain is controlled by changing the switching frequency. The LLC resonant converter contains a resonant network. This network is consisted, as the name implies from two inductors and a capacitor. Figure 18.8 defines a resonant inductor L_r and a shunt inductor L_m and also a resonant capacitance C_r.

The resonant inductor can be the leakage inductance of the transformer, or a discrete inductor, or both in series. The shunt inductor is the magnetizing inductance of the transformer. If the primary side of the converter is used in a half-bridge configuration, the resonant capacitor value is the sum of the two bridge capacitor values. The resonant tank contains two resonant frequencies:

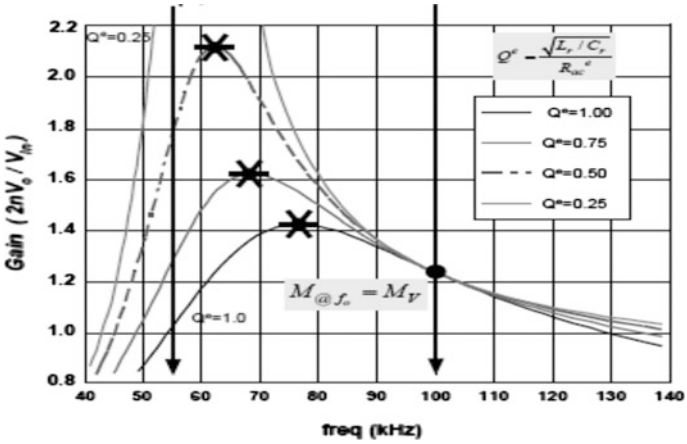


Fig. 18.9 Typical gain curves of LLC resonant converter

– a resonant frequency f_0, defined as:

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{18.15}$$

– a lower resonant frequency f_p, defined as:

$$f_p = \frac{1}{2\pi\sqrt{L_p C_r}}, \tag{18.16}$$

where L_p is the sum of the shunt inductor and the series inductor, and L_r is the resonant inductor. To maintain ZVS conditions the converter must be designed to operate with a switching frequency higher than fp, ideally f_p + (10–20%) margin.

A particularity of this converter is that by operating around the resonant frequency f0, the gain characteristic is almost independent of the load, as shown in Fig. 18.9 [12].

Analyzing Fig. 18.9, depending on the primary side we can identify conduction losses in switches Q1 and Q2, conduction losses in Lr winding, transformer windings and also in the ESR of the resonant capacitor. The secondary side rectifiers can be diodes or synchronous rectifiers. If operated above the resonant frequency fp, there are theoretically no switching losses, one of the main advantages of this topology. Contrary to other topologies, a larger leakage inductance value will not affect the performance since the leakage inductance value is absorbed in the series inductor.

This topology is a good candidate for an intermediate bus converter because of its load independent constant gain while operated at the resonant frequency f_0. The main drawback of this topology is that the RMS current values in both primary side

and secondary side are higher than typically operated PWM converters and also the peak values of the voltage and currents are higher, thus requiring higher component derating values.

18.3.5 Control Mechanisms of Power Converter Units

Controlling a power DC-DC converter unit is always dependent on the topology, transient needs and other factors required. Control mechanisms can be achieved via analog control, digital control or mixed analog-digital control [13, 14].

Traditionally, analog control was used to generate the drive signals, feedback loop and other auxiliary needs. Some of the main advantages of analog control were the low quiescent power and very fast feedback loops. The disadvantages are the high number of discrete components, higher susceptibility to electrically induced noise and few reconfiguration options. As things evolved, IC manufacturers built integrated analog controllers, which are very good tools in building power supplies. However, they offer little flexibility and their usage is standard.

As things evolved, digital control gained popularity, now being the most used control mechanisms. The advantages are numerous, while the disadvantages are low and decreasing. Advantages come from the fact that there is usually a user-programmable microprocessor core connected to numerous digital and analog peripherals, which offer large flexibility. Such peripherals include high-speed analog-to-digital converters, fast digital and analog comparators, high performance pulse width modulation (PWM) signal generators, which often allows dead time compensation and many other tweaks. Having all those peripherals backed by a microprocessor results in designing fast digital feedback loops, temperature and voltage protection, as well as powerful communication.

Some of the drawbacks of using a microcontroller are that depending on the need for computation power (i.e. how fast the feedback loop needs to be), the current consumption may be higher. Also, for multi-output power supplies, the microcontroller may not have sufficient computation power to drive multiple output, each with its own loop, if we're talking about voltage regulation, or loops if both the voltage and the current needs to be regulated.

Mixed analog and digital control usually incorporates both a user-programmable digital microprocessor and analog circuitry. The microprocessor usually handles communication, faults, temperature measurements, alarms and signal driving, while the analog circuitry provide a fast response feedback loop, with a reference set by the microprocessor. This allows for lower power consumption on the microprocessor (no need to process lot of signals) and very high transient performance of the power supply.

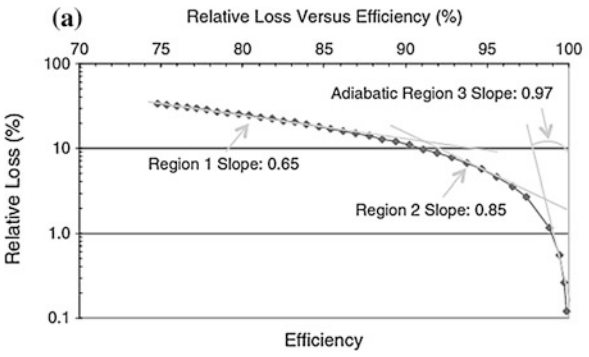
Feedback control mechanisms used vary from the simplest On/Off control, to PI and PID loops, N pole M zero controls, Sliding Mode Controllers and Fuzzy logic. Any of these can be implemented in a microcontroller, with standard C or Assembly programming, or mixed C-ASM. The reason for using mixed C-ASM

coding is: state machines, alarms and communication require usually more complex thinking but are not time critical. For this reason C code (which after compiling, the output is usually less efficient) is a perfect candidate, while feedback loops and cycle by cycle current limiting are written directly in Assembly because of the time constraint. Other advantages in doing this is the fact that though the microcontroller has enough processing power to allow the user to write C-code over the entire firmware, having efficient code allows the possibility of tuning the processor clock down and reduce overall power consumption.

18.4 Adiabatic Point of Load Modern Concept for Space Applications

In thermodynamics, the "adiabatic" term refers to a system that doesn't change (gain or loss) heat with the exterior surroundings. Starting from this definition, an adiabatic point of load technology refers to an ultrahigh efficiency that forces the power converter to virtually produce no heat when processing the power, which is essential in space applications where no atmosphere exists for heating dissipation [15]. Applied in the electrical power systems for the existing satellites whose end-to-end efficiency in payloads doesn't exceed today 65%, this new, modern and of ultrahigh efficiency technology promises to bring the advantages of no heat removal and constant temperature [16].

An illustrated explanation of this adiabatic technology concept is presented in Fig. 18.10a, where the adiabatic region has a slope of minimum 97% efficiency (ideally, at least 98.5%). It can be observed that both cost reduction and efficiency improvement are simultaneously achieved. With an efficiency improvement of only 1.3% the throughout power doubles, as is shown in Fig. 18.10b.



(b)

Efficiency (%)	Efficiency Delta (%) to Cut Loss by a Half
74.78	11.4
80.41	9.0
84.66	7.3
89.38	5.3
92.83	3.7
95.6	1.9
97.4	1.3
98.84	0.6
99.45	0.3

Fig. 18.10 POL with high efficiency intermediate bus converter **a** the definition of the adiabatic region; **b** example of reducing the power loss by a half

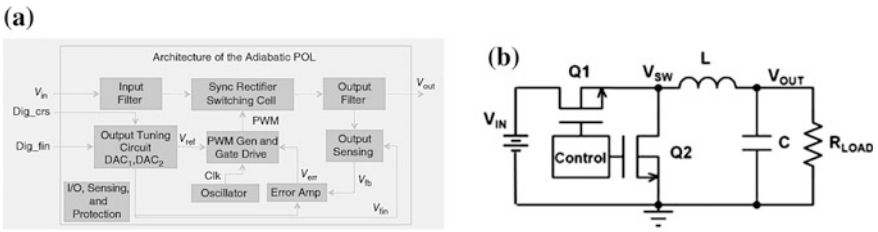


Fig. 18.11 **a** Block diagram of adiabatic POL design; **b** synchronous buck converter (synchronous rectifier)

In Fig. 18.11a the adiabatic POL design block diagram is presented and it can be observed that its overall architecture is similar with the Buck synchronous converter/rectifier, whose electrical diagram results from the basic Buck converter diagram from Fig. 18.11b if diode D1 is replaced with another switch similar to the switch S1, thus significantly reducing losses and optimizing the overall conversion efficiency [17].

Point of Load (POL) or Point of Use (POU) is emerging solutions for applications in which circuits require low voltages of 3.3 V and below. As it was shown above, the most popular POL topology is the Buck converter. Stepping down the voltage from the bus voltage of for example 48 to 1 V or lower will require a very low duty cycle, which will result low converter efficiency. For this reason, to obtain a good power system efficiency the POL must have in front of it an intermediate bus converter as Fig. 18.4c with a double regulated intermediate bus architecture shows. With this type of architecture both the bus converter and the POL converter can reach higher efficiencies and, with both tightly regulated, system's end-to-end efficiency and static and dynamic performances are improved to the level of the needed adiabatic region in Fig. 18.10a.

Typically, the bus voltage for space applications is 12 V. The Buck converter is the most basic SMPS circuit. It is also called a DC transformer without galvanic isolation since it's a non-isolated topology. The Buck topology has several modes of operation: continuous conduction mode, boundary conduction mode and discontinuous conduction mode. Depending on the load current and specific application, the converter can be designed to operate in one or more of these three modes. The Buck converter is widely used in Voltage Regulated Module (VRM) applications, where the output voltage is low and the load current is very high. This is similar the requirements of mission critical power levels. A good part of this proven technology can be borrowed from the VRM technology. For high current applications, the Buck POL will operate in continuous conduction mode and fixed frequency with variable duty cycle. For lower load current and higher voltage applications, the Buck POL will operate in discontinuous conduction mode with variable switching frequency and variable duty cycle.

Figure 18.11b shows synchronous Buck converter's components which are: switches Q1 and Q2 (in the VRM technology, Q2 is placed instead diode D2 of the

classical Buck converter in order to improve efficiency), output filter L and C and input resistance Rload. In the case of synchronized rectification, the main switch and the synchronous rectifier have a complementary drive signal, resulting in the fact that at low duty cycles (for switch Q1), the synchronous rectifier receives most of the load current. The implementation of a synchronous rectifier switch allows the converter to operate in discontinuous conduction mode with a negative rectifier current. This negative current allows the two switches to operate under zero voltage switching mode and eliminate the switching losses. This mode of operation has the drawback of introducing a large AC current ripple in the output inductor L which translates into AC winding inductor losses and increased inductor core loss. This is the reason that for high currents operation in discontinuous mode is less efficient.

Decreasing the size of the POL has been a challenge in the industry for many years, POL efficiency has always been the limiting factor for this. New advancements in semiconductor technologies such as the use of Gallium Nitride (GaN) devices allow the increase of the switching frequency and reduction of the magnetic component size [18, 19]. Low voltage GaN switching devices, which can be employed in the POL are compared by similar silicon device in Table 18.3. These two devices are typical devices specifically designed to be used in POL converters. The GaN switching devices have an advantage over similar silicon devices in terms of parasitic capacitances, which is significantly lower than silicon counterpart.

For the same Drain-to-Source maximum voltage the GaN exhibits a lower conduction resistance. It also exhibits a 40% lower gate charge, which decreases the driving losses. This advantage becomes more significant at a higher switching frequency. The GaN device output capacitance is almost half of the silicon counterpart, meaning that there will be efficiency advantages for the POL in both operating modes. Zero voltage switching is easier to obtain in discontinuous conduction mode because of the lower output capacitance requiring less negative circulating current. In continuous conduction mode the drain-to-source voltage spike on the switching device is lower.

Table 18.3 Silicon versus GaN

	Low voltage silicon BSN012N03LSI	Low voltage GaN EPC2023
V_{DS} (V)	30	30
$R_{DS(on)max}$ (mΩ)	1.6	1.3
I_D (A)	50	60
Size (mm)	3 × 3	6 × 2.3
Q_g (gate charge total) (nC)	37	20
C_{OSS} (output capacitance) (nF)	2.2	1.3
Q_{rr} (reverse recovery charge)	5 nC	0

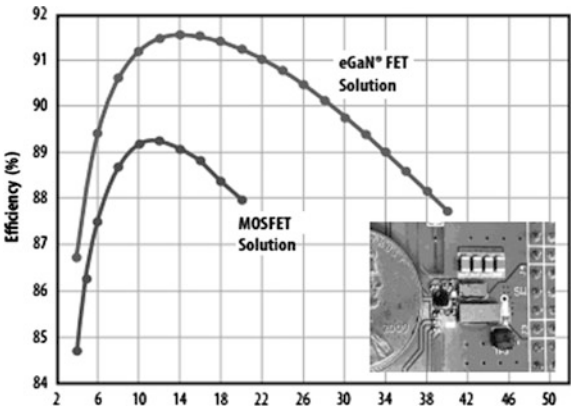


Fig. 18.12 GaN versus MOSFET POL efficiency for a V_{in} = 12 V, V_{out} = 1.2 V, f_{sw} = 1 MHz industrial example

Operation in continuous conduction mode has a fundamental problem in both cases using either rectifying diode or synchronous rectifier because of the reverse recovery losses. In each case this also creates voltage spikes on the switching devices. The main advantage of the GaN switching device is that it experiences zero reverse recovery charge, thus allowing POL operation for high currents at high switching frequencies. The voltage spike amplitude reduction due to the zero reverse recovery charge allows the usage of lower voltage switching devices, which have an inherent lower $R_{DS(ON)}$ and as a result increases efficiency. In Fig. 18.12 we can see power density and efficiency improvements by using GaN transistors instead of conventional silicon ones for a typical POL application running at the switching frequency of 1 MHz. Low voltage GaN devices are being priced at comparable level with the silicone ones which makes them to be taken into account for new designs [20, 21].

Briefly, the trend for POL converters is to decrease the size, increase the efficiency and increase the power density. The ultimate goal is that the converter not to require heat transfer to the surrounding environment. In order for the POL to run in an adiabatic environment, the power dissipation must be controlled, temperatures monitored at all times and considering no air flow, the only possible cooling is done via conduction and radiation.

18.5 Energy Management and Experimental Results

A power system configuration composed by an intermediate bus converter and one or more POL converters must have a governing "brain", which monitors the overall system by knowing exactly each blocks status. This governing function is performed by one or several controllers. In case of multiple controllers, they must be able to establish bidirectional communication between them.

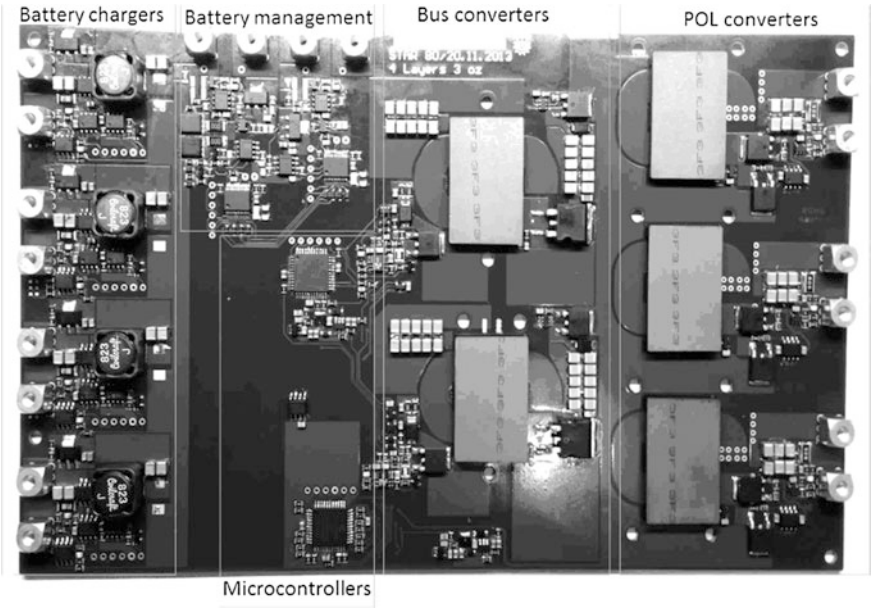


Fig. 18.13 Power management/distribution system for small satellites prototype

In this overall power arrangement there are two or more isolation areas. As already stated before, the intermediate bus converter provides the isolation boundary which is defined by a primary side and a secondary side. The POL is located in the secondary side isolation.

In Fig. 18.13a the power distribution/management system for very small satellites is presented. As also the picture shows, it is composed of four redundant battery charging units (BCU), two battery management units (BMU), two redundant intermediate bus converters, three POL converters and the management unit with two microcontrollers (the primary controller and the secondary controller). The system is designed to have four independent solar panels at its inputs and to supply three galvanic isolated output voltages of 5, 3.3 and 1.2 V. The total combined output power is designed to be 50 W. Also is has a 14.4 ÷ 16.8 V four cell LiIon battery pack connection, which is charged from the solar panels and also supplies the output power when the panels are in shade or malfunctioning. Figures 18.14 and 18.15 describe the software flowchart for the primary side and secondary side controllers. The two intermediate bus converters have two system controllers, one for the primary side and the other for the secondary side. The secondary side controller is also responsible for regulating the voltages on the POL stages. The chosen topology for the intermediate bus converter shown here is the Flyback topology. The Flyback is chosen because of its ability to have a large input voltage range needed for our application and because it has no need for an output inductor and thus saving space on the PCB. The transformers are implemented using planar

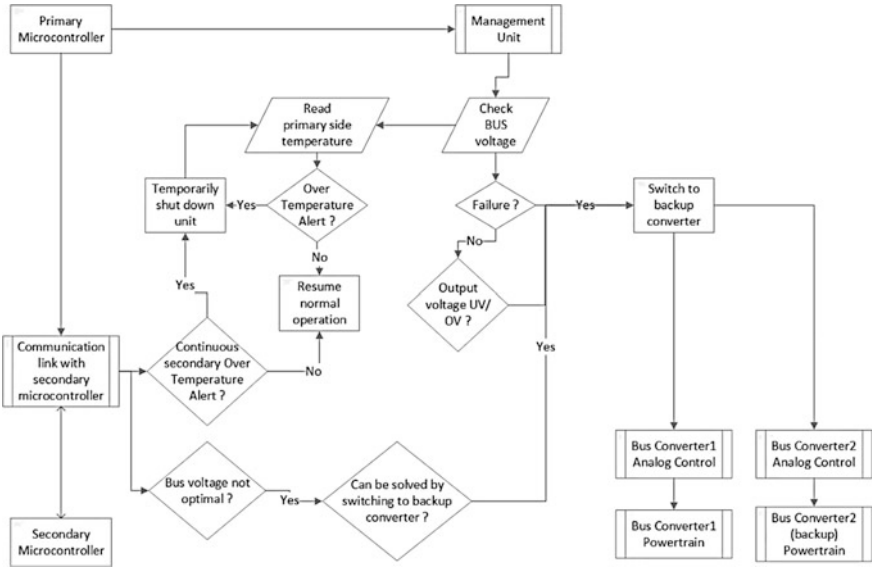


Fig. 18.14 Primary side controller software chart

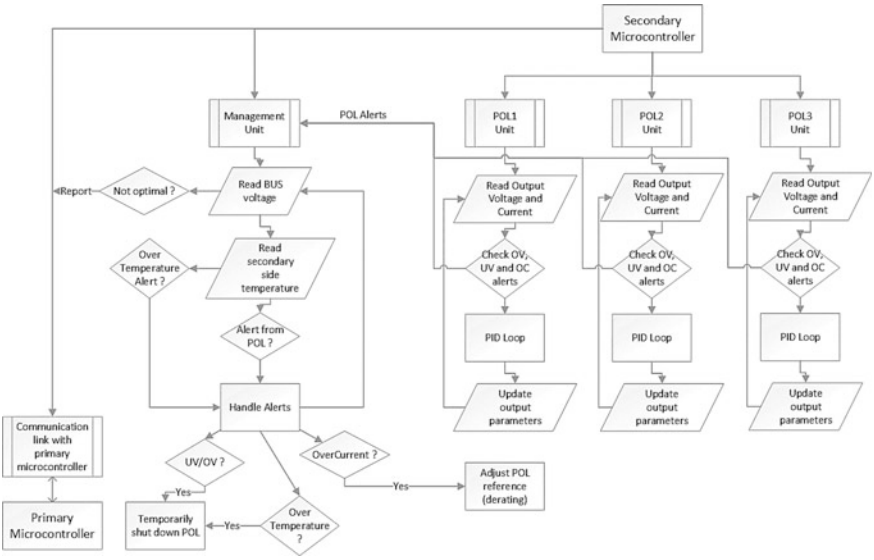


Fig. 18.15 Secondary side controller software chart

magnetic technology, which is more common in military applications and server applications. This was chosen because of inherent cooling capabilities, and better mechanical rigidity, especially in the cases of transportation vibrations. There are two intermediate bus converters for redundancy purposes. Each one has its own analog controller which drives and regulates the output bus voltage. As can be seen in Fig. 18.14, these analog controllers can be turned on and off by the primary system controller. In the same time, this controller can assume the drive and regulation functions, fully replacing the analog control by digital control.

At the end of each Flyback converter there is a protection stage called an ORING stage. This ORING stage technology is borrowed from telecom industry, where multiple DC-DC converters are paralleled into a single bus. The classical approach is for each converter to have an ORING diode. The main drawback of this represents the high power dissipation on the diode. In the latest power systems, this diode has been replaced with a high-side MOSFET switch with low $R_{DS(ON)}$. This switch is controlled by an analog ORING controller, which monitors the switch current and disables the switch if the current becomes negative. A negative current in the switch indicates a converter fault which creates a short circuit path to ground. The basic function of the ORING controller is to disconnect this current path to ground, thus disconnecting and isolating the faulty stage from the bus.

The primary controller also has a temperature monitoring array of sensors for both Flyback intermediate bus converters. Any detection of an abnormal temperature will trigger an internal fault state which decides whether to completely shut down the stage or run it in a power derating mode. The primary controller performs an under voltage and over voltage lockout function in case the bus converter input voltage is outside the accepted specifications.

The primary controller communicates with the secondary controller via a bi-directional digital isolator. Since optoelectronic components are not accepted for mission-critical space applications due to their sensitivity to radiation and fast aging, the chosen isolator with magnetic transformers.

The POL stages, have a regulated input bus voltage of 12 V and output voltages of 5, 3 and 1.8 V. They are digitally controlled and regulated by the secondary side controller. The output current for the 5 V POL is 6 A, for the 3.3 V POL is 9 A and for the 1.8 V output is 10 A.

As depicted in Fig. 18.15, the secondary controller independently reads the output power for each POL and monitors the bus voltage. It also has a temperature monitoring function, buy monitoring the temperature of each POL. The secondary controller can receive fault signals from the primary controller and can control the ORING stages. In the case of an intermediate bus converter fault, the primary controller sends information to the secondary sides which must react and disconnect the faulty stage. This is a redundant protection in case the ORING controller fails to turn off the output switch.

The primary controller can also send to the secondary controller a temperature warning information in the case the intermediate bus converters are getting close to the maximum temperature limit, such as the secondary controller will prepare to go into a power derating mode for the POL loads which allow it. If the POL load does

not allow power derating mode, then the secondary controller will completely shut down the entire POL stage. The secondary controller can send information to the primary side regarding the bus voltage. If the bus voltage is out of the required specification, the secondary controller will send a shutdown command to the primary controller.

One of the most innovative features of the whole system is that the regulated intermediate bus voltage can be adjusted to make the POL converters operating under the most efficient conditions and/or make the Flyback intermediate bus converter run more efficiently. In the scenario of a high load situation for the POLs, with one of the POL stage goes close to the critical operation temperature, and the Flyback stage is in normal operating temperature, the secondary controller will ask the primary controller for a lower bus voltage, decreasing the POL power losses and decreasing the POL temperature. This works both ways, in the case that if the Flyback reaches the critical operating temperature while the POL is in the nominal operating temperature, the primary controller inquires the secondary controller for POL temperature values. If the POL temperatures are in the nominal regions, the primary controller decides to increase the bus voltage, which reduces the Flyback output current, increases its efficiency and inherently lowers the Flyback temperature.

Figure 18.16 shows the intermediate bus converter efficiency curve versus different loading conditions.

The flyback intermediate bus converter operates in critical conduction mode using primary winding feedback. The control method is current mode control. Because of this mode of operation, voltage switching for the main primary side switch can be obtained.

Figure 18.17 shows the efficiency graph of the POL 5 V Vout converter. The three POL converters have the same hardware components, the output voltage is set by the secondary side digital controller. Figure 18.18 shows the efficiency graph of the POL 1V2 Vout converter. Figure 18.19 shows the efficiency graph of the POL 1V2 Vout converter. All three POL's operate in continuous conduction mode with the switching frequency of 250 kHz. The output filter is composed of a planar inductor E32/6/20 core 3F3 material with 1 turn parallelized on 4 layers and six ceramic capacitors 1210 size 22 uF/25 V.

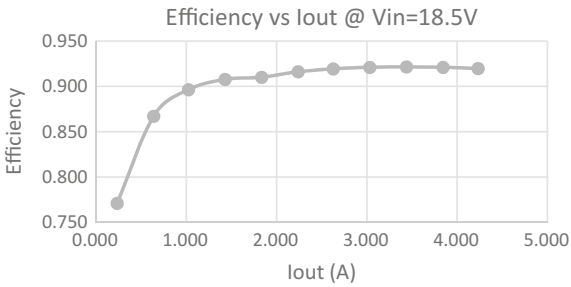


Fig. 18.16 Efficiency graph for intermediate bus converter

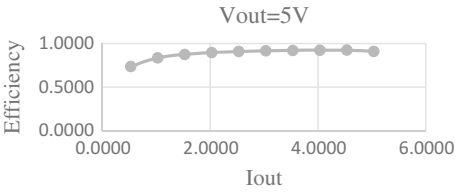


Fig. 18.17 Efficiency graph 5 V POL

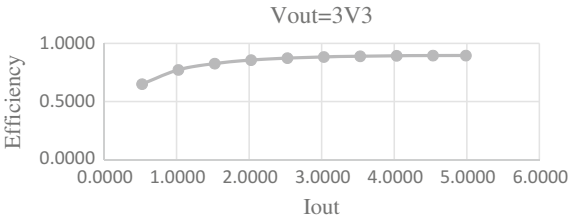


Fig. 18.18 Efficiency graph 3V3 POL

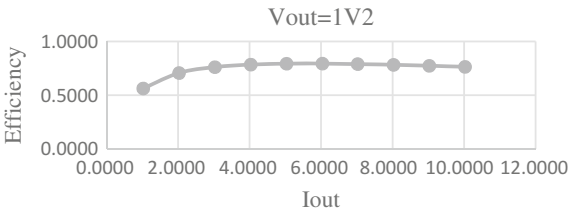


Fig. 18.19 Efficiency graph 1V2 POL

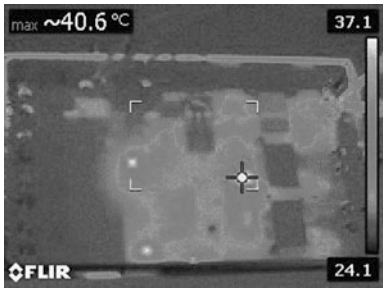


Fig. 18.20 Thermal pictures of the unit

Figure 18.20 shows the thermal imaging of the unit at full load operating conditions. With an ambient temperature of 24° the unit maximum temperature is 40.6° at full load condition. The temperature rise is 16°. The unit is clamped in aluminum housing with gap pad thermal conductive material. The aluminum case extracts heat from the unit in a very efficient way. The components on the PCB are rated to 125 °C and the PCB itself is rated to 150 °C and as a result is way below the maximum temperature of the unit.

Fig. 18.21 Power module testing conditions

Figure 18.21 shows the power module testing conditions. The solar panel and the LiIon battery can be observed. In order to simulate the solar panel in different sunlight conditions a solar array simulator was used.

18.6 Conclusions

Different requirements from conventional power conversion are imposed due to the critical nature of space applications. Any failure will likely trigger a chain of events which may lead to cancelling the mission. Component size restrictions are different from conventional power systems, which, in order to achieve lower end price and higher efficiency, use smaller and more high density and novel parts, which are usually smaller, like smaller resistors and capacitors and ball grid array (BGA) footprints. Especially in space power systems, components have a larger footprint in order to withstand the vibration stress.

In most mission-critical applications there is limited cooling available due to the fact of operation in extreme environments such as the vacuum of space, high altitude, lower or higher pressure and lower or higher temperatures. In such cases, efficiency of the power system is a key parameter in the design. The packaging of the converter is a challenge to design because in the operation in harsh environments the power system needs to be protected from outside elements, but also its inputs and outputs need to be protected with rated connectors. To improve packaging, planar magnetics are the future trend as a replacement for conventional magnetics. The advantages include lower profile, improved cooling, reduced parasitic elements and high repeatability in production. System miniaturization is possible by the use of the planar magnetics and digital control. This feature is very important for power management units designed especially for very small satellites.

The most proven power stage topologies can be imported from conventional power systems. Also the control schemes can be imported from conventional power systems, with an emphasis on parameters monitoring and redundancy. In order to improve converter efficiency new GaN devices can be employed. Intelligent power processing such as intelligent voltage buses help increase the overall power system

efficiency, thus creating much smaller and lighter designs for the electrical power system of the very small satellites.

Acknowledgements This work was supported by a grant of the Romanian National Authority for Scientific Research, Program for research Space Technology and Advanced Research—STAR, project number 80/29.11.2013.

References

1. . http://www.esa.int/Our_Activities/Space_Engineering_Technology/Power_Laboratories
2. Bussarakons T. Thick film hybrid DC-DC converters are standard 'Brick' for satellite power systems. Int Rectifier. http://www.irf.com/product-info/hi-rel/tp-hybridbrick.pdf
3. Dowell PL (2010) Effects of eddy currents in transformer windings. In: IEEE IET proceedings of the institution of electrical engineers, January 2010, vol 113, no 8, pp 1387–1394. ISSN 0020-3270, doi:10.1049/piee.1966.0236
4. Margueron X, Besri A, Lembeye Y, Keradec JP (2010) Current sharing between parallel turns of a planar transformer: prediction and improvement using a circuit simulation software. IEEE Trans Ind Appl 46(3):1064–1071. doi:10.1109/TIA.2010.2046294 0093-9994
5. Prieto R, Garcia O, Cobos JA, Uceda J (2002) Designing inductors at device and converter level. In: IEEE proceedings of the 2002 international symposium on industrial electronics (ISIE 2002), vol 3, pp 987–993. Print ISBN: 0-7803-7369-3, doi:10.1109/ISIE.2002.1025868
6. Xu H, Ngo KDT, Bloom G (1995) Design techniques for planar windings with low resistances. In: IEEE tenth annual proceedings of applied power electronics conference and exposition (APEC 1995), March 1995, vol 2, part 2, pp 533–539. Print ISBN: 0-7803-2482-X, doi:10.1109/APEC.1995.469073
7. Ouyang Z, Thomsen C, Andersen MAE (2012) Optimal design and tradeoffs analysis if planar transformer in high power DC-DC converters. IEEE Trans Ind Electron 59(7):2800–2810. doi:10.1109/TIE.2010.2046005 0278-0046
8. Acero J, Carretero C, Millan I, Lucia O, Alonsoa R, Burdio JM (2011) Analysis and modeling of planar concentric windings forming adaptable-diameter burners for induction heating appliances. In: IEEE transactions on power electronics, May 2011, vol 26, no 5, pp 1546–1558. ISSN: 0885-8993, doi:10.1109/TPEL.2010.2085453
9. Tan D (2014) A review of intermediate bus architecture: a system perspective. IEEE J Emerg Sel Top Power Electron 2(3):363–372. doi:10.1109/JESTPE.2014.2303154 ISSN: 2168-6777
10. Sutto T (2010) 2 switch forward current mode converter. ON semiconductor application note AND8373D. http://www.onsemi.com/pub_link/Collateral/AND8373-D.PDF
11. Saliva AA (2013) Design guide for QR flyback converter. Infineon Technologies North America (INFA) Corporation, January 2013. http://www.mouser.com/pdfdocs/2-9.pdf
12. Fairchild Application Note AN4151 (2014) Half bridge LLC resonant converter design using FSFR-series fairchild power switch (PFS). https://www.fairchildsemi.com/application-notes/AN/AN-4151.pdf
13. Erickson RW, Maksimovic D (2001) Fundamentals of power electronics, 2nd edn. Springer, New York. ISBN -13: 978-1475705591
14. Mohan N, Undeland TM, Robbins WP (2003) Power electronics: converters, applications, and design, 3rd edn. Wiley, USA. ISBN -13: 978-0471226932
15. Tan D (2015) Emerging system applications and technological trends in power electronics. IEEE Power Electron Mag 2(2):38–47
16. Tan D (2015) Power-conversion technology is going adiabatic: adiabatic point-of-load technology for space applications. IEEE Power Electron Mag 2(4):47–53

17. Rashid MH (2014) Power electronics: circuits, devices and applications, 4th edn. Prentice Hall, USA. ISBN -13: 978-0133125900
18. Lidow A, Strydom J, Rooij M, Reusch D (2014) GaN transistors for efficient power conversion, 2nd edn. Wiley, USA. ISBN 978-1-118-84476-2
19. Reusch D, Glaser J (2015) DC-DC conversion handbook: a supplement to GaN transistors for efficient power conversion. Power Conversion Publication. ISBN-10: 0996649204
20. http://epcco.com/epc/Portals/0/epc/documents/briefs/AB006%20eGaN%20FETs%20for%20POL.pdf
21. http://epc-co.com/epc/Applications/DC-DCConversion/PointofLoadConverters.aspx