Chapter 7
Grid Integration Techniques in Renewable Energy Systems

Learning Objectives
On completion of this chapter, the reader will have knowledge on

- Grid Issues in integrating renewable energy systems.
- Converters used for grid integration techniques and its control strategy.
- MATLAB/SIMULINK models of Synchronous Reference Frame PLL (dq PLL), Stationary Reference Frame PLL (αβ PLL), Decoupled Synchronous Reference Frame PLL (DSRF PLL), Decoupled Stationary Reference frame PLL (Dαβ PLL) and Hybrid Dαβ PLL.
- Filters used for grid integration techniques and its control strategy.

7.1 Introduction

Depending on the scale of generation, the renewable energy can be integrated into the utility grid either at the transmission level or at the distribution level. Wind farms which are a part of large renewable energy generation can be directly interconnected to the transmission system whereas the small scale distributed generation is generally interconnected to the medium or low voltage distribution systems. Before designing the system for both the types of interconnections a detailed analysis have to be made to face the different challenges in it. The most common issues encountered during the grid integration of different types of renewable energy systems are outlined and discussed in this chapter. The different problems and solutions are highlighted in this chapter through detailed simulations and case studies.

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7.1.1 Integration of Small Scale Generation into Distribution Grids

Electricity generation using various renewable energy resources like small hydro, solar photovoltaic, biogas, biomass and small wind turbine based electricity generation are often taking place in small scale due to disperse nature of the resources and the generation varies between a few hundreds of kilowatts to several megawatts. Distributed generation (DG) or distributed resources (DR) are the one where these small scale electricity generators are generally connected to the grid either at the primary or secondary distribution level. Distributed resources include both renewable and non-renewable small scale generation as well as energy storage.

7.1.2 Different Types of Grid Interfaces

The energy generated through small renewable energy generators cannot be directly connected to grid. Some kind of interface is required between the generation and utility distribution grid. For example, power electronics based dc -to –ac converter is required between the grid and the solar photovoltaic's (PV) panel generator. Though the direct connection to the ac grid is possible through induction generator based small hydro or wind a power electronic converter is used to avoid concerns regarding starting transients, energy conversion efficiency and power quality. The common types of energy generation and their preferred interfacing technologies are summarized in Table 7.1.

7.1.3 Issues Related to Grid Integration of Small Scale Generation

Conventional electric distribution system has a single voltage source on each distribution feeder. But this is not the case when small scale renewable energy generations are interconnected to the distribution grid. Hence in order to ensure safe and reliable operation of the grid certain special requirements are to be satisfied during interconnection. Major protection related problems are fault clearance, reclosing and inadvertent islanded operation. In many cases, the grid –DG interface

Table 7.1 Interfacing technologies

Type	Interfacing technology
Fuel cells	Power electronic converter
Wind	Induction generator/power electronic converter
Photovoltaics	Power electronic converter
Small hydro	Synchronous or induction generator, power electronic converter

is based on power electronics inverters or asynchronous generators. The utilities are concerned about their impact on power quality and the impact includes harmonics, voltage dips, over voltages, and voltage flicker. Several studies in literature have identified that the technical requirements imposed by utilities to address these concerns as a major technical barrier for grid integration of DG. The general technical requirements for interconnection of small scale generation uses IEEE P1547 standards as guideline.

7.1.3.1 Protection Issues

The most serious issue related to the interconnection of distributed generation is Protection. Usually radial type distribution network configuration is used with time graded over current protection scheme. When a DG is interconnected it may alter the coordination of the existing protection scheme and can lead to malfunction of the protection equipment. The protection issues related to the interconnection of DG are briefly discussed below.

(a) Change of Short Circuit Levels

The main parameter used in the selection of fuses, reclosers. circuit breakers and currents transformers, and the coordination between over current relays are based on Short circuit level. The equivalent system fault point impedance and the expected fault current level are decided by the short circuit level. Rotating machine characteristics around the surroundings also decides the time variation in the fault current. Initially most distribution systems are designed as passive networks but the interconnection of DG made the equivalent network impedance to decrease which results in increase in the fault level. Therefore if fault occurs the existing circuit breakers may not withstand to the sudden high fault currents which also lead to CT saturation. Also the changed fault levels may upset the synchronisation among the over current relays which leads to unacceptable protection system operation. To explain the problem, consider the distribution system in Fig. 7.1. During the absence of DG the fault currents seen by the feeder breaker BK ($\mathbf{I_s}$) and the recloser RC ($\mathbf{I_r}$) are approximately equal to the fault current $\mathbf{I_f}$ ($I_s = I_r = I_f$). But when the DG is connected, $I_r = I_s + I_{dg}$ and $I_r > I_s$. This condition is not normally observed in passive radial network. This is not a concern if the interrupting capacity of the recloser is sufficient to handle the increased fault current. But, it is likely that coordination between the recloser and any downstream fuses is lost. During higher fault currents the recloser and fuses operate faster which makes the coordination to lose, due to reduction in the required margin between the recloser fast curve and the fuse melting curve.

(b) Reverse Power Flow

The power flows are unidirectional in radial distribution systems. Initially depending upon the power flow the protection schemes are designed. When a DG is connected, the coordination among the protection relays may get altered due to reversal in power.

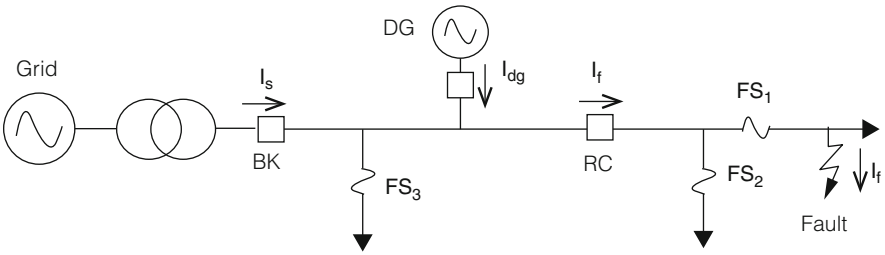

Fig. 7.1 Change of fault currents due to DG interconnection

(c) Lack of Sustained Fault Current

If fault occurs the protection relays may detect and discriminate the fault currents only if the measured fault current by the relays is significantly high when compared to the normal load current. When the DG fault current contribution is limited, the effective detection of faults by over current based protection relays is difficult. Normally, induction generators, small synchronous generators or power electronic converters are employed in renewable based energy generation. Supply of continual fault currents to three phase faults is not possible by the induction generators and fault current contribution to the asymmetrical faults is also limited. In small synchronous generators sustained fault current supply which is significantly higher than the rated current is not possible. Power electronic converters are designed to limit the output current internally since the power semiconductor devices cannot resist the significant over current for long period. The ability of the relays to detect faults is compromised by the lack of sustained fault.

(d) Islanding

When a part of utility network is disconnected from the main grid and if the network is operated as an independent system supplied with one or more generators then it is called Islanding. Islanding may leads to abnormal voltage and frequency variations. During a fault, if an auto recloser is opened then two independent systems are formed which are operated at two different frequencies. Disastrous results may occur when the auto recloser is made to reclose during out of phase of two systems. In addition to that the islanding operation may create an ungrounded system which depends on the transformer connection. An unidentified island would be hazardous for the repair crews. Owing to aforesaid reasons, islanding is accepted as unsafe situation and upon formation of an island immediate disconnection of DGs from the grid is recommended.

7.1.3.2 Voltage Control

In low load or high (DG) production conditions, interconnection of DG results in over voltages and results in changes in power flows and the voltage profile of the

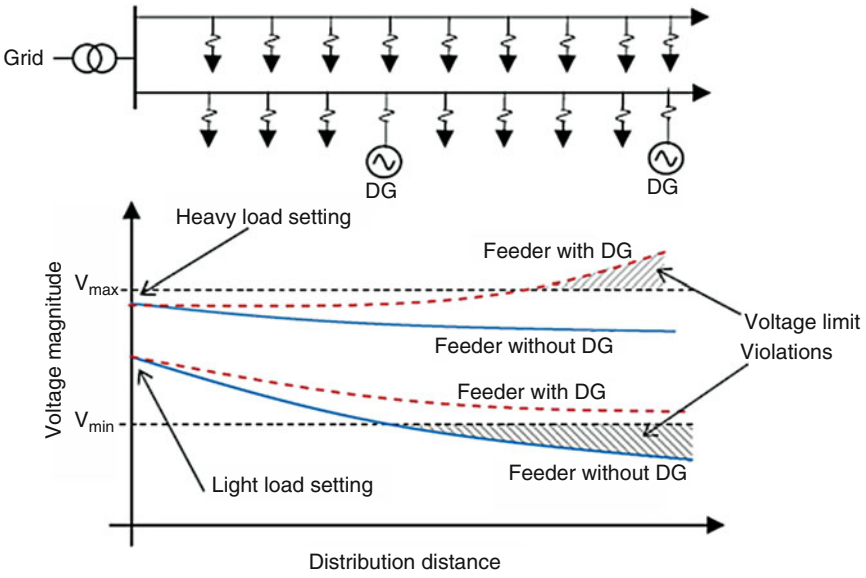

Fig. 7.2 Possible DG interconnection configurations

feeder. The voltage limit usually determines the DG capacity in weak networks and in addition to that the utility does not control the connection status of DG. Over voltages or under voltages may occur during the reconnection of DG under low load conditions or while during the disconnection of a DG during high load conditions. This may results in the operation of over/under voltage relays due to poor power quality situation. The increased penetration of DG made the selection of appropriate tap settings for the distribution transformer becomes difficult. The situation becomes more difficult when the DGs are not equally distributed among the feeders supplied by the same transformer. Figure 7.2 explains the concentration of DG on only one out of two feeders which are being supplied by a same transformer. Usually, the connection of DGs provides power to the nearby loads which results in reduction of net current flow through the transformer. Accordingly the transformer tap needs to be changed to the light load settings. As shown in Fig. 7.2 the decline in sending end voltage can cause a voltage violation at the far end of the feeder without DGs. Leaving the transformer tap at the heavy load setting risks over voltages on the feeder with DGs. The feeder voltages can be controlled by using switched capacitors and static VAr compensators, but it is too expensive. Unbalanced voltage profile also affects the operation of DGs at distribution level. As shown in Fig. 7.3, both the loads as well as DGs can be either three phase or single-phase. There will be an increase in system unbalance due to the interconnection of single phase sources. In addition to that, unbalanced distribution systems can pose problems for the three-phase DGs which are connected to it: causes overheating and frequent shutdowns due to unbalance currents in DGs.

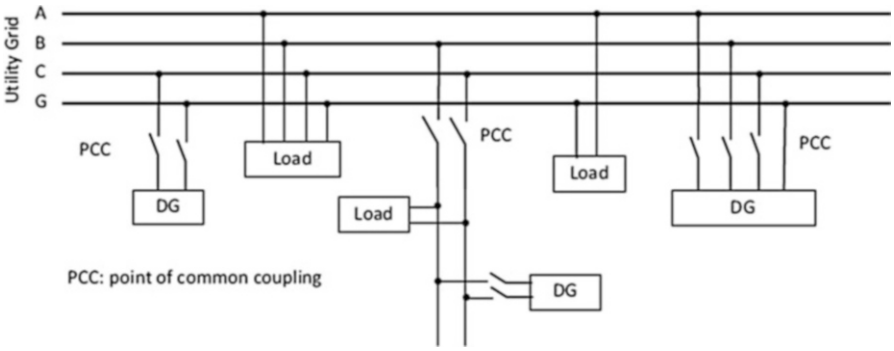

Fig. 7.3 Possible DG interconnection configurations

7.1.3.3 Harmonics and Flicker

One of the major concerns of service providers is to supply quality power to customers. Power electronic converters are used to interface most of the DGs, but this will injects harmonics into the system which results in poor power quality for the consumers. Harmonic filters can be used to overcome this. Based on the requirement hybrid filters can be selected appropriately and filters can be active, passive or hybrid. In addition to that voltage flickers may occur when connected induction generators are directly started. These voltage fluctuations can be reduced by some soft-starting mechanisms. Tower shadow effect may generate periodic voltage fluctuations in wind generators.

7.1.3.4 Interconnection Standards and Examples of Grid Codes

DG interconnection standards and guidelines have been introduced to address protection and safety issues. IEEE Std. 1547–2003, "IEEE Standards for Interconnecting Distributed Recourses (DR) with Electric Power Systems 2003" is the most commonly applied standard. Most utilities have accepted IEEE Std. 1547–2003 standard as a guideline/rule for interconnecting DG to their networks. The salient feature of IEEE Std. 1547–2003 is described below. Due to faults and other disturbances, when the voltage and/or frequency at the point of interconnection is deviated from their base values then the IEEE Std. 1547–2003 recommends to disconnect the distributed energy resources. Tables 7.2 and 7.3 define the allowable deviations. In Table 7.2, base voltages are the nominal system voltages stated in ANSI C84.1-1995. bDR 5 30 kW, maximum clearing times; In Table 7.3, if $DR \leq 30$ kW, maximum clearing times occur, and if $DR > 30$ kW, default clearing times occur.

Also, for an unintentional island where a DG energizes a portion of the network, within 2 s of the formation of island the DG interconnection system must detect the island and should disconnect the DG.

Table 7.2 Interconnection system response to abnormal voltages

Voltage range (% of base voltage)	Clearing time
$V < 50\ \%$	0.16
$50\ \% \leq V < 88\ \%$	2.00
$110\ \% \leq V < 120\ \%$	1.00
$V \geq 120\ \%$	0.16

Table 7.3 Interconnection system response to abnormal frequencies

DR size	Frequency range (Hz)	Clearing time
≤ 30 kW	>60.5	0.16
	<59.3	0.16
>30 kW	>60.5	0.16
	<{59.8–57.0} (adjustable set point)	0.16–300 (adjustable)
	<57.0	0.16

7.1.4 Integration of Large Scale Renewable Energy Generation

Based on synchronous generators conventional large scale renewable energy generations like hydro, steam turbines operated with biomass or geothermal energy uses conventional technologies. The utilities are very familiar with this conventional technology. But large scale wind farm integration poses completely different set of challenges, mainly due to interest of variable speed of generators and irregular nature of wind.

7.1.4.1 Issues Related to Grid Integration of Large Wind Farms

Current growths of wind energy generation have results in the development of large wind farms with more than 100 MW capacities and are usually interconnected to the transmission grid. The installed wind generation capacity has reached several thousand megawatts in few countries like Germany and Spain and is still increasing. But, the wind generators cannot dispatch the output power. Though there are many advances in short-term (and long-term) wind forecasting technology, accurate forecast of wind speed is still difficult. Hence, to cover the fluctuations in wind farm production a significant amount of spinning reserve and stand by capacity is required. Even though, there exist some moderating effect in wide geographic area distribution of wind forms, the chance of simultaneous low energy generation from all wind farms cannot be completely neglected. Short circuit in high voltage transmission network causes short duration voltage dip which results in disconnection of several thousand megawatts of wind generation from the grid and leads to severe stability problems within the power system. So, many system operators introduce new connection requirements for large wind farms. New connection

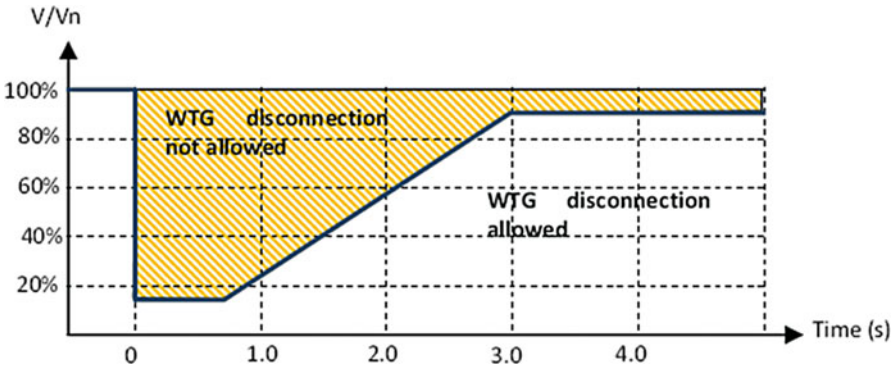

Fig. 7.4 Typical fault ride through requirements. The actual fault ride through curve can vary depending on the transmission operator

regulations like fault ride through capabilities force wind turbine to have a supporting effect on grid operations. Figure 7.4 shows the expected requirement of fault ride through capability in large, modern wind farms. The figure describes different levels of voltage depressions in wind farm and its connection time duration. This is a try to guarantee that the system will maintain stability after the clearance of fault and the wind farm is capable and ready to supply power immediately.

Serious challenges faced by the wind turbine system designer through 'strict' fault ride through standards are presented.

- The power transfer capability of the wind turbine generator (WTG) is reduced during fault. This will results in mechanical stress on blades and other rotating parts due to over speeding.
- The WTG may draw increased amount of reactive power from the system during fault and it depends on the employed generator technology which results in a poor fault recovery response.
- WTG technology decides the nature and the magnitude of the fault current. A good knowledge in this helps in designing equipment ratings for protection and control settings.
- The input mechanical power has to be regulated by the pitch control of turbine blades. During faults, the mechanical over speeding of rotating elements can be limited by the fast pitch control of blades.
- The overall performance of the wind farm can be improved by applying the appropriate FACTS based reactive power compensation device. One of the key issues related to wind power generation is the requirement of reactive power for voltage support. Induction generators are mostly used in wind generation systems. Induction machines do not have reactive power supply capability as synchronous machines. As per interconnection regulation the wind farms have to maintain the power factor within ± 0.95. Dynamic reactive supports like combination of capacitor bank and static var compensators (SVCs)/STATCOM are provided if the wind generators are not capable of meeting the aforesaid

requirements. The major protection problems related to the large wind farms is the over voltage due to the disconnection of the wind turbine generators while the capacitor bank is still connected. The performance of the wind farm immediately after the clearance of a system fault depends on the type of reactive power compensation method and devices. 'Available' terminal voltage of a capacitor banks (and SVCs) is decided by the reactive power capability. Owing to this reason, during fault recovery capacitor banks have a degraded reactive power capability which is also most needed. According to reactive power capability point of view FACTS based voltage source converters (e.g. STATCOM) are generally superior option and does not have this inherent drawback. Careful evaluation has to be done while selecting the reactive power compensation and its control strategy. Large wind farms can also use synchronous condensers as reactive power compensator they also provide inertia to the system but it has slower response when compared to STATCOM. This may be advantageous particularly when a weak ac system with dynamic stability concerns is interconnected. Detailed investigation which may be required on other possible challenges are as follows:

- Optimization of turbine power electronic design and controller.
- Protection and filter system design.
- Numerous turbine interaction.
- Wind farm issues which are connected into series compensated systems.
- Voltage flickers and other power quality problems.
- Wind farms starting and synchronization to the grid.
- Interaction of the electric network and the complex shaft/gear system of wind turbine leads to sub synchronous resonance problems.

To identify possible interconnection problems and its optimal solution, a detailed study on electromagnetic based transient program is essential.

7.2 MATLAB Model of Grid Integration

Solar grid-tie inverters are designed to quickly disconnect from the grid if the utility grid goes down. This is an NEC requirement that ensures that in the event of a blackout, the grid tie inverter will shut down to prevent the energy it produces from harming any line workers who are sent to fix the power grid. This section focuses on a MATLAB/SIMULINK model of a solar PV grid connected system. This model is developed to obtain solar panel output power and present it to an utility grid through a boost converter and an inverter. The boost converter is to step up the voltage obtained from the solar panel and the inverter is to convert the DC into AC. This section discusses the solar panel module, boost converter design and also design of the inverter. The solar PV grid connected system was tested using MATLAB/SIMULINK and the results are shown. During grid connection harmonic reduction, power factor corrections are taken into account.

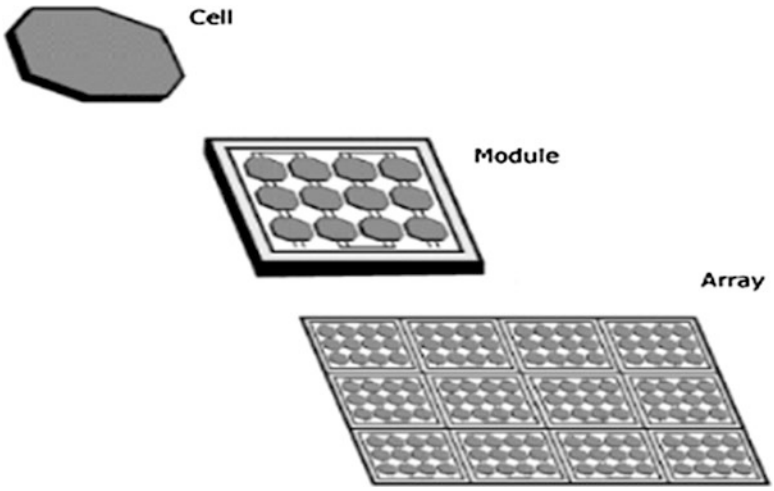

Fig. 7.5 Photovoltaic system

7.2.1 Photovoltaic Module

To produce the desired output, several low voltage PV cells (around 0.5 V) are connected in series (for high voltage) and in parallel (for high current) to form a PV module. A typical photovoltaic system is shown in Fig. 7.5. During partial or total shading, and at night, separate diodes may be needed to avoid reverse currents. These are not necessary for mono-crystalline silicon cells as they have sufficient reverse current characteristics. Reverse current can also leads to waste of power and overheating of shaded cells. At higher temperatures solar cells become less efficient and installers may provide good air circulation behind solar panels. Since a single module is not sufficient to produce the required power for home and business, Inverters are mostly used with PV arrays to convert the DC power into alternating current which can power motors, loads, lights etc. To produce desired voltage and current the modules in a PV array are first connected in series and then the individual modules in parallel. The MATLAB/SIMULINK model of a solar PV array is available in Sect. 2.4.1 of Chap. 2.

7.2.2 Boost Converter

DC-to-DC power converter whose output voltage is greater than its input voltage is known as step-up converter or boost converter. Boost converter shown in Fig. 7.6 is a type of SMPS (Switched Mode Power Supply) which consists of at least two semiconductor switches (a diode and a transistor) and one energy storage element like a capacitor, inductor or the combination of two. To reduce the output voltage

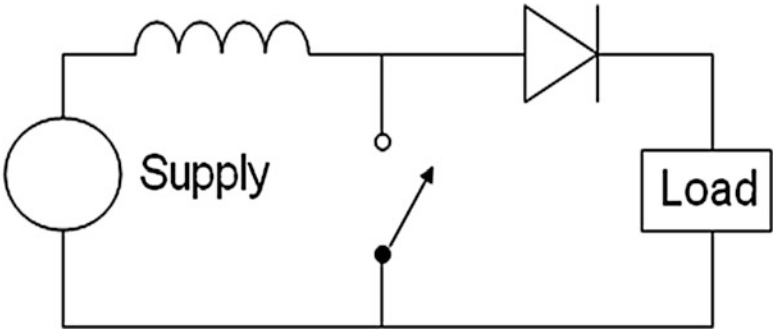

Fig. 7.6 Boost converter

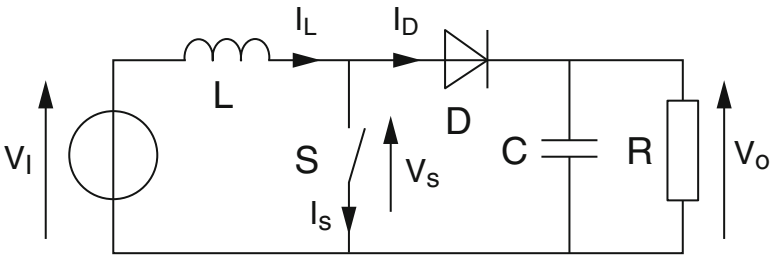

Fig. 7.7 Boost converter schematic

ripple a capacitor filter (sometimes in combination with inductor) is added at the output of converter.

DC sources like batteries, solar panels, rectifiers or DC generators can be used to power the boost converter. DC to DC conversion is the process of changing one voltage to other voltage. A converter with an output DC voltage greater than source DC voltage is known as boost converter or step-up converter. Since power must be conserved, the output current is lower than the source current.

The tendency of an inductor to resist changes in current is the key driving principle of the boost converter. The output voltage is higher than the input voltage in boost converter. Figure 7.7 shows the schematic boost power stage.

(a) Current flows through the inductor in clockwise direction and inductor stores energy when the switch is closed. Inductor left side polarity is positive.
(b) Impedance is higher and so the current is reduced when the switch is opened. Hence the inductor opposes the change or reduction in current. Now the left side of the inductor is negative and thus the polarity is reversed. The diode D made the capacitor to charge to higher voltage as a result of two sources in series.

The inductor will not discharge fully in between charging stages if the switching cycle is fast. Only when the switch is opened the load will always see a voltage greater than that of the input source. The capacitor parallel with the load is charged

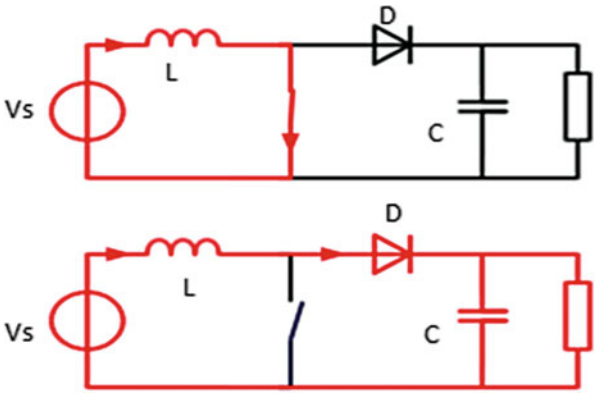

Fig. 7.8 The two configurations of a boost converter, depending on the state of the switch S

to the combined voltage. The capacitor provides voltage and energy to the load only when the switch is closed and the right hand side is shorted out from the left hand side. In the course of this time, the discharging of capacitor through the switch is prevented by the blocking diode. To prevent the capacitor from discharging too much, the switch must be opened fastly again.

Two distinct states of principle of boost converter are:

- The inductor current is increased when the switch is closed and is in on- state.
- The inductor current is flowed through the fly back diode D, the capacitor C and the load R when the switch is open and is in off-state. The energy accumulated during the on-state is transferred into the capacitor.

Figure 7.8 infers that the input current is same as the conductor current. Hence it is not discontinuous as in the buck converter. The input filter requirements are also relaxed when compared to buck converter.

7.2.3 SIMULINK Model of Boost Converter

The output voltage of 272 V DC obtained from the 2 KW panel is stepped up to about 500 V DC by means of boost converter shown in Fig. 7.9.

7.2.3.1 Design Parameters

The parameters involved in the design of boost converters are shown below:

(i) $V_0 = \frac{V_S}{1-K}$

(ii) $L = \frac{K(1-k)R}{2f}$

(iii) $C = \frac{K}{2fR}$

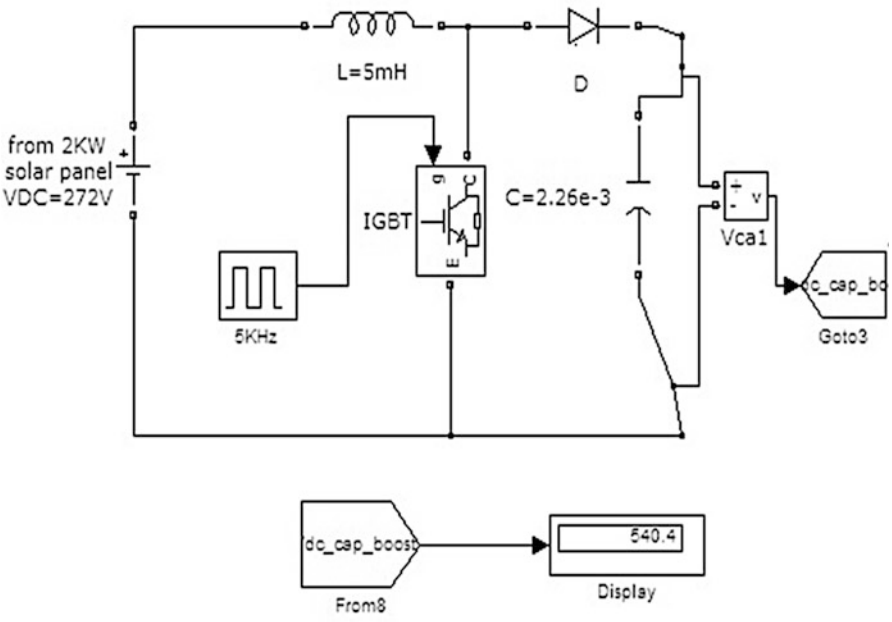

Fig. 7.9 SIMULINK model of boost converter

Table 7.4 Boost converter design values used in simulation

S. No.	Parameter	Value
1	Input voltage (V_s)	273 V
2	Output voltage (V_0)	500 V
3	Switching frequency (f)	5 KHz
4	Duty cycle (k)	0.456
5	Inductor (L)	5 mH
6	Capacitor (C)	0.226 μF

where

$V_0 =$ output voltage(V)
$V_s =$ input voltage(V)
K = duty cycle = Ton/T
F = switching frequency (Hz)

The parameters and their values are set in the simulation according to Table 7.4.

7.2.3.2 Voltage Source Inverter (VSI)

The VSI inverter is used in this grid integration model to regulate the DC 500 V from the boost converter. To achieve full control of the utility-grid current, the

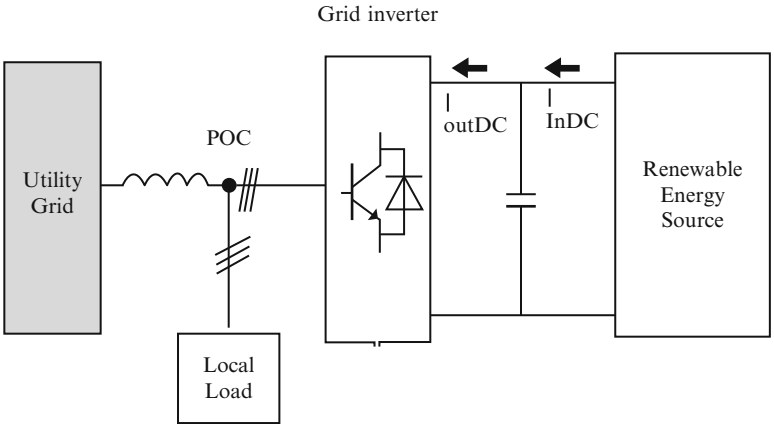

Fig. 7.10 Block diagram of grid inverter

DC-link voltage must be boosted to a level higher than the amplitude of the grid line voltage. In order to keep the DC-link voltage constant the power flow of the grid side inverter is controlled. Figure 7.10 shows the block diagram of grid inverter, with local load and grid interconnection.

The three- phase VSI is composed of a bridge with six reverse blocking switches (S1–S6) and each have IGBT and a series diode. The inductor is considered as the main storage component of the DC-link at the output. During unintended open circuit of bridge the transient voltage suppressor diode D provides a "freewheeling" path. The VSI is appropriate with IGBTs during commutation as their intrinsic body diodes are inactive. These have poor switching losses. Three phase inverters are commonly used in the application of AC motor drive and UPS. The circuit consists of six power semiconductor devices like transistors and six diodes. The change in firing from one switch to next in proper sequence for one cycle of 360° is known as step.

180 Degree Conduction

(i) Each switch conducts for 180°
(ii) Switch S1–S4 state change will occur after 180°
(iii) Upper arm switches S1, S3, S5 state change will occur at every 120°

At any instant of time, three devices conduct. Thus effective utilization of the switch is achieved. The switching sequence of VSI for 180° is shown in Fig. 7.11 and the states are shown in Table 7.5.

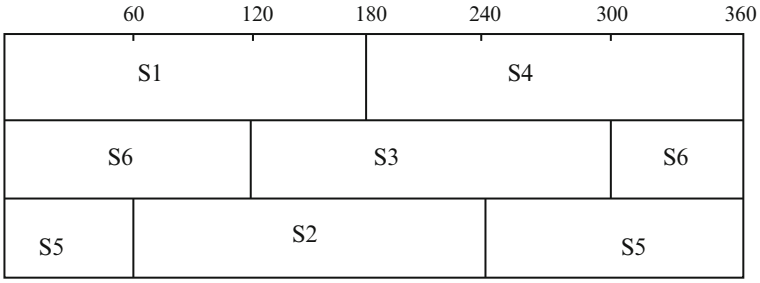

Fig. 7.11 Switching sequence of VSI for 180 conduction

Table 7.5 Switch states for three phase VSI

State		State no.	Switch state (binary)	V_{ab}	V_{bc}	V_{ca}	V_{an}
On	Off						
S6, S1, S5	S3, S4, S2	1	101	V_s	$-V_s$	0	$\frac{V_s}{3}$
S1, S2, S6	S4, S5, S3	2	100	V_s	0	$-V_s$	$\frac{2V_s}{3}$
S2, S3, S1	S5, S6, S4	3	110	0	V_s	$-V_s$	$\frac{V_s}{3}$
S3, S4, S2	S6, S1, S5	4	010	$-V_s$	V_s	0	$\frac{-V_s}{3}$
S4, S5, S3	S1, S2, S6	5	011	$-V_s$	0	V_s	$\frac{-2V_s}{3}$
S5, S6, S4	S2, S3, S1	6	001	0	$-V_s$	V_s	$\frac{-V_s}{3}$
S1, S3, S5	S4, S6, S2	7	111	0	0	0	0
S4, S6, S2	S1, S3, S5	8	000	0	0	0	0

7.2.4 Implementation of Grid Integration Using MATLAB

In the grid development shown in Fig. 7.12 using MATLAB/SIMULINK, first the generating station is represented by a programmable voltage source of 120 KV, 2,500 MVA capacity. Then the 120 KV is stepped down to 25 Kv by means of a star-delta transformer. In this type of connection, then primary is connected in star fashion while the secondary is connected in delta fashion as shown in the Fig. 7.13.

7.2.4.1 Grounding Transformers

A ground path is provided to an ungrounded "Y" or a delta connected system through a grounding transformer. Grounding transformers are usually used to:

1. The system neutral at or near ground potential is maintained by providing a relatively low impedance path to ground.
2. The transient over voltage magnitude is limited during the occurrence of re-striking ground faults.
3. A source of ground fault current is provided during line-to ground faults.
4. The connection of phase to neutral loads is permitted when required.

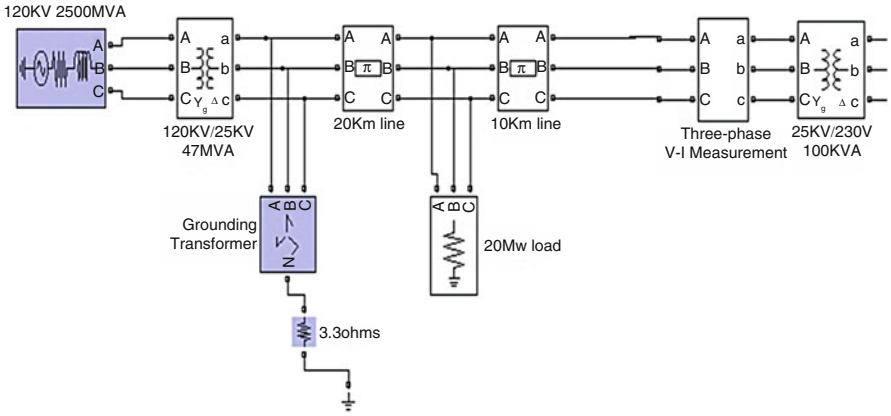

Fig. 7.12 SIMULINK model of grid development

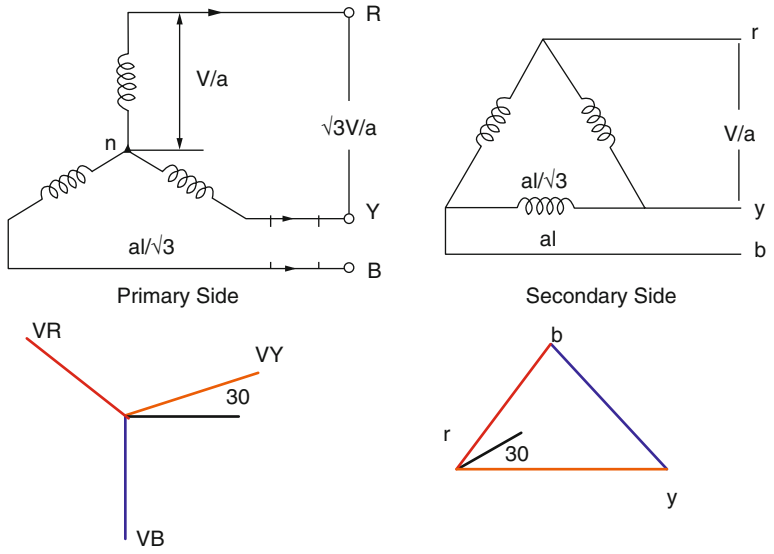

Fig. 7.13 Star – delta configuration of transformer

The transmission line is represented by a 'pi section line of 10 and 20 km. Then the 25 KV is stepped up to 230 V by means of a star-delta transformer. The setup as a whole forms the grid development. The SIMULINK Model of the grid integration using six IGBT switches is shown in Fig. 7.14. The model designed to generate pulses for the VSI inverter is shown in Fig. 7.15. Figure 7.16 shows the output voltage and current waveforms before 25 KV/230 V in the grid and Fig. 7.17 shows the output voltage of the inverter to the grid.

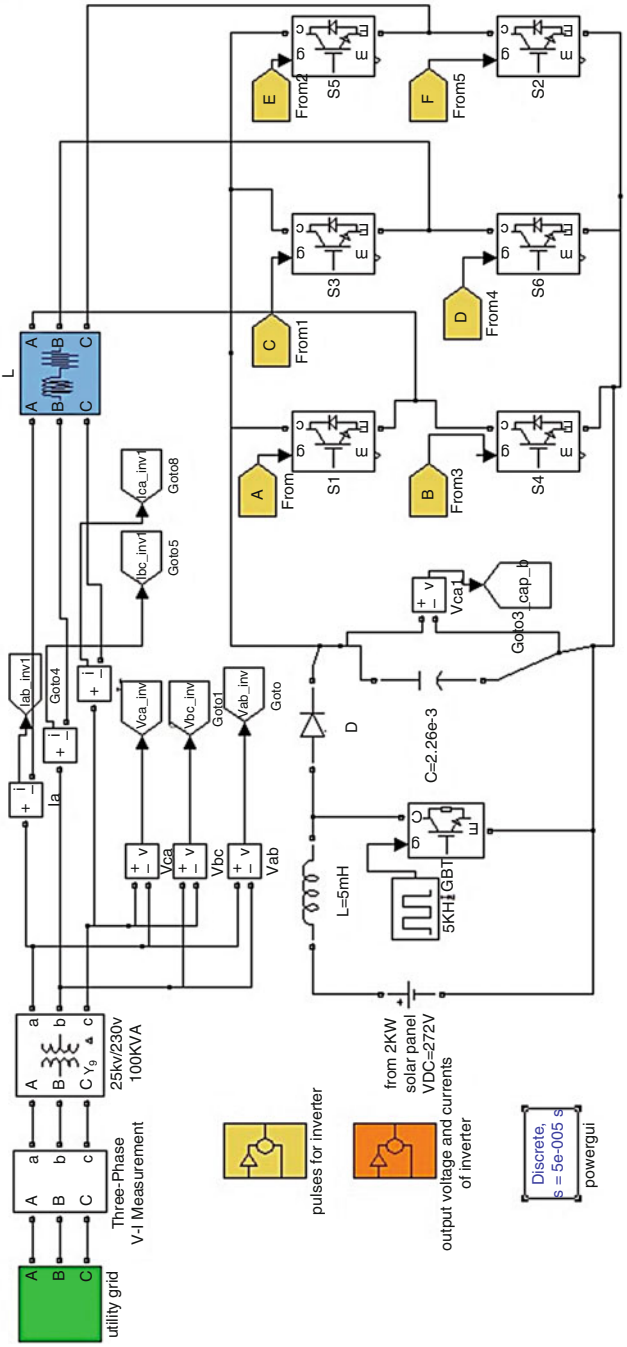

Fig. 7.14 SIMULINK model for solar PV grid integration

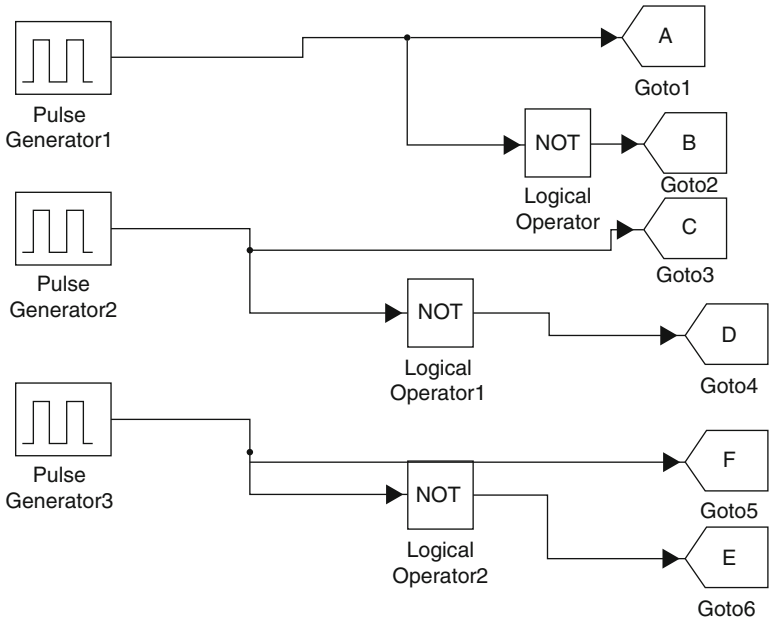

Fig. 7.15 SIMULINK model – pulses for inverter

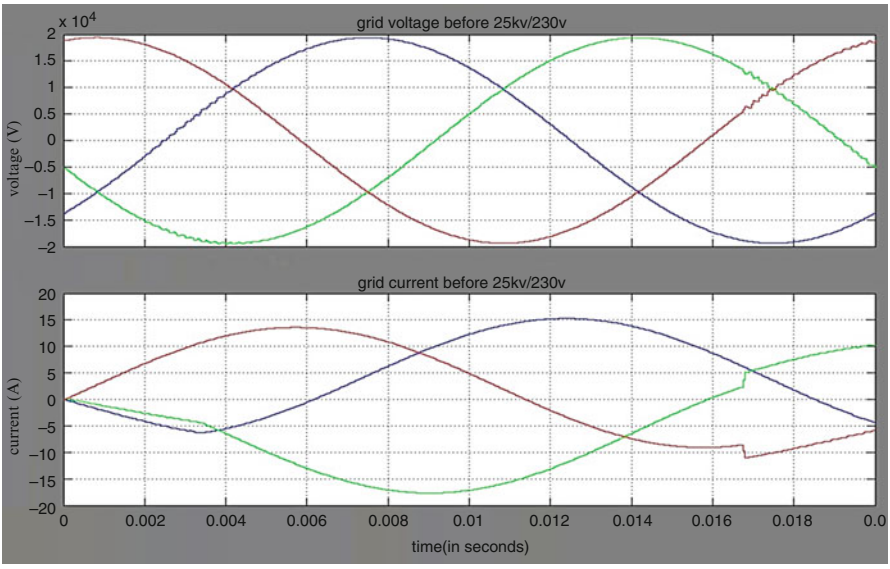

Fig. 7.16 Voltage and current waveforms before 25 KV/230 V in the grid

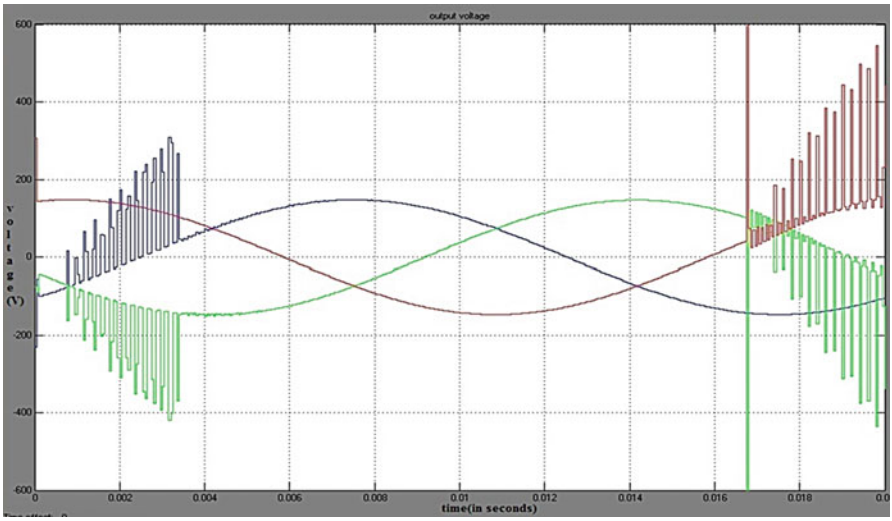

Fig. 7.17 Output voltage of the inverter to the grid

The MATLAB/SIMULINK is used to develop the solar PV grid integration models and their respective waveforms are shown. Certain technical requirements encouraged the utility industries with the deployment over 15–20 % range. Such work needed areas include:

- Integration of all characteristics from the transient to long-time domain and storage control.
- Sophisticated adaptive controls for combination and re-combination of PV resources.
- PV resources modeling and forecasting, from the feeder level to all the control areas.
- The nationwide grid is exploited to the fast response of inverter based generations by adapting the operating and reliable strategy.
- Adaptive techniques like advanced permissive signal anti-Islanding for self-identification of phase, feeder, and substation are exploited to low bandwidth requirement and for low-cost signal generators.

7.3 Phase Locked Loop for Grid Connected Power System

A Voltage Source Inverter (VSI) is connected to the supply network through a filter in many grid- connected power electronic systems like Static Synchronous Compensators (STATCOM), Unified Power Flow Controllers (UPFC) and Distributed Generation System (DGS). The switching harmonics entering the distribution network is reduced by this series inductance filters. LCL network is the alternative

filter which achieves the aforesaid requirement which has high potential benefits for high power applications. But more complex control strategies are required for the system which incorporates LCL filters and are not commonly presented in literature. A robust strategy for regulating the grid current entering a distribution network from a three phase VSI system connected via a LCL filter. An outer loop grid current regulator with inner capacitor current regulation strategy is integrated to stabilize the system. For the outer grid current control loop a synchronous frame PI current regulation strategy is used.

This section investigates and compares new control techniques to properly regulate the power flow between renewable source and the utility network. The control strategies are typically based on a fast and accurate detection of the phase angle of the grid voltage which may be estimated by using a Phase Locked Loop (PLL) control circuit. Here performances of four different PLLs that are investigated are Synchronous Reference Frame PLL (dq PLL), Stationary Reference Frame PLL (αβ PLL), Decoupled Synchronous Reference Frame PLL (DSRF PLL) and Decoupled Stationary Reference frame PLL (Dαβ PLL). The Decoupled Stationary Reference Frame PLL (Dαβ PLL) may be an appropriate solution to use in an interconnected RES with Fault Ride Through (FRT) capability, since it prevails the other PLLs with regards to its accuracy under unbalanced faults. Further, it has a lower deviation of the estimated phase after the fault occurs. The performance of the New Hybrid Dαβ PLL is verified through simulations and experiments. Further the new PLL is used in an interconnected RES through experiments under normal and FRT operation.

Special attention is given to systems which demand a third order Inductor-Capacitor-Inductor (LCL) filter as interface between converter and grid. This filter configuration is widely employed in high power systems, in which the switching frequency is typically limited by the switching devices. The LCL filter has the ability to reduce the level of harmonic distortion with less inductance, when compared to the first order Inductor (L) filter. Also, the evaluation of different current controllers employed for grid-connected distributed power generation systems are discussed. The MATLAB/SIMULINK models are developed to investigate the performance of the control strategies discussed in the literature.

The environmental regulations due to green house gas emission, the electricity business restructuring, and the recent development in small scale power generation are the main factors driving the energy sector into a new era, where large portions of increases in electrical energy demand will be met through wide spread installation of distributed resources or what's known as DGS. As a result, DGS can give commercial consumers various options in a wider range of high reliability-low price combinations.

The customer and utility requirements, such as compensation of reactive power and higher harmonic components, compensation of power quality events, power factor correction, peak saving, backup generation, and voltage reliability enhancement requirements are also meet in the DGS power system which is not possible with centralized generation. Within a micro-grid the DGS can operate either in Grid-connected mode or in an islanded mode. DC-AC Pulse Width Modulated

(PWM) Voltage Source Inverter (VSI) systems is used to interface the major distributed resources to the utility grid or to the customer load. Different sizes of DGS units ranging from few kW up to 1.6 MW can be interfaced through current power electronic technologies. When compared to the conventional rotary generators the inverter interface makes the energy sources more flexible and controllable.

7.3.1 Challenges Imposed on an Inverter-Based DG Interface

The dynamic and uncertain nature of a distribution network challenges the control and stability of the DGS interface system. The fact that a typical distribution system faces unavoidable disturbances and uncertainties complicates the design of a practical inverter-based DGS interface. In the Grid-connected mode, most of system disturbances are related to the main grid due to the relatively small size of DGS energy sources. Various grid disturbances can be imposed on the DGS interface. Difficulties occur in the following ways:

- Depending on the grid configuration, a large set of grid impedance values is yielded as DGS is commonly installed in weak grids with long radial distribution feeders. The interfacing impedance variations directly affect the stability of the inner controls of the DGS interface. With that, high frequency resonance dynamics might be excited due to the grid impedance interaction with the AC side filter of the DGS interface. Due to this, high distortion of injected current may propagate through the system which will drive other voltage and current harmonics.
- There is a strong trend toward the use of current control for PWM inverters in DGS, which offers the possibility of high power quality injection when it is properly designed. In this approach, it is commonly desired to design the inner current control loop with high bandwidth characteristics to ensure accurate current tracking, shorten the transient period as much as possible, and force the VSI to equivalently act as a current source amplifier within the current loop bandwidth. But, the sensitivity of the dominant poles of the closed loop current controller becomes very high to uncertainties in the total interfacing impedance (the impedance seen by the inverter at the point of common coupling, which is a function of the grid impedance) when the current control loop is designed with high bandwidth characteristics (e.g. Deadbeat control performance).
- The control performance of the DGS inverter is directly affected by the voltage at PCC. The grid voltage at the PCC is more distorted in weak grids with long radial distribution feeders due to the exposure to nonlinear loads.
- Grid faults, time- varying loads, non-dispatchable generation, voltage transients associated with parallel connected loads, and voltage transients caused by capacitor switching may cause severe and random voltage disturbances. Interfacing DGS should have high immunity and ability to override aforesaid disturbances especially in feeders with sensitive loads.

In the presence of the aforementioned system challenges, along with the reliability and cost enhancements, significant performance enhancements can be obtained by eliminating the grid voltage sensors in the Inverter-based DG interface. Among these are: (1) The elimination of the residual negative sequence and voltage feed-forward compensation errors, and (2) The positive contribution to the robustness of the power sharing mechanism.

The stability and control effectiveness of a grid-connected inverter-based DGS interface is affected by the uncertain and dynamic nature of the distribution network. Usually, grid impedance and interfacing parameter variations, grid voltage disturbances, and interaction with existing grid harmonics and unbalance are the possible challenges. A strong DGS interface should be developed to overcome these challenges and to make a safe integration and larger penetration of DGS. The characteristics which are offered by the DGS are as follows:

- Distribution system insensitivity and AC side filter parameters.
- Perfect current control performance with a strong capacity of eliminating the grid distortion and voltage disturbances caused by interfacing parameters mismatch and compensating for inverter system delays.

7.3.2 Requirements for Establishing a Grid Connection

The general grid code requirement for investigating the dynamic behavior of DGS is listed in this section. In countries like USA, Germany, Spain, Denmark, China and India which have substantial generation have imposed the grid codes. Main grid codes for operation and grid connection are listed as below:

7.3.2.1 Voltage Regulation

The voltage should not go outside the specified range at the Point of Common Coupling (PCC) during DGS connection.

7.3.2.2 System Frequency

The frequency variations should not go outside a specified range.

7.3.2.3 Synchronization

The voltage fluctuation due to synchronization of DGS with an area Electric Power System (EPS) should not be more than ± 5 % of the prevailing voltage level at the PCC.

7.3.2.4 Monitoring Provisions

250 kW or larger DGS rating will have provisions for monitoring connection status and real and reactive power output at the point of DGS connection.

7.3.2.5 Isolation Device

An isolation device shall be located between the DGS unit and the area EPS when required.

7.3.2.6 Grounding

Proper coordination is required among the grounding scheme and the grounding fault protection of DGSs with the EPS operators.

7.3.2.7 Voltage Disturbances

A DGS should cease to energize the EPS within a specified clearing time during abnormal voltage conditions.

7.3.2.8 Frequency Disturbances

A DGS should cease to energize the EPS within a specified time when the frequency is not within the limits.

7.3.2.9 Loss of Synchronization

The disconnection of 250 kW or larger DGS from the area EPS without intentional time delay can be made with synchronism loss protection.

7.3.2.10 Reconnection

The DGS will stop to energize the area EPS and remain disconnected until the area EPS voltage and frequency have returned to and maintained normal range for 5 min after an out-of-bound disturbance.

7.3.2.11 Anti-islanding

The DGS can detect the island condition and stop to energize the area EPS within 2 s from the formation of an Island.

7.3.2.12 Harmonics

The permissible voltage harmonic distortion is specified at the PCC. A maximum voltage total harmonic distortion of 5 % and maximum individual frequency voltage harmonics is 3 % of the fundamental component is usually required.

7.3.2.13 DC Current Injection

A DGS and its interconnection system will not inject dc current greater than 0.5 % of its rated output current into the area EPS at the PCC.

7.3.2.14 Flicker

The DGS will not create any objectionable drop for customers on the area EPS.

7.3.3 Grid Synchronization Algorithms

Some various grid synchronization algorithms that are presented in literature are discussed below:

7.3.3.1 Zero Crossing Detectors

Transition of AC voltage from one polarity to another is detected by the Zero Crossing Detector (ZCD). A pulse is generated showing 0° for a transition from positive to negative and 180° for the reverse case.

Drawbacks of Zero Crossing Detectors

The power quality phenomenon affects the performance of ZCD badly. Figure 7.18 shows the performance of ZCD during the presence of harmonics and notches.

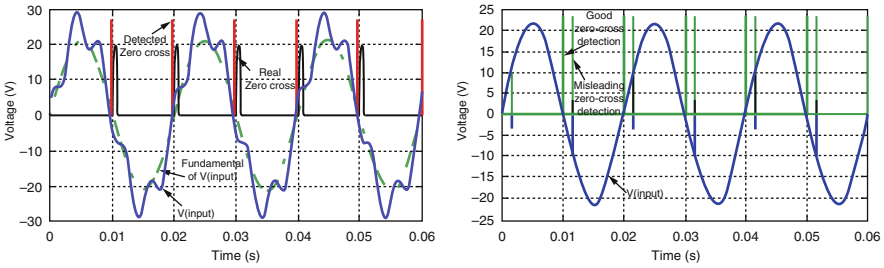

Fig. 7.18 Misleading zero cross detection due to harmonics and notches

Input wave transients also affect the performance of ZCD. The zero crossing detector detects the zero crosses once or twice during every cycle. This implies that even the phase jump occurrence is not estimated until the next zero cross. Frequency deviations may lead to severe malfunctioning of the system since the ZCD does not provide frequency estimation or adaptation.

The performance of the zero crossing detectors can be improved by applying some of the following improvement techniques. In three phase circuits the usual practice is to filter out the y-phase signals and to extrapolate the r-phase signals. Digital filters in discrete devices can provide better results when the fundamental component is extracted from noisy waveform. The performance of the normal ZCD can be improved by implementing suitable algorithm in discrete devices.

7.3.3.2 Phase Locked Loop

A system which synchronizes its output signal with a given input signal or reference signal both in frequency and in phase is known as Phase Locked Loop (PLL). It is a non-linear closed loop control which changes the frequency of a controlled oscillator automatically depending on the frequency and phase of the input signal such that the output is synchronized both in frequency and phase with the reference or the input signal.

The following are the main components of a PLL

(i) A **phase detector** generates an error signal by comparing the input/reference signal with the output signal.
(ii) A **loop filter** removes unwanted harmonics terms from the error signal.
(iii) A **voltage controlled oscillator (VCO)** which generates the output signal whose frequency varies around a central frequency depending on the output of the loop filter. Figure 7.19 shows the block diagram of a PLL.

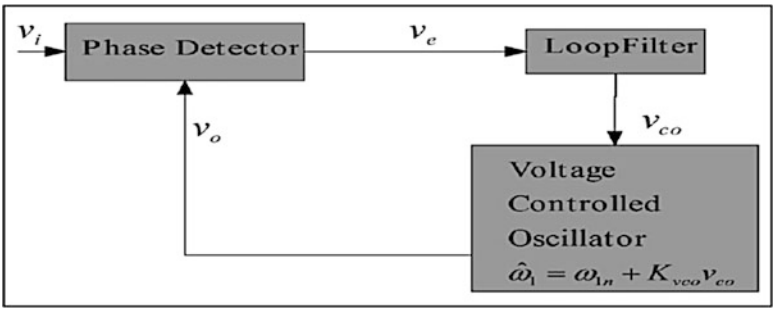

Fig. 7.19 3.2 block diagram of PLL

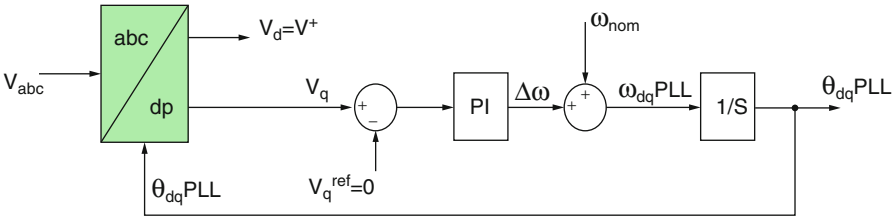

Fig. 7.20 The structure of a dq PLL

7.3.4 PLLs for Three Phase Systems

In this section, three different PLLs for three phase systems are presented in order to motivate the development of a hybrid PLL, Decoupled Stationary Reference Frame PLL (Dαβ PLL).They are:

- Synchronous Reference Frame PLL (dq PLL).
- Stationary Reference Frame PLL (αβ PLL).
- Decoupled Synchronous Reference Frame PLL (DSRF PLL).

7.3.4.1 Synchronous Reference Frame PLL (dq PLL)

The basic configuration is shown in Fig. 7.20. The dq PLL uses the equations of the Park's transformation, as shown in Eq. 7.1, to translate the abc natural rotating reference frame into the dq-Synchronous Reference Frame (SRF).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix}^{syn} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-120) & \cos(\theta+120) \\ -\sin\theta & -\sin(\theta-120) & -\sin(\theta+120) \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{7.1}$$

In this PLL either direct axis component or quadrature axis component of voltage can be considered for the estimation of frequency or hence phase angle. A crucial aspect of the transformation is that the voltage of the d-axis (V_d) has to lie on the voltage of phase A. This is achieved by having the voltage of the q-axis (V_q) to track zero through a Proportional-Integral (PI) controller and therefore frequency, ω_{dqPLL} and phase, θ_{dqPLL} could be estimated as illustrated in Fig. 7.20. In this PLL, the PI controller performs the function of Loop filter in the basic PLL. The angle θ_{dqPLL} is found integrating the output ω_{dqPLL} which uses the error signal $V_q - V_q^{ref}$ in the dq frame.

When a balanced fault occurs, the dq PLL is operating well and can track the phase angle. However, when an unbalanced fault occurs, then the dq PLL fails to track accurately the phase angle because V_d does not perfectly match with the positive sequence voltage V^{+1} due to the oscillation which appears because of the existence of the negative sequence voltage V^{-1} under unbalanced disturbances.

7.3.4.2 Stationary Reference Frame PLL (αβPLL)

The basic configuration of a Stationary reference frame PLL is shown in Fig. 7.21. The αβ PLL sets $\theta = 0$ in that of dq PLL, in order to translate the αβ natural rotating reference frame into the αβ-stationary reference frame. Trigonometric equations are used in order to estimate the phase angle $\theta_{\alpha\beta PLL}$ as shown in Eqs. 7.2 and 7.3. It should be noticed that the below expression is valid if $\Delta\theta$ is small.

$$\Delta\theta = \theta_{gr} - \theta_{abPLL} \approx \sin\left(\theta_{gr} - \theta_{abPLL}\right) \tag{7.2}$$

$$\Leftrightarrow \Delta\theta \approx \sin\left(\theta_{gr}\right)\cos\left(\theta_{abPLL}\right) - \cos\left(\theta_{gr}\right)\sin\left(\theta_{abPLL}\right) \tag{7.3}$$

The objective of the closed loop control of αβPLL (Fig. 7.21) is to induce the difference $\Delta\theta$ to be controlled to zero by using a PI controller, where θ_{gr} is the actual phase angle of the voltage. The αβPLL in unbalanced operation has similar problems to those mentioned for the dq PLL.

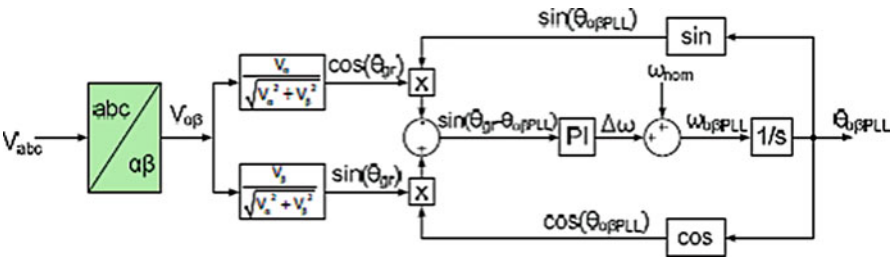

Fig. 7.21 The structure of αβ PLL

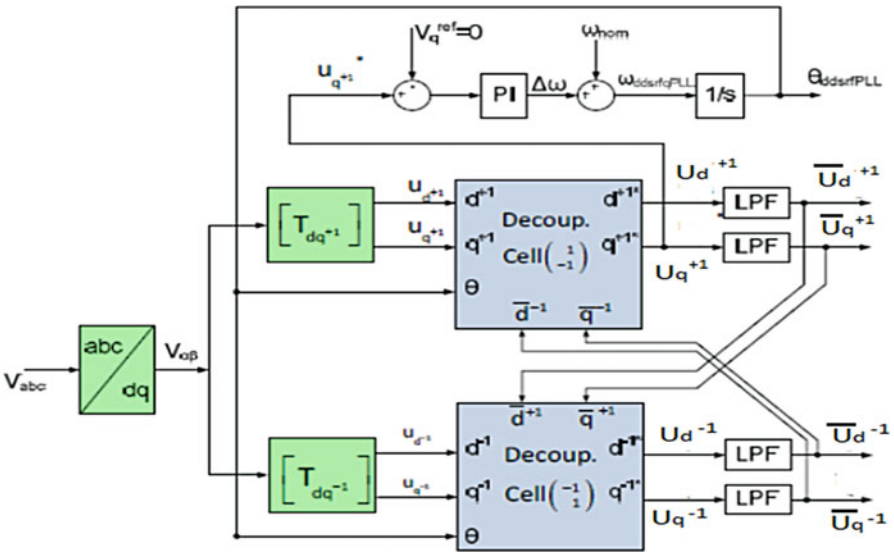

Fig. 7.22 The structure of a DSRF PLL

7.3.4.3 Decoupled Synchronous Reference Frame PLL (DSRFPLL)

The DSRFPLL stems from improving the conventional dq PLL. It consists of a decoupling network and phase locked loop operating on synchronous reference frame (dq PLL) as shown in Fig. 7.22. The decoupling network provides positive and negative sequence components from the input voltage vector. The synchronization to the positive sequence component of the grid voltage is achieved when the voltage positive sequence q-component is controlled to zero. This is done using dq PLL.

During the unbalanced three phase grid voltage, the fundamental positive-sequence voltage vector is appeared as a DC voltage on the dq^{+1} axes of the positive sequence SRF and ac voltages at twice the fundamental utility frequency on the dq^{-1} axes of the negative sequence SRF. Opposing to this the negative sequence voltage vector will cause a dc component on the negative sequence SRF and an ac oscillation on the positive sequence SRF. In order to cancel out the amplitude oscillation of the positive sequence SRF which matches to the DC level on the negative sequence SRF and vice versa, a decoupling network is applied to signals on the dq positive/negative SRF axes. DC component from the signal on the decoupled SRF axes can be extracted by using low pass filters. The information about the amplitude and phase angle of the positive and negative sequence components of the grid voltage vector can be collected by these DC components.

The DSRF PLL loop controller works on the decoupled q-axis signal of the positive sequence SRF (U_q^{+1}). Due to the effect of decoupling cells the signal is free from ac components and therefore the loop controller band width is increased.

7.3.4.4 Decoupling Network

The unbalanced grid voltage vector $u_{\alpha\beta}$ can be expressed in stationary reference frame as shown in Eq. 7.4.

$$u_{\alpha\beta} = \begin{matrix} u_\alpha \\ u_\beta \end{matrix} = U^+ \begin{bmatrix} \cos(\omega t + \varphi^+) \\ \sin(\omega t + \varphi^+) \end{bmatrix} + U^- \begin{bmatrix} \cos(-\omega t + \varphi^-) \\ \sin(-\omega t + \varphi^-) \end{bmatrix} \tag{7.4}$$

where U is the phase voltage peak value, ω is the grid angular frequency and φ is initial angle. The positive and negative sequences are represented by + and − superscripts. The positive sequence reference frame is assumed to rotate synchronously with the fundamental frequency positive sequence grid voltage component. Therefore, $\theta_{sync} = \omega t$. Angle θ_{sync} which is the output of the SRF-PLL of synchronous dq reference frame is used to express the positive and negative sequence components.

$$u_{dq}^+ = \begin{bmatrix} u_d^+ \\ u_q^+ \end{bmatrix} = T_{dq}^+ \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta_{sync}) & \sin(\theta_{sync}) \\ -\sin(\theta_{sync}) & \cos(\theta_{sync}) \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} =$$
$$U^+ \begin{bmatrix} \cos(\varphi^+) \\ \sin(\varphi^+) \end{bmatrix} + U^- \cos(\varphi^-) \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + U^- \sin(\varphi^-) \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \tag{7.5}$$

$$u_{dq}^- = \begin{bmatrix} u_d^- \\ u_q^- \end{bmatrix} = T_{dq}^- \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} \cos(\varphi^-) \\ \sin(\varphi^-) \end{bmatrix} + U^+ \cos(\varphi^+) \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix}$$
$$+ U^+ \sin(\varphi^+) \begin{bmatrix} -\sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \tag{7.6}$$

The left side terms and right side terms of the Eqs. 7.5 and 7.6 represents the DC and AC values respectively. The DC-values are solved in order to differentiate the positive and the negative sequence components from the grid voltage.

$$U^+ \begin{bmatrix} \cos(\varphi^+) \\ \sin(\varphi^+) \end{bmatrix} = \begin{bmatrix} U_d^+ \\ U_q^+ \end{bmatrix} = \begin{bmatrix} u_d^+ \\ u_q^+ \end{bmatrix} - U^- \cos(\varphi^-) \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix}$$
$$- U^- \sin(\varphi^-) \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \tag{7.7}$$

$$U^- \begin{bmatrix} \cos(\varphi^-) \\ \sin(\varphi^-) \end{bmatrix} = \begin{bmatrix} U_d^- \\ U_q^- \end{bmatrix} = \begin{bmatrix} u_d^- \\ u_q^- \end{bmatrix} - U^+ \cos(\varphi^+) \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix}$$
$$- U^+ \sin(\varphi^-) \begin{bmatrix} -\sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \tag{7.8}$$

Figure 7.23 represents the decoupling network based on Eqs. 7.7 and 7.8 which is used to cancel AC components from positive and negative sequence reference

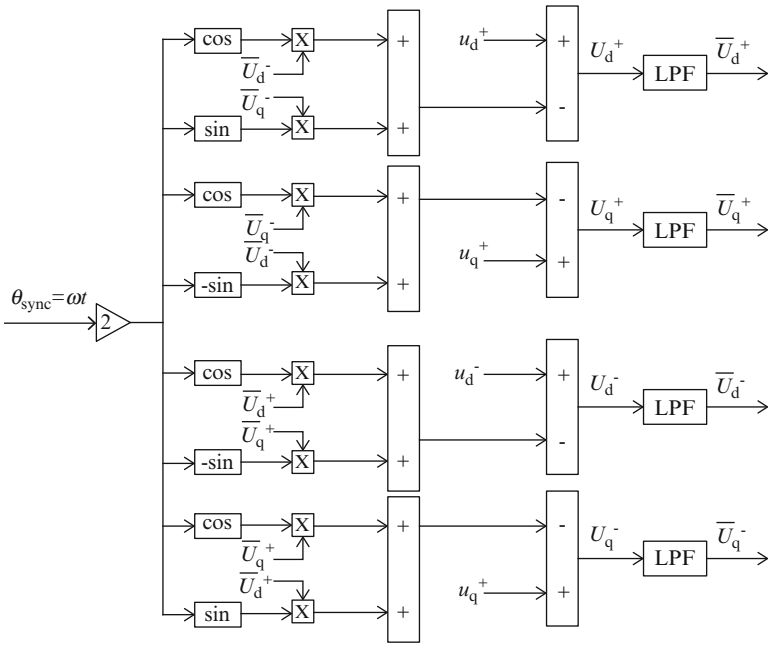

Fig. 7.23 Decoupling network

frames. The block LPF represents a simple first order low-pass filter with cut-off frequency of ω_f as shown in Eq. 7.9.

$$LPF(s) = \frac{\omega_f}{s + \omega_f} \tag{7.9}$$

The positive and negative sequence component from the input voltage vector is provided by the decoupling network. Hence, it is possible to synchronize the control system instead of GSC sub system to the grid voltage positive sequence component. When the positive sequence q axis voltage component U_q^+ is zero the synchronization of the grid voltage is achieved. In such case, the initial phase angle φ+ is zero and the positive sequence voltage component is aligned to d+ axis rotating with angular speed of ω. The positive sequence voltage component angle θ_{sync} is obtained using SRF-PLL.

The backward numerical approximation can be used to build the discrete controller and the integrator. As shown in the equation the frequency and phase can be then represented considering U_q^{+1} as the error to be minimized. ω_{nom} represents the feed forward nominal frequency as shown in Eqs. 7.10 and 7.11.

$$W(Z) = \frac{(K_p + K_i T_s)Z - K_p}{z - 1}.U_q^{+1}(Z) + w_{nom} \tag{7.10}$$

$$\theta^{+'} = \frac{T_s Z}{z - 1}.W(Z) \tag{7.11}$$

Finally the sample representation provides the equations whose expressions are to be programmed. The frequency feed forward has been included by introducing a initial condition to W′ in the Eqs. 7.12 and 7.13.

$$W'[n+1] = W'[n] + (K_p + K_i T_s)U_q^{+1}[n+1] \tag{7.12}$$

$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s W[n+1] \tag{7.13}$$

Even though the DSRF PLL is more complex than dq PLL, due to its excellent performance under unbalanced conditions of the network it is preferred for industrial applications. The performance of PLL is good even under distorted conditions when there is reduction in bandwidth.

A high overshoot in the phase angle and frequency estimation is appeared during the instant of fault occurrence. This is the only drawback of the DSRF PLL.

7.3.4.5 Decoupled Stationary Reference Frame PLL (DαβPLL)

The results of the investigation of the performance of the three PLLs motivate the development of a new hybrid PLL which is a combination of the abovementioned PLLs and uses the advantages of each PLL.

The effect of the time response of each PLL on the overshoot of the estimated phase angle is investigated and is shown in Fig. 7.24.

The simulation results in Fig. 7.24 show how the changing of the time response settings of each PLL affects the overshoot of the frequency estimation (f_{dqPLL}, $f_{\alpha\beta PLL}$ and $f_{DSRFPLL}$) when a 50 % balanced voltage sag occurs. Clearly the desired faster operation of a PLL causes undesirably higher overshoots in the frequency. An important conclusion from Fig. 7.24 is that the overshoot of αβ PLL is always

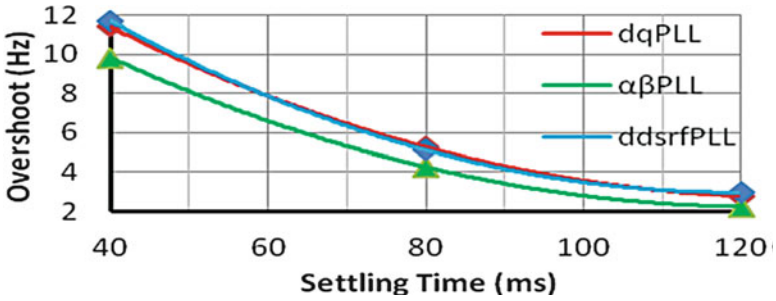

Fig. 7.24 Overshoot response of the three PLLs

lower (18 % lower overshoot on average) in comparison to the other two PLLs and also that dq PLL and DSRF PLL have very similar responses since the structure of the DSRFPLL is based on the dq PLL and on two decoupling cells.

The results in Fig. 7.24 show that the αβ PLL has lower overshoot on the frequency estimation when a fault occurs compared to the two other PLLs under investigation. In addition, the αβPLL faces a problem under unbalanced conditions, in contrast to the DSRF PLL, where the decoupling of the voltage sequence makes it very accurate under balanced and unbalanced conditions. The hybrid Dαβ PLL is a combination of the decoupling cells that are used in DSRF PLL to decouple the voltage sequence and the αβ PLL algorithm to estimate the phase angle of the grid voltage, which offers lower estimation overshoot instead of the algorithm that is used in dq PLL. The new hybrid Dαβ PLL aims at operating very accurately under balanced and unbalanced disturbances and also at having a lower phase angle and frequency overshoot than the DSRF PLL. Therefore, the desired faster operation could be achieved by the suggested Dαβ PLL within the same frequency limits. The structure of the hybrid DαβPLL is illustrated in Fig. 7.25.

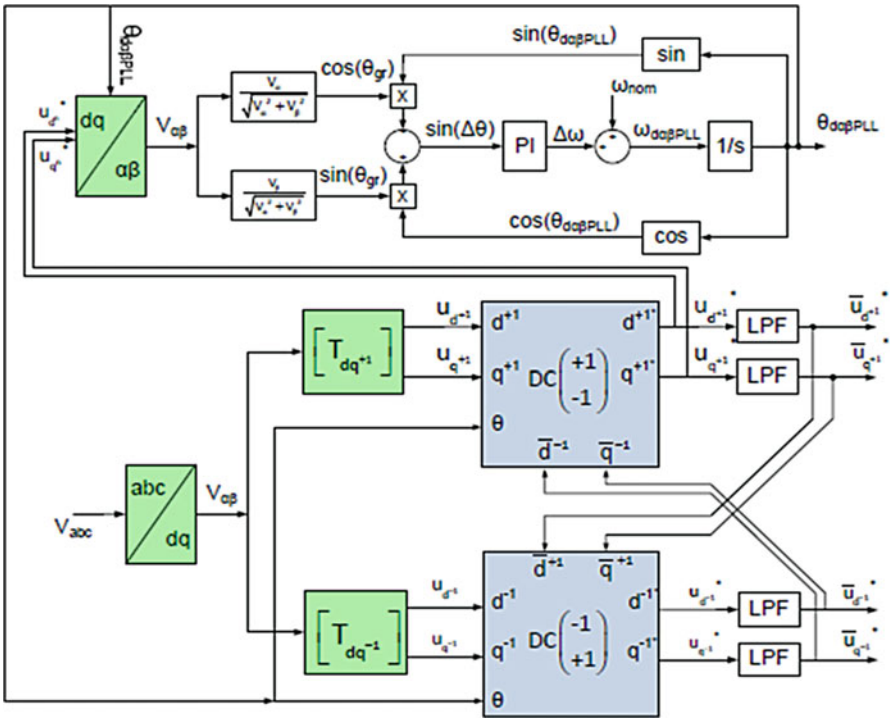

Fig. 7.25 The structure of the hybrid DαβPLL

7.4 Grid Connected Inverters

7.4.1 Inverters

Inverter is a power electronic device which converts the input DC source into an AC source. It is widely used in many applications which require the transportation of bulk power from source to load.

Power inverters produce one of three different types of wave output:

1. Square Wave.
2. Modified Square Wave or Modified Sine Wave.
3. Pure Sine Wave or True Sine Wave.

The three different wave signals represent three different qualities of power output.

7.4.1.1 Square Wave

Square wave inverters were first made but it is no longer used now a days. It delivers uneven power which cannot efficiently drive most devices. Modified square wave inverters came into existence which consistently delivers power and efficient to run devices. Sensitive equipment like medical equipments and variable rechargeable drives requires sine wave which shows great improvement over their predecessors.

7.4.1.2 Modified Sine Wave

Modified sine wave inverter has its own advantages over a true sine wave inverter which has lower efficiency and higher cost. These are the second generation of power inverters. It produces an approximate sine wave with low enough harmonics which do not cause problems with the household equipments. This inverter also has its own disadvantage as the peak voltage varies with the battery voltage. Battery voltage fluctuations may change the behavior of cheaper electronic devices fed by power supply without regulation.

7.4.1.3 True Sine Wave

True sine wave inverters are the recent trend inverters as the power delivered by them has no harmonics and all appliances operate properly. The problem arises with the implementation as the circuit is complex and costly.

Inverter operation depends mainly on the types of switches and their switching pattern which mainly depends on the configuration of the system and required output voltage. Conventionally transistors are used and it may vary as either IGBT (Insulated Gate Bipolar junction Transistor) or Power MOSFET (Metal Oxide

Silicon Field Effect Transistor) based on designer's requirement. IGBT is preferred for higher switching frequencies whereas MOSFET is preferred for little slower frequencies and high power demands.

7.4.2 Pulse Width Modulation Control

Pulse width modulation (PWM) control is used within inverters to obtain constant fundamental magnitude of the output voltage from inverter. PWM control eliminates the use of external circuitry for controlled output. By adjusting the on and off of the inverter components fixed input voltage can be converted to controlled ac voltage output.

The advantages of PWM control scheme are (i) no external circuit required to obtain desired output; (ii) Lower order harmonics are minimized by PWM itself whereas higher order harmonics are eliminated by filters.

Even though PWM scheme posses disadvantages as usage of expensive switching devices, this scheme is popularly used in all industrial equipment. PWM techniques use a constant amplitude pulse whose duty cycle can be varied as per the requirement for each period. Desired output voltage with reduced harmonic content can be obtained by modulating the width of these pulses. Based on the difference in the output harmonic content PWM techniques are classified into many types. Selection of particular PWM technique mainly depends on the acceptable harmonic content in the inverter output voltage.

7.4.2.1 Sinusoidal Pulse Width Modulation (SPWM)

SPWM is very popularly used in industrial applications. The different terminologies used for the same are the triangulation, sub-harmonic or sub-oscillation method.

The high-frequency triangular carrier wave, V_c is compared with a sinusoidal reference, V_r of the desired frequency to realize SPWM. In Figs. 7.27 and 7.28, V_c and V_r waves interact to determine the switching pattern of the modulated pulses. The magnitude and frequency of these signals are arbitrary. V_c represents the peak value of triangular carrier wave and V_r represents the peak value of the reference signal.

Comparator is used to mix reference control signal and the triangular wave which in turn controls the operation of the switches T_1 and T_6 (shown in Fig. 7.26). The logic behind this control is that when reference wave has higher magnitude than carrier wave the comparator output is high else it is low. The comparator output is processed in a trigger pulse generator such that the output voltage wave of the inverter has a pulse width in relation with the comparator output pulse width. The ratio of magnitude of reference wave to that of the carrier wave is termed as Modulation Index (M_i) i.e., $M_i = \frac{v_r}{v_c}$ and its value vary between 0 and 1. If the

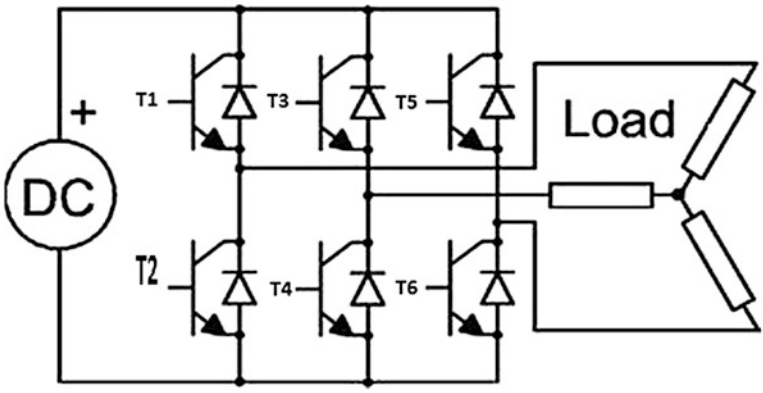

Fig. 7.26 Three phase inverter

triangular wave amplitude is kept constant, the magnitude of fundamental component of output voltage is proportional to the modulation index.

While designing inverters for grid connection designer should be aware of the current standards and regulations which apply in the target country. The National Renewable Energy Laboratory has published the American National Standard ANSI/IEEE 1547 in 2003. Additionally the International Electrotechnical Commission also published the standard IEC 61727.

7.4.2.2 Voltage

PV systems do not influence the grid voltage when it is connected to the grid. Their voltage operation range is more of a protection function that is used for detecting abnormal utility, rather than regulators. Such typical voltage detection may be as defined in and shown in Table 7.6. Trip time refers to the time between the abnormal condition and the inverter ceasing to energize the utility line. The inverter will actually remain connected to the utility to allow the inverter to sense utility electrical conditions for the reconnection process.

7.4.2.3 DC-Injection

The maximum rated output current injected into the power grid under any circumstances is not more than 0.5 % because large and durable DC currents will eventually saturate the transformer's iron core. Saturation leads to the selection of other paths outside the iron core by the magnetic flux and results in increasing leakage flux and lowering of the transformer ratio.

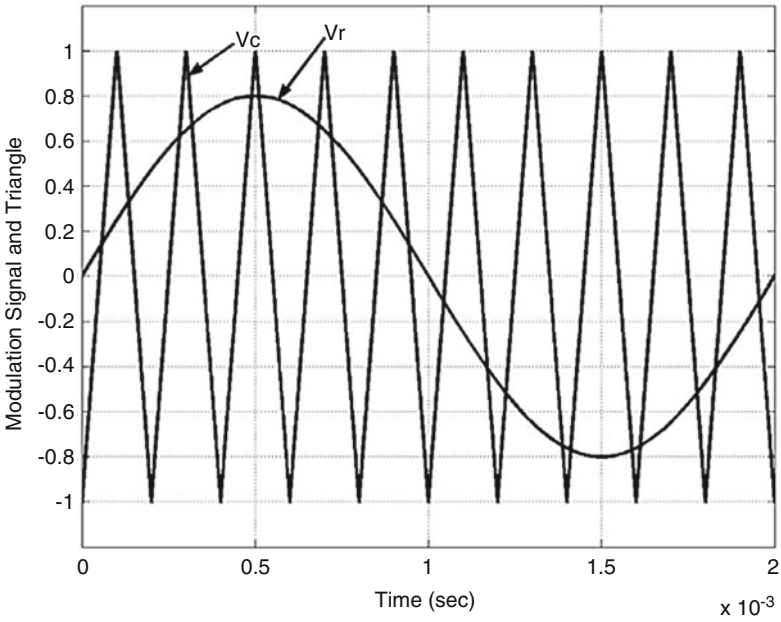

Fig. 7.27 Comparison of sinusoidal and triangular waveforms

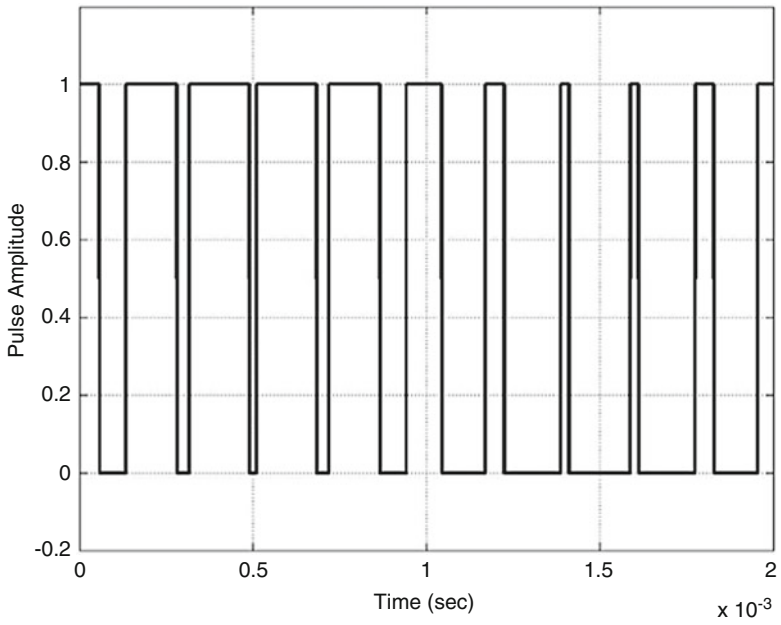

Fig. 7.28 Pulses generated

Table 7.6 Standards of grid-connected inverters

Issue	IEC 61727	IEEE 1547
Nominal power	10 kW	30 kW
Harmonic currents	(3–9) 4.0 %	(2–10) 4.0 %
	(11–15) 2.0 %	(11–16) 2.0 %
	(17–21) 1.5 %	(17–22) 1.5 %
	(23–33) 0.6 %	(23–34) 0.6 %
	Even harmonics shall be less than 25 % of the odd harmonics listed	(>35) 0.3 %
		Even harmonics shall be less than 25 % of the odd harmonics listed
Maximum current THD	5.0 %	5.0 %
Power factor at 50 % of rated power	0.90	–
DC current injection	Less than 1.0 % of rated output current	Less than 0.5 % of rated output current
Voltage range for normal operation	85–110 %	88–110 %
Frequency range for normal operation	50 ± 1 Hz	59.3–60.5 Hz

7.4.2.4 Flicker

Based on IEEE standard, flicker created by the PV system should not cross the acceptable limit. The percentage for this acceptance is not specified in the IEEE standard but it is specified in IEC as limits for the flicker for short term duration should be less than 1 s and for long term flickers the duration has to be less than 0.65 min.

7.4.2.5 Frequency

Inverter and power grid are always synchronized during the operating periods but if the grid itself goes outside some specified frequencies, then the PV system must stop providing power to the grid.

7.4.2.6 Current Distortion

Current distortion affects the grid connected devices in a negative manner and hence it should be avoided in any grid. An overview of the maximum allowed harmonic current distortion may be found in Table 7.6. The THD is limited to 5 % of the rated fundamental harmonic. Even harmonics are limited to 25 % of the odd harmonic limit.

7.4.2.7 Power Factor

The power factor can be larger than 0.85 (leading or lagging) in normal conditions when the load is larger than 10 % of the rated power. For reactive power compensation, the utility may allow lower power factors. For small systems the possible contribution of reactive power to the grid is very small that allows it to be excluded and only consider the given power factor provided by the grid.

7.4.2.8 Reconnection

Based on IEEE standards the inverter for some reason ceases to deliver power due to abnormal grid activity, then it may be reconnected to the grid only after the power voltage and frequency has been within normal voltage and frequency ranges for at least 5 min.

Table 7.6 summarizes the current standards dealing with interconnections of PV systems to a grid.

7.4.3 Grid Filter

Renewable power generation mainly depends on the control technology used in grid connected inverters. Fully-controlled power electronic devices IGBT and (Gate Turn-off Thyristor) GTO are to be used, which is modulated by the high frequency PWM.

Due to that the dv/dt and di/dt are ever large. The presence of some vagrant parameters made the harmonic pollution by inducing high order harmonic flow current into the power grid. The inductor filter is most commonly used in the grid-connected inverter. So as to decrease current ripple, the inductance have to be increased. As a result, the volume and weight of the filter increased. Even though the structure and the parameter of the LC filter are easy, the filtering effect is not good because of the uncertainty of network impedance. LCL filter had an inherently high cut-off frequency and strong penetrating ability in low frequency. So LCL filter has come into wide use in the inverter. The challenge arise in the selection of the parameter and control resonance. The structure of LCL filter is shown in Fig. 7.29.

7.4.3.1 Advantages of LCL Filters

The advantages of the LCL filters are listed below

- The LCL filters have the capability of attenuating harmonics at lower frequencies, which is a significant feature for high power applications.
- Precise control of the output current is possible.
- They provide a better decoupling between the filter and grid impedance (as it reduces the dependence of the filter on the grid parameters).
- A lower ripple of the current stress across the grid inductor is achieved.

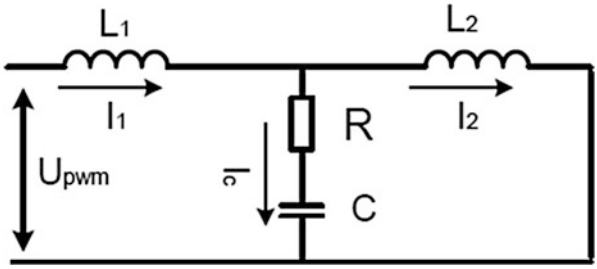

Fig. 7.29 LCL filter with series damping resistor

Table 7.7 Simulation parameters

Grid line-line voltage	Vg = 415 V
Rated active power	P = 5 kW
DC-link voltage	V_{dc} = 400 V
Frequency of grid voltage	f_g = 50 Hz
Switching frequency	f_s = 3 kHz

7.4.3.2 Filter Design

Factors which must be considered for the designing of LCL filter are current ripple, filter size and switching ripple attenuation. The reactive power requirements may cause a resonance of the capacitor interacting with the grid. Therefore, a resistor in series with the capacitor is included for passive or active damping. The required parameters are: V_{rated} – phase voltage (inverter output), P_{rated} – rated active power, V_{dc} – Dc link voltage, f_g – grid frequency, f_s – switching frequency. The selected values are given in Table 7.7.

7.4.3.3 Filter Inductance

Current ripple is the major consideration for the design of L. Smaller ripple results in lower switching and conduction losses. Typically the ripple current can be chosen as 10–15 % of rated current. Current ripples can be considered as 10 %. The value of inductor (L_1) in the system can be obtained from current ripples as given by Eq. 7.14.

$$\Delta I_{L\max} = \frac{\frac{1}{s}V_{dc}}{L_1 * f_s} \tag{7.14}$$

The inductance L_2 is calculated by multiplying the inductance L_1 with an attenuation factor as shown in Eq. 7.15. Here the attenuation factor is selected as 20 %.

$$L_2 = K_a * L_1 \tag{7.15}$$

Table 7.8 Filter values

Filter parameter	Value
L_1	6.6 mH
C	9.20 μF
L_2	1.32 mH
R_f	0.55 Ω

7.4.3.4 Filter Capacitance

Capacitor C selection is mainly based on the reactive power supplied by the capacitor at fundamental frequency. In this design reactive power is chosen as 15 % of the rated power is given by Eq. 7.16.

$$C = \frac{15\% * P_{rated}}{3 * 2\pi f * V_{rated}^2} \tag{7.16}$$

7.4.3.5 Damping Resistance

Because the LCL filter has resonance, the some order harmonic current that come from the grid-connected inverters may increase rapidly. For this reason, adding the damping resistance into filter to suppress the resonances. Generally, it is resistor.

The obtained LCL filter values are shown in the Table 7.8.

7.5 Current Controllers for PWM Inverters

Different reference frames such as synchronous rotating (dq), stationary (αβ), or reference (abc) frame can be used for the control strategy implementation for a distributed generation system. Designing mainly implies on different controller types and their implementation in different reference frames.

Each existing current control techniques have its own characteristics and strengths, which makes it suitable for specific applications. Properties associated to switching frequency, load current distortion and dynamic behavior usually contradict each other. Thus the most appropriate current control method can be selected based on the effective compromise between these characteristics and the nature of the application.

A few current control methods that are used for PWM inverters are shown in Fig. 7.30.

7.5.1 SRF PI Current Controller

The current controller of three-phase VSI plays a major role in controlling grid-connected inverters. The performance of the inverter system is highly affected by the quality of the applied current controller. Among many control mechanisms

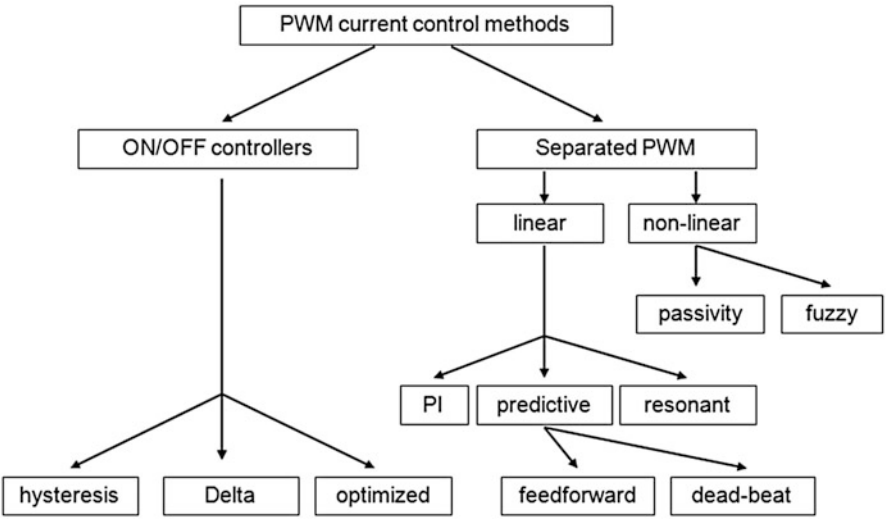

Fig. 7.30 Current controllers for PWM inverters

which have been developed to regulate the inverter output current that is injected into the utility grid, three major types of current controller have evolved: Hysteresis Controller, Predictive Controller and Linear Proportional-Integral (PI) controller. Predictive controller has a very good steady-state performance and provides a good dynamic performance. But, its performance is sensitive to system parameters. The Hysteresis Controller has a fast transient response, non-complex implementation and an inherent current protection. But it has some drawbacks such as variable switching frequency and high current ripples. These cause a poor current quality and introduce difficulties in the output filter design.

The PI controller is the most common control algorithm used for current error compensation. PI controller calculates an error value as the difference between a measured inverter output current and a desired injected current to the grid, then the controller attempts to minimize the error between them. The PI controller calculation algorithm involves two separate constant parameters, the proportional constant K_p and the integral constant K_i. The proportional term of the controller is formed by multiplying the error signal by a K_p gain. This tends to reduce the overall error with time. However, the effect of the proportional term will not reduce the error to zero, and there is some steady state error. The Integral term of the controller is used to fix small steady state errors. The Integral term integrates the error then multiplies it by a K_i constant and becomes the integral output term of the PI controller. This removes the steady state error and accelerates the movement of the process into the reference point.

The advantages of PI current control is that it offers an excellent steady-state response, low current ripple, constant switching frequency, in addition to well-defined harmonic content. Moreover, the controller is insensitive to system

parameters since the algorithm does not need system models. PI controllers can be applied either in the stationary (αβ) or in synchronous (dq) reference frame. When the synchronous PI controller is used, the control variables become DC and the PI compensators are able to reduce the stationary error of the fundamental component to zero whereas with PI controllers working in the stationary system, there is an inherent tracking error of phase and amplitude. Therefore, current control in a synchronous (rotating) reference frame, using PI controllers is the typical solution in the three-phase grid-connected inverters.

Based on the mathematical model of the grid-connected inverter, the output voltages of the inverter in the synchronous (dq) frame are given by Eq. 7.17.

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + R\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega L\frac{d}{dt}\begin{bmatrix} -i_q \\ i_d \end{bmatrix} + \begin{bmatrix} e_d \\ e_q \end{bmatrix} \tag{7.17}$$

where L is the inductance between the grid-connected inverter and the grid; R is the resistance between the grid-connected inverter and the grid; e_d and $e_{q.}$ are the components of the park transformation of the grid voltage; u_d and u_q are the components of the park transformation of the inverter output; ω is the angular frequency of the grid.

The block diagram of the synchronous controller for the grid-connected inverter is represented in Fig. 7.31. It is seen from the figure that the inverter has two PI controllers to compensate the current vector components that are defined in synchronous reference frame (dq). Because of coordinate transformations, i_q and i_d are DC components and therefore, PI compensators reduce the error(s) between the desired current I^*_d (I^*_q) and the actual current I_d (I_q) to zero The output energy

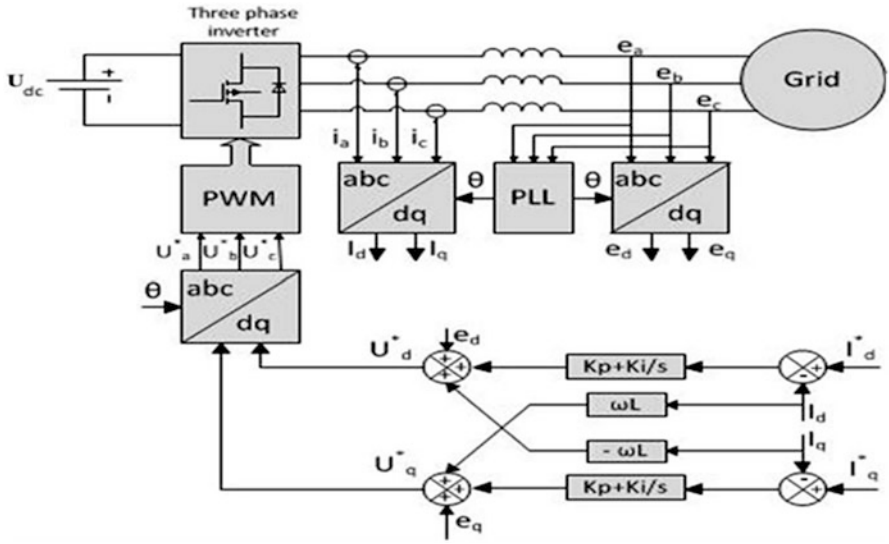

Fig. 7.31 SRF PI controller structure for a grid-connected inverter

and power factor can be controlled by changing d-axis current and q-axis current. The performance of PI controller can be improved by using cross-coupling terms and voltage feed forward.

7.5.2 *Cascaded Deadbeat and PI Controller*

A new effective control strategy named the Cascaded Deadbeat and PI current controller is used for DC-AC voltage source converters, connected to the grid via LCL filters as shown in Fig. 7.32. The advantage of the structure of this control system is intuitive, simple and straight forward. The output current is regulated via a PI controller. The output of PI controller determines the current reference for an inner-loop Deadbeat controller. Thus, the overall control is decomposed into two cascaded parts, facilitating the application of control analysis techniques for the design of a robust and well-damped control system.

Figure 7.32 shows the structure of the control system, which includes an external PI control loop for the output current regulation, stabilized by an inner loop Deadbeat controller for the inverter current. The control scheme is developed to regulate the output current by appropriately modulating the PWM inverter. This is achieved in two stages: the output current iL_2 error is fed to a PI controller, which generates the reference value iL_1^* for the inverter current. The PWM inverter is then modulated according to the output of the inner Deadbeat controller.

In Fig. 7.32, $Z_s = R_s + j\omega L_s$ is the grid impedance. This impedance is incorporated in the impedance L_2 of the filter for the derivation of transfer functions to yield $L = L_2 + L_s$, $R = R_s$.

The DC voltage input to the inverter is assumed to be constant when a reasonably large capacitor is connected at the inverter input. The output voltage of the modulator is modeled as a constant dc voltage per modulation period T_s (100 μs)

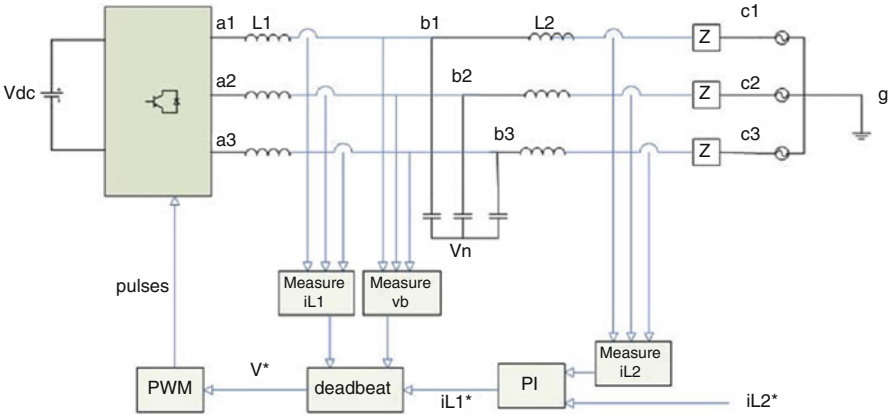

Fig. 7.32 Cascaded deadbeat PI control system

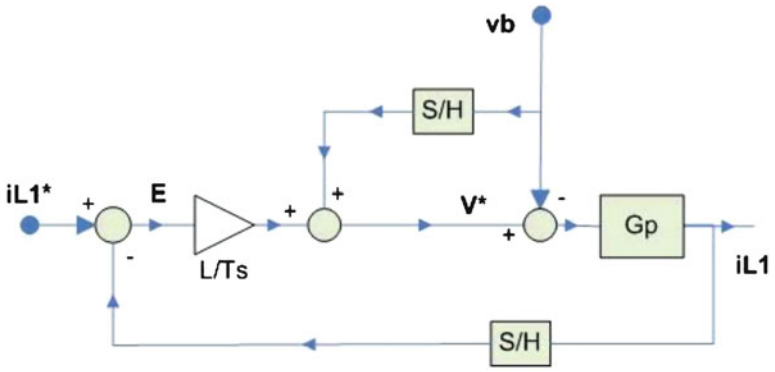

Fig. 7.33 The control diagram for iL_1 referring to d and q axis components

equal to the average value of the input dc voltage. The sampling period for the Deadbeat control is equal to T_s. Both the Deadbeat and PI controllers are analyzed in the synchronous dq frame, which significantly simplifies controller design and stability analysis.

7.5.2.1 Deadbeat and PI Controllers

For a sufficiently short PWM carrier period, T_s, it is possible to calculate the transfer function of the Deadbeat controller shown in Fig. 7.33 with difference equations in the z-plane. Z transform is applied to imply that the capacitor voltage is considered constant throughout T_s, which is valid for sufficiently high switching frequencies. The Principle of this controller is quite simple than other controllers. Feedback of iL_1 is amplified by L_1/T_s and added to the measured capacitor voltage v_b, thus yielding the voltage signal V^* which is fed to the modulator. Given that v_b remains constant over T_s, the transfer function of the above system is given by Eq. 7.18.

$$I_{L1}(z) = \left(I + G_p(z)\frac{L_1}{T_s}\right)^{-1} G_p(z)\frac{L_1}{T_s} {I_{L1}}^*(z) \tag{7.18}$$

where, the transfer function $G_p(z) = V_{ab}(z)/I_{L1}(z)$

Assuming a sufficiently small T_s, $G_p(z)$ is simplified and substituted in Eq. 7.18 yields Eq. 7.19,

$$I_{L1}(z) = \begin{bmatrix} \frac{1}{z} & 0 \\ 0 & \frac{1}{z} \end{bmatrix} {I_{L1}}^*(z) \tag{7.19}$$

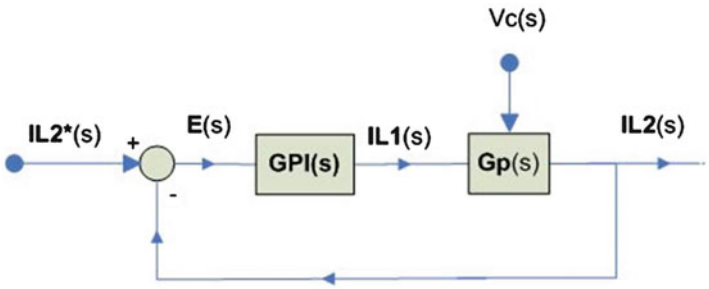

Fig. 7.34 The PI control of I referring to d and q axes components

Figure 7.34 shows the structure of the external PI control loop. The assumption is made that the output of the PI control is actually iL_1, not iL_1^*, for analysis because, as shown in Eq. 7.19, iL_1 follows iL_1^* with a lag of T_s, which is sufficiently small and can be ignored. The system is s-transformed on the dq frame. The transfer function of the PI controller is then given by Eq. 7.20; i.e., the d and q axes currents are controlled by independent regulators.

$$G_{pi}(s) = \begin{bmatrix} K_p + {}^{K_i}/_{s} & 0 \\ 0 & K_p + {}^{K_i}/_{s} \end{bmatrix} \tag{7.20}$$

$G_{pi}(s) = V_{ab}(s)/I_{L2}(s)^2$ is the transfer function of the network formed by C, L_2 and the grid impedance.

7.6 SIMULINK Model of PLL Grid Connected Power System

A comparison of the hybrid Dαβ PLL to the other PLLs is necessary in order to demonstrate its advantages. The comparison focuses especially on Dαβ PLL and DSRF PLL which are the only ones that are able to operate accurately under unbalanced disturbances.

7.6.1 SIMULINK Model of a Synchronous Reference Frame PLL

The SIMULINK Model of a Synchronous Reference Frame PLL is shown in Fig. 7.35. The tuning parameters of a PI controller are selected as kp = 180 ki = 3,200 calculated using Ziegler-Nichols method.

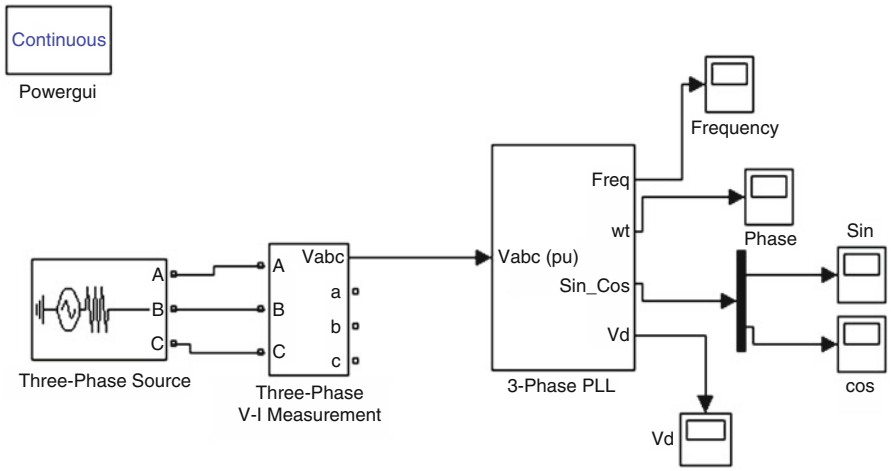

Fig. 7.35 SIMULINK model of a synchronous reference frame PLL

In the above SIMULINK diagram, the quadrature component of the voltage is taken for the frequency and hence the phase angle. The estimated phase angle is obtained by integrating the frequency. Practically this type of estimation results in $\theta = \text{infinity}$. As this type of design cannot be achieved in any discrete devices, the calculated value of the phase is made to fall between 0 and 2π using modulus operation.

7.6.1.1 Voltage and Phase Angle Tracked by SRF PLL

The output voltage Vd is obtained as 264.7 v for an input voltage of 325.26 v and the phase angle tracked by the SRF PLL is shown in Fig. 7.36.

7.6.2 SIMULINK Model of a Synchronous Reference Frame PLL During Unbalanced Fault

The SIMULINK Model of a Synchronous Reference Frame PLL during Unbalanced fault is shown in Fig. 7.37. Here an unbalanced fault is applied where there is a line to ground fault in two of the three phases.

7.6.2.1 Voltage and Phase Angle Tracked by SRF PLL During an Unbalanced Fault

The Voltage and Phase Angle Tracked by SRF PLL during an unbalanced fault are shown in Fig. 7.38.

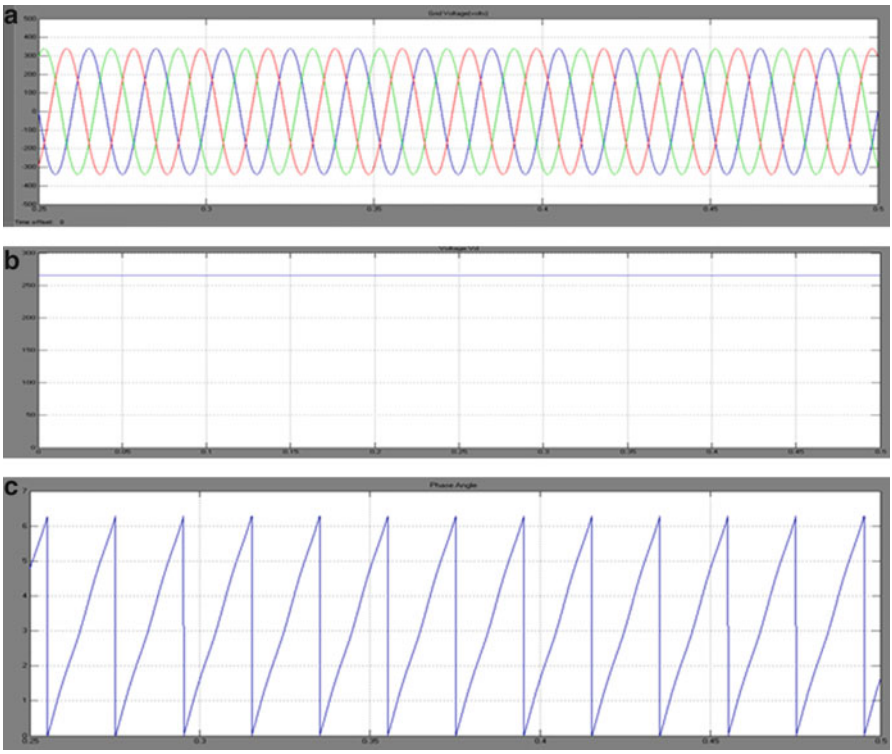

Fig. 7.36 (**a**) Grid voltage (**b**) voltage Vd obtained from PLL and (**c**) phase angle tracked by SRF PLL

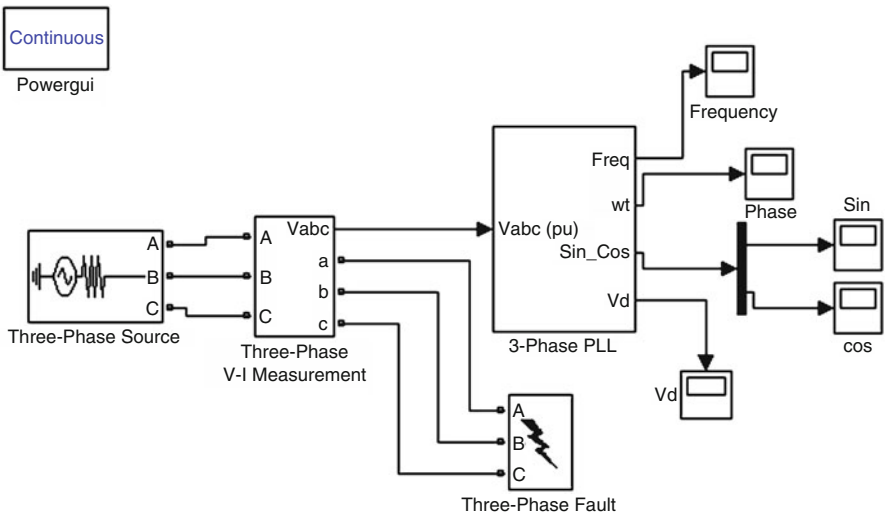

Fig. 7.37 SIMULINK model of a synchronous reference frame PLL during unbalanced fault

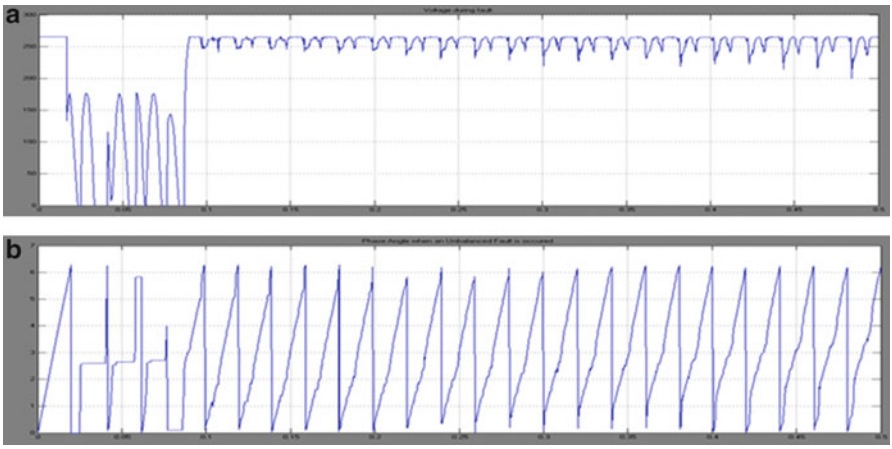

Fig. 7.38 (**a**) Voltage and (**b**) phase angle tracked by SRF PLL during an unbalanced fault

From the above two results, it is concluded that a synchronous reference frame PLL tracks the voltage and phase angle properly during normal conditions and under balanced faults

During an unbalanced fault, the voltage and phase angle are not tracked properly and are seen with many distortions.

7.6.3 SIMULINK Model of a DSRF PLL

The SIMULINK Model of a DSRF PLL is shown in Fig. 7.39. The tuning parameters of a PI controller are selected as $k_p = 2.2214$, $k_i = 246.74$ calculated using Ziegler-Nichols method.

7.6.3.1 Voltage and Phase Angle Tracked By DSRF PLL

The output voltage V_d, obtained as 420 V for an input voltage of 415 V, is shown in Fig. 7.40.

7.6.4 SIMULINK Model of a DSRF PLL Under an Unbalanced Fault

The SIMULINK Model of a DSRF PLL under an unbalanced fault is shown in Fig. 7.41. Here, an unbalanced fault is applied where there is a line to ground fault in two of the three phases.

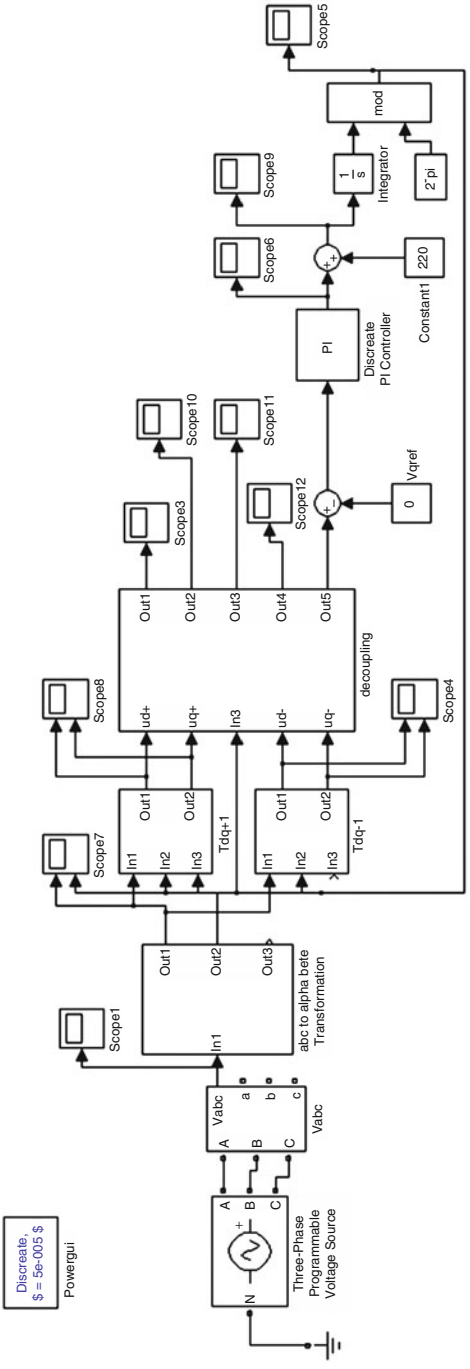

Fig. 7.39 SIMULINK model of a DSRF PLL

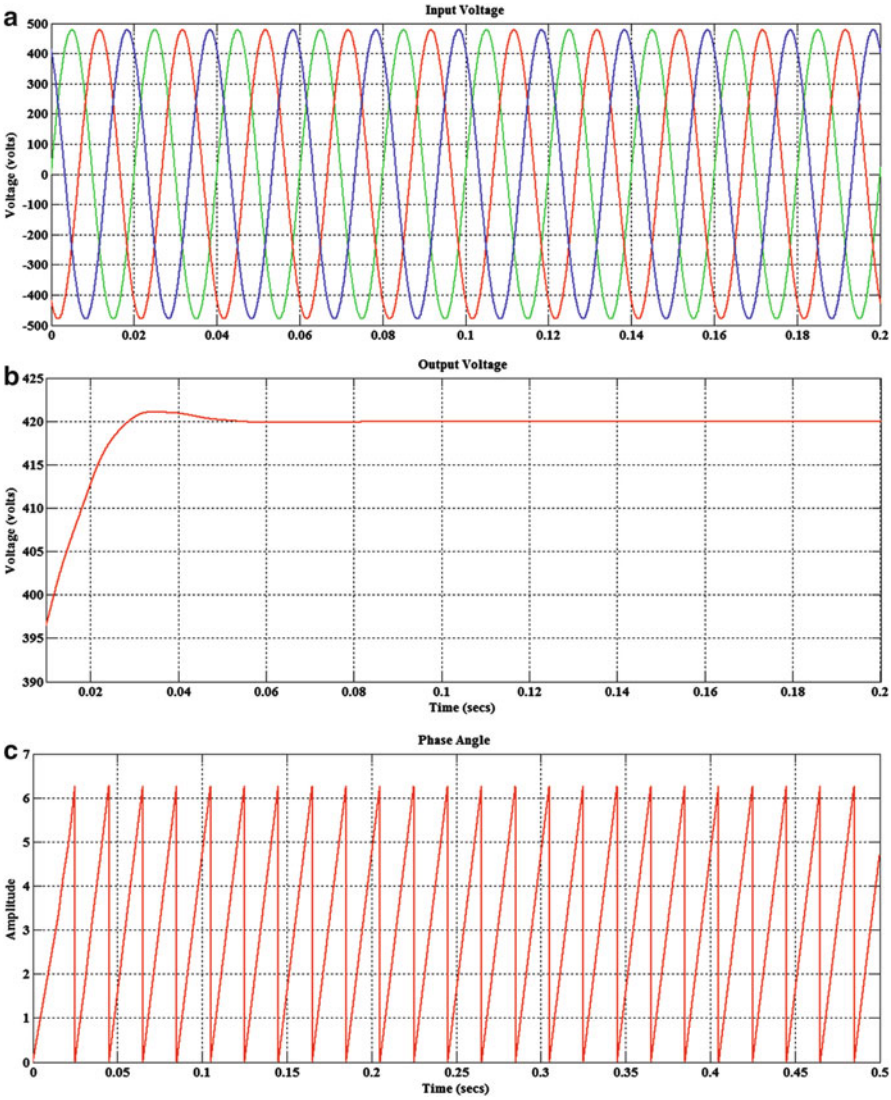

Fig. 7.40 Tracking by DSRF PLL – normal conditions (**a**) grid voltage (**b**) voltage V_d (**c**) phase angle

7.6.4.1 Voltage and Phase Angle Tracked By DSRF PLL During an Unbalanced Fault

The Voltage and Phase Angle Tracked by DSRF PLL during an unbalanced fault are shown in Fig. 7.42.

From the above results it is understood that when an unbalanced fault occurs, the DSRF PLL operates as same as under normal condition. Therefore it has an

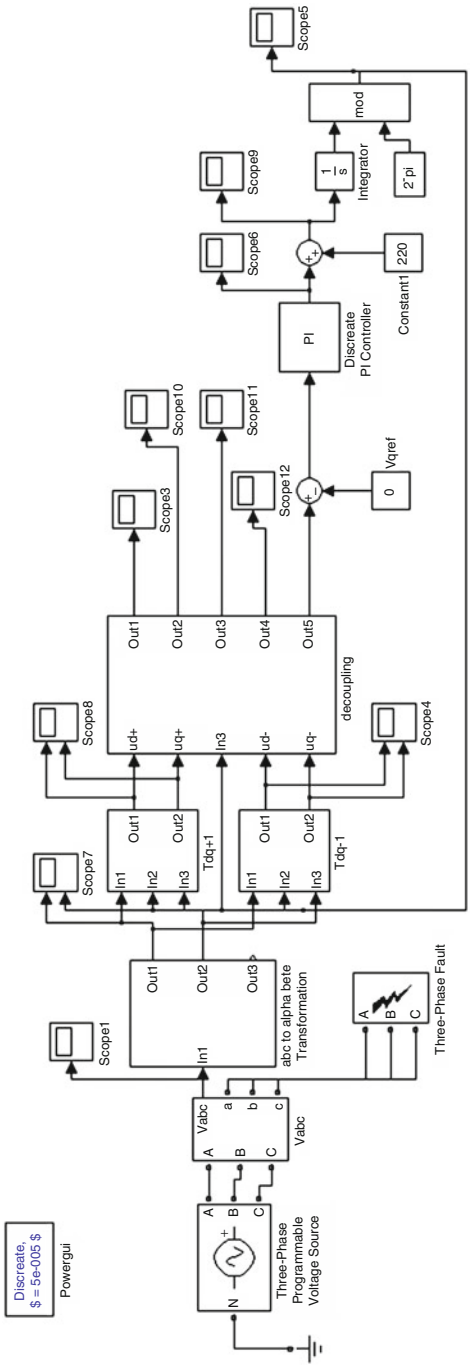

Fig. 7.41 SIMULINK model of a DSRF PLL under an unbalanced fault

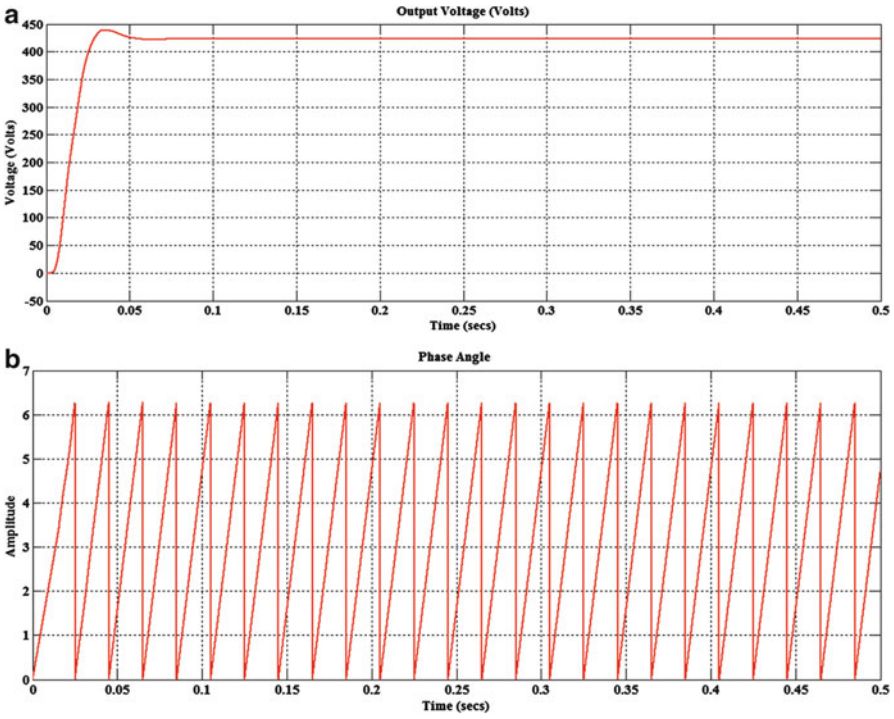

Fig. 7.42 Tracking by DSRF PLL -unbalanced fault (**a**) voltage (**b**) phase angle

improved result over the conventional dq PLL which cannot track the phase angle under fault conditions.

This is because of the decoupling of the positive and negative components present in the voltage and taking the positive component of the voltage as reference.

7.6.5 SIMULINK Model of αβPLL

The SIMULINK Model of an αβ Frame PLL is shown in Fig. 7.43. The tuning parametres of a PI controller are selected as kp = 180 ki = 3,200 calculated using Ziegler-Nichols method.

7.6.5.1 Voltage and Phase Angle Tracked by SRF PLL During an Unbalanced Fault

The voltage obtained by the PLL in d-q frame is shown in Fig. 7.44. The input voltage to the PLL is 325.26 V.

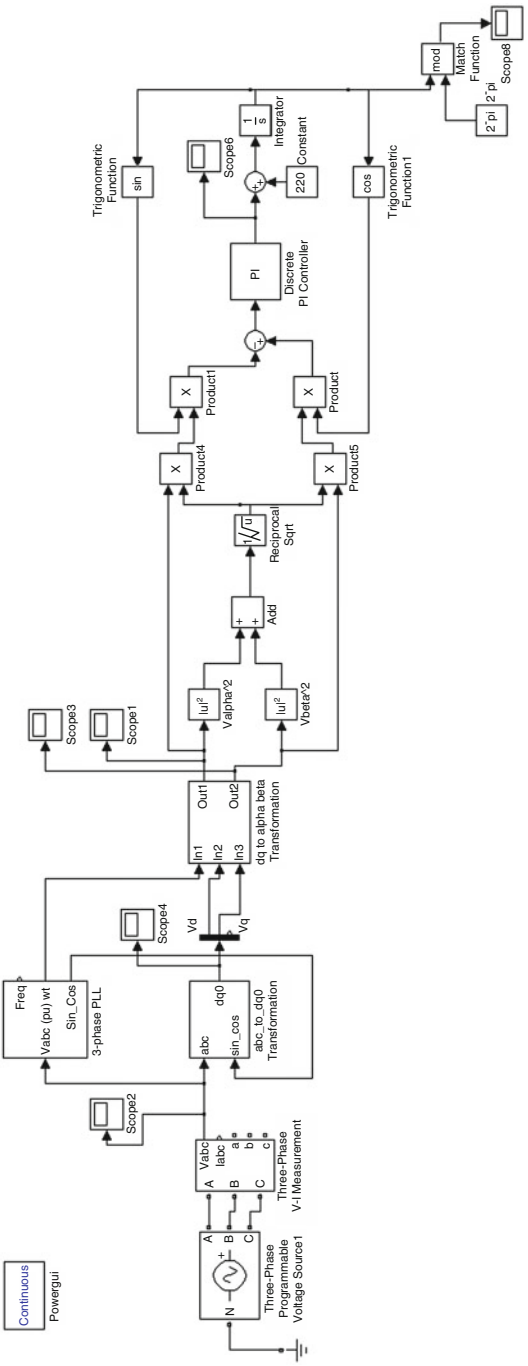

Fig. 7.43 SIMULINK model of an αβ PLL

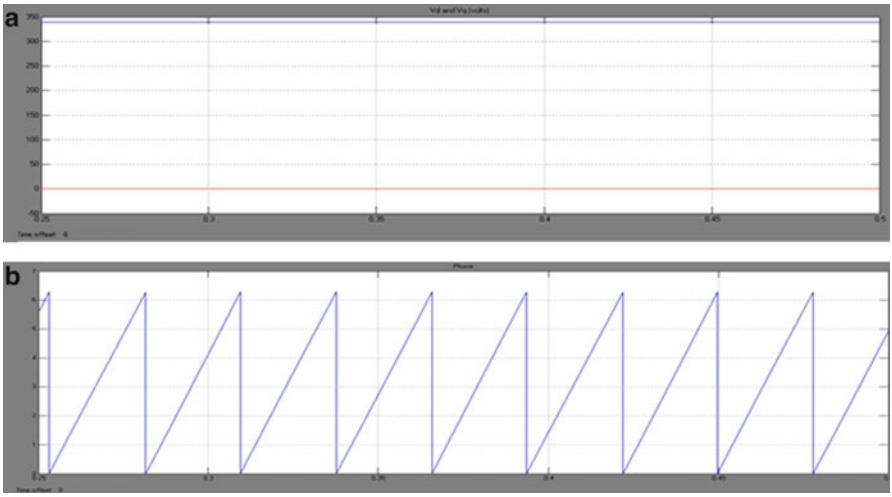

Fig. 7.44 (**a**) Voltage and (**b**) phase angle tracked by αβ PLL

7.6.6 SIMULINK Model of a αβPLL During Unbalanced Fault

The SIMULINK Model of a αβPLL during Unbalanced fault is shown in Fig. 7.45. Here an unbalanced fault is applied where there is a line to ground fault in two of the three phases.

7.6.6.1 Phase Angle Tracked by αβ PLL During an Unbalanced Fault

The phase angle tracked by αβ PLL during an unbalanced fault is shown in Fig. 7.46.

From the above two results, it can be inferred that the αβ PLL also exhibits the same behavior as that of the synchronous reference frame PLL. It also has a disturbed phase when an unbalanced fault occurs.

The advantage of the αβ PLL over the SRF PLL is that the peak over shoot in the phase angle tracked is less.

7.6.7 SIMULINK Model of a Dαβ PLL

The SIMULINK Model of a Decoupled αβ PLL (Dαβ PLL) is shown in Fig. 7.47. The tuning parameters of a PI controller are selected as $k_p = 180$, $k_i = 3{,}200$ calculated using Ziegler-Nichols method.

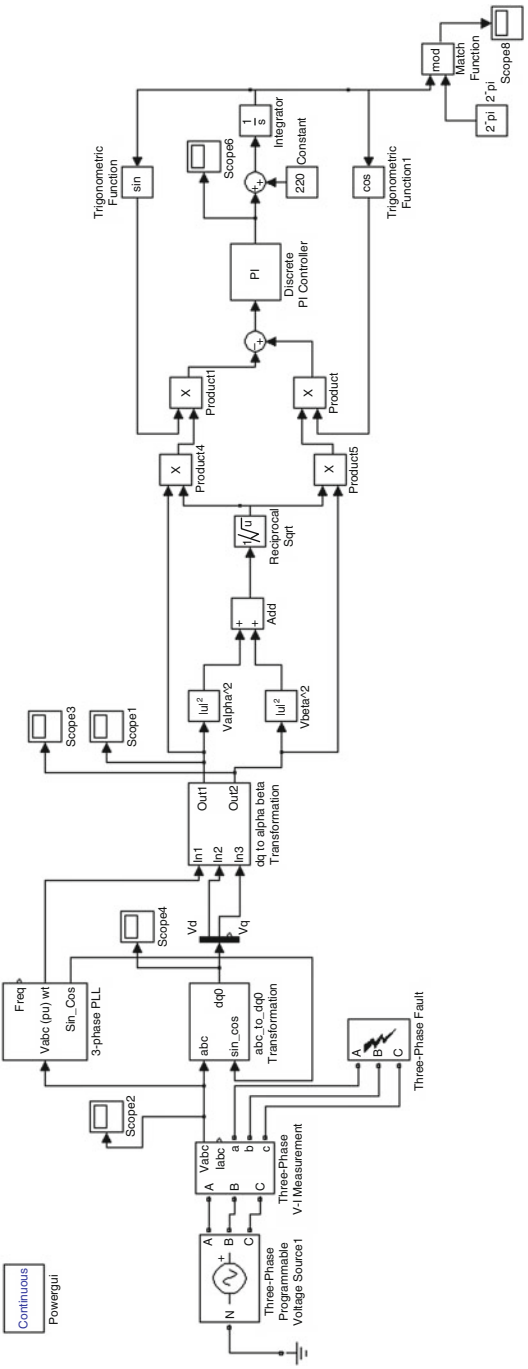

Fig. 7.45 SIMULINK model of an αβ PLL under an unbalanced fault

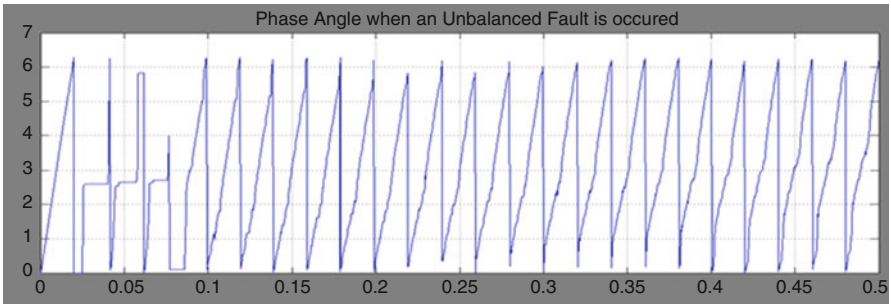

Fig. 7.46 Phase angle tracked by αβ PLL under an unbalanced fault

7.6.7.1 Voltage and Phase Angle Tracked Using Dαβ PLL

The Voltage and Phase angle tracked using Dαβ PLL is shown in Fig. 7.48. The output voltage V_d is 423.3 V for an input voltage of 415 V.

7.6.8 SIMULINK Model of a Dαβ PLL Under an Unbalanced Fault

The SIMULINK Model of a Decoupled αβ PLL (Dαβ PLL) under an Unbalanced Fault is shown in Fig. 7.49. Here an unbalanced fault is applied where there is a line to ground fault in two of the three phases.

7.6.8.1 Voltage and Phase Angle Tracked Using Dαβ PLL Under Unbalanced Fault

The Voltage and Phase angle tracked using Dαβ PLL under Unbalanced Fault are shown in Fig. 7.50.

From the above results it is found out that, the Dαβ PLL also efficiently tracks the phase even under unbalanced conditions.

The main difference between the DSRF PLL and Dαβ PLL is the peak overshoot that appears in the phase angle. The peak over shoot of DSRF PLL is more than that of the Dαβ PLL which is undesirable. The frequency response of two PLLs is shown in the Fig. 7.51.

Hence this PLL model has the better performance when compared to the other PLLs that are investigated under normal and unbalanced conditions.

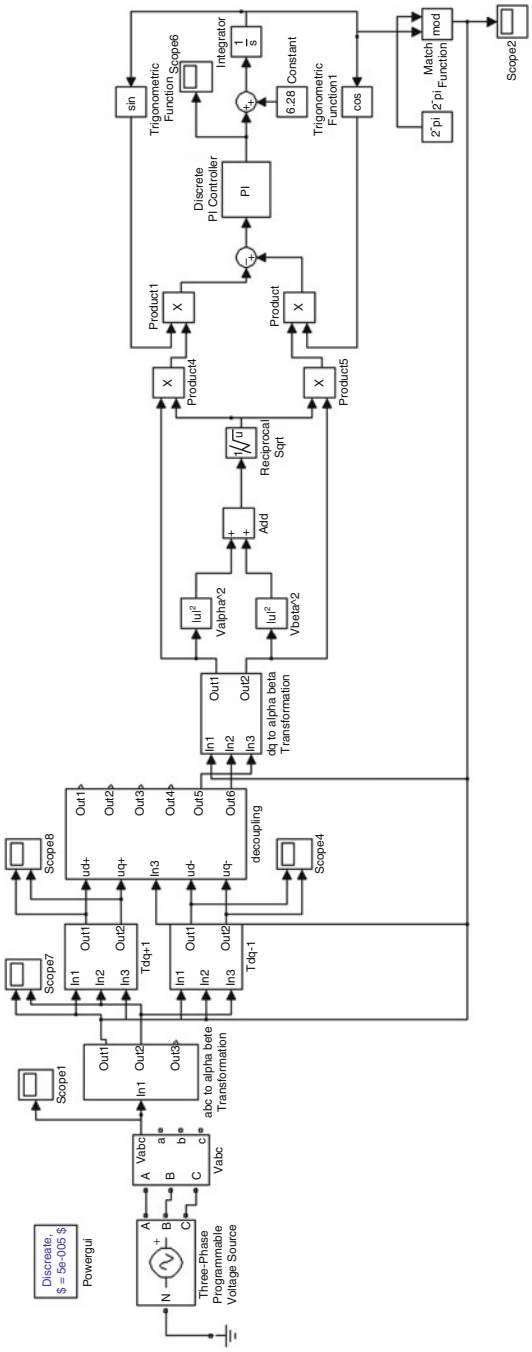

Fig. 7.47 SIMULINK model of a Dαβ PLL

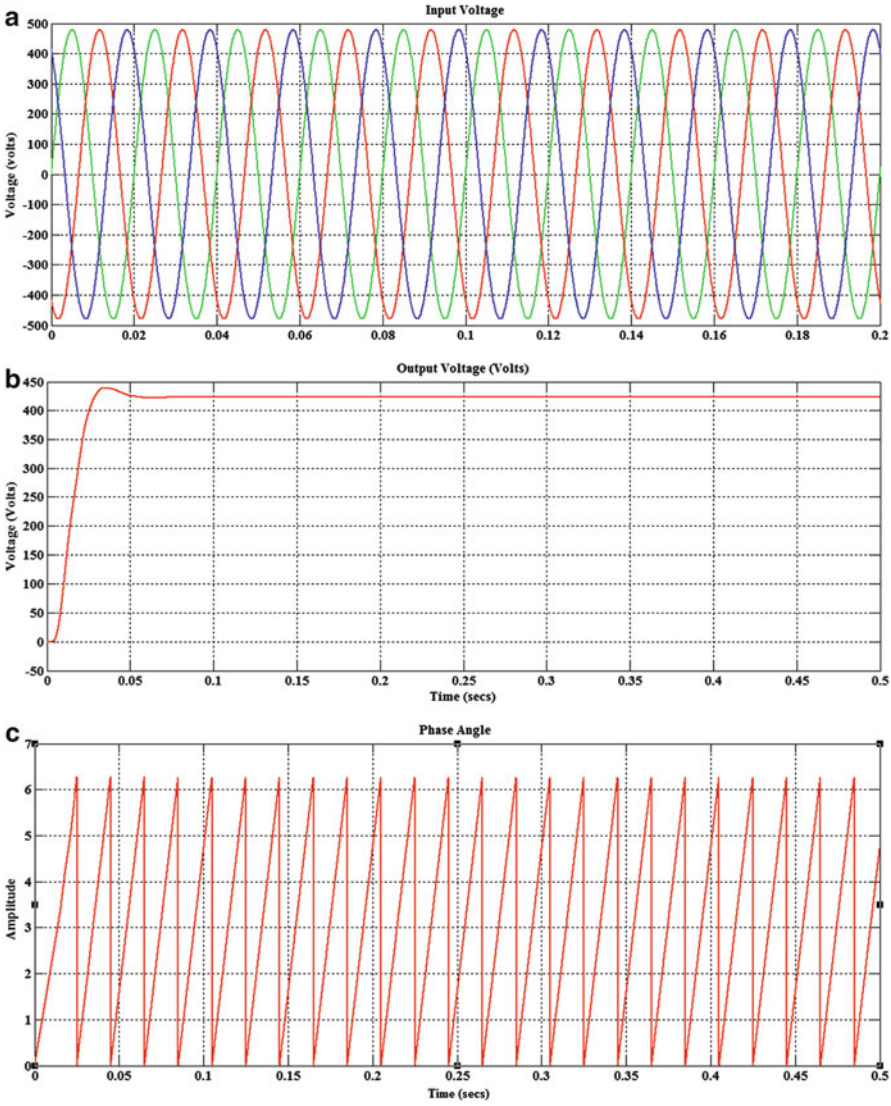

Fig. 7.48 Tracking by a Dαβ PLL – normal conditions (**a**) grid voltage (**b**) voltage (**c**) phase angle

7.6.9 SIMULINK Model of a Decoupled Double Synchronous Reference Frame PLL(DDSRF PLL)

The SIMULINK Model of a Decoupled Double Synchronous Reference Frame PLL(DDSRF PLL) is shown in Fig. 7.52. The tuning parameters of a PI controller are selected as kp = 2.2214 ki = 246.74 calculated using Ziegler-Nichols method.

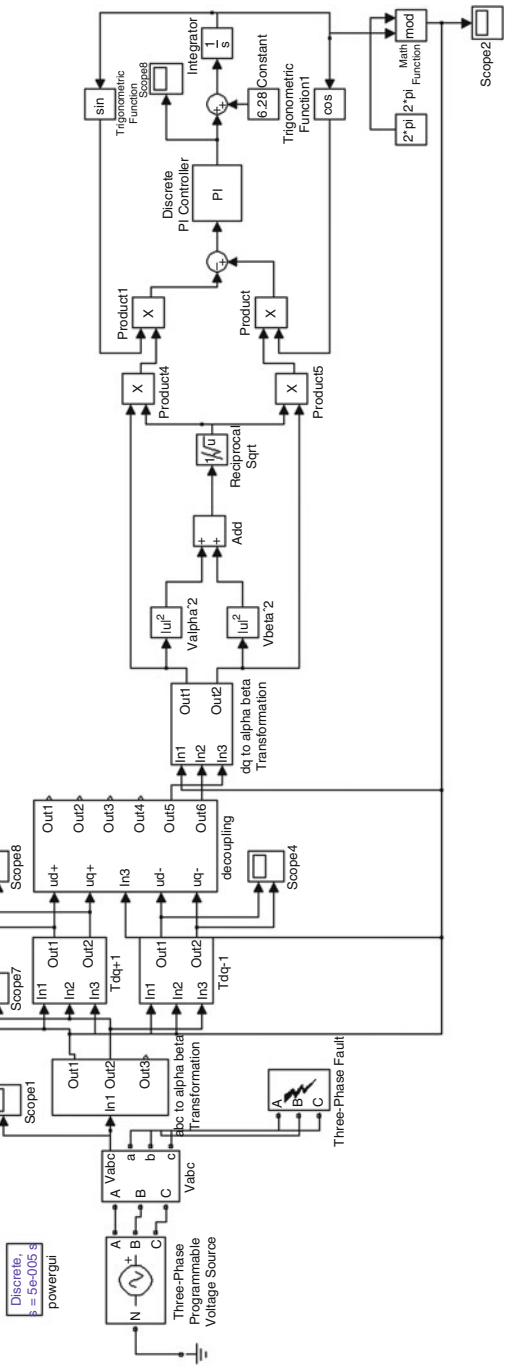

Fig. 7.49 SIMULINK model of a Dαβ PLL under unbalanced fault

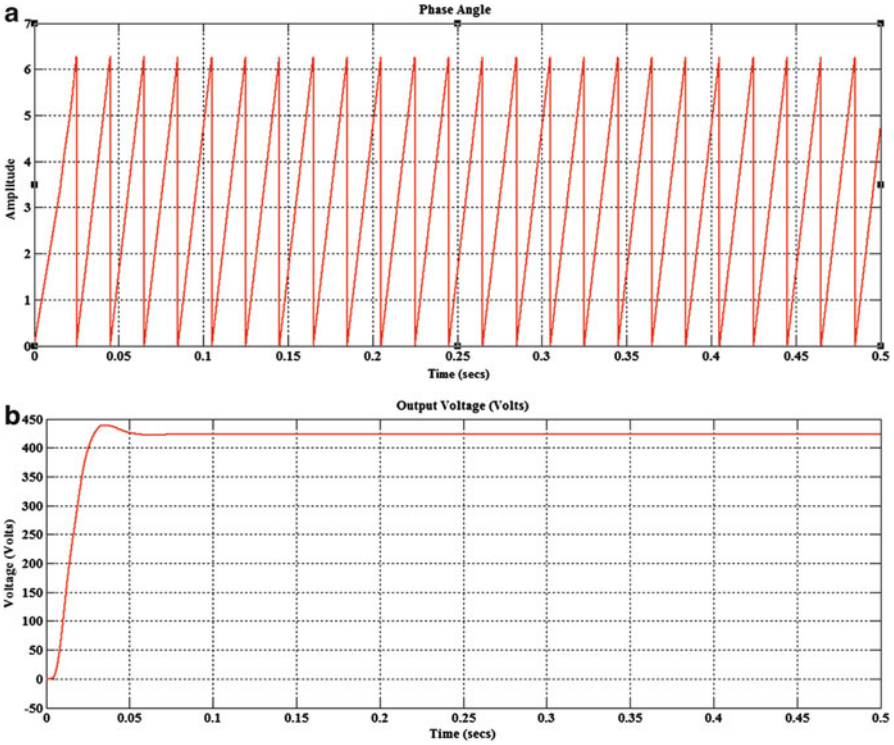

Fig. 7.50 Tracking by a Dαβ PLL -unbalanced fault (**a**) voltage (**b**) phase angle

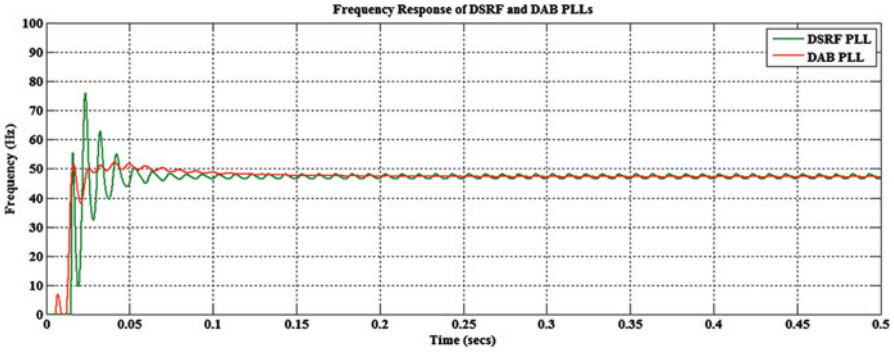

Fig. 7.51 Frequency response of DSRF and Dαβ PLLs

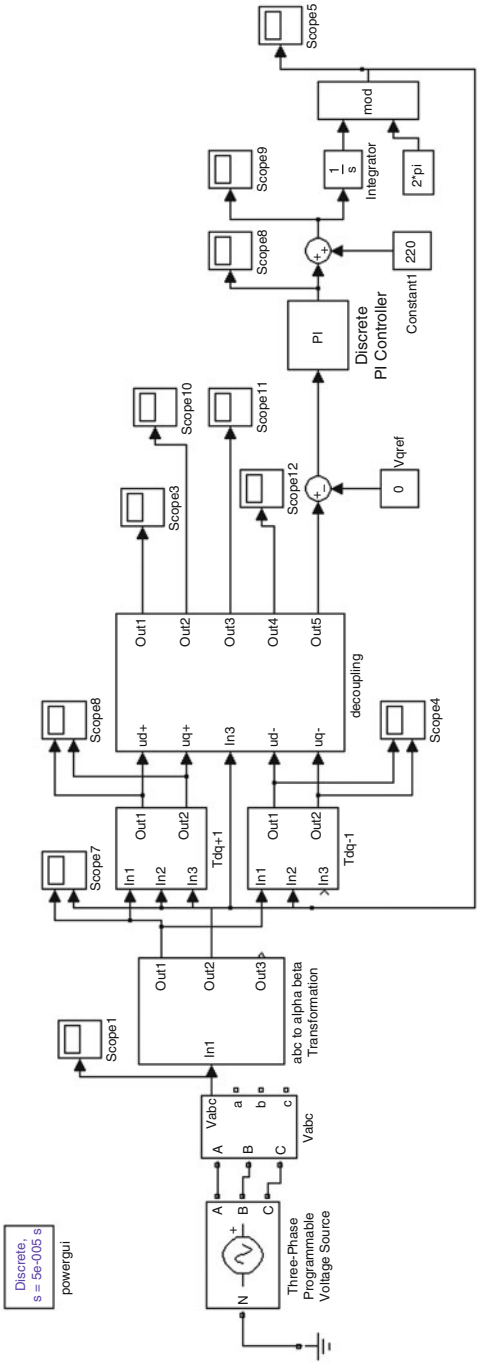

Fig. 7.52 SIMULINK model of a decoupled double synchronous reference frame PLL(DDSRF PLL)

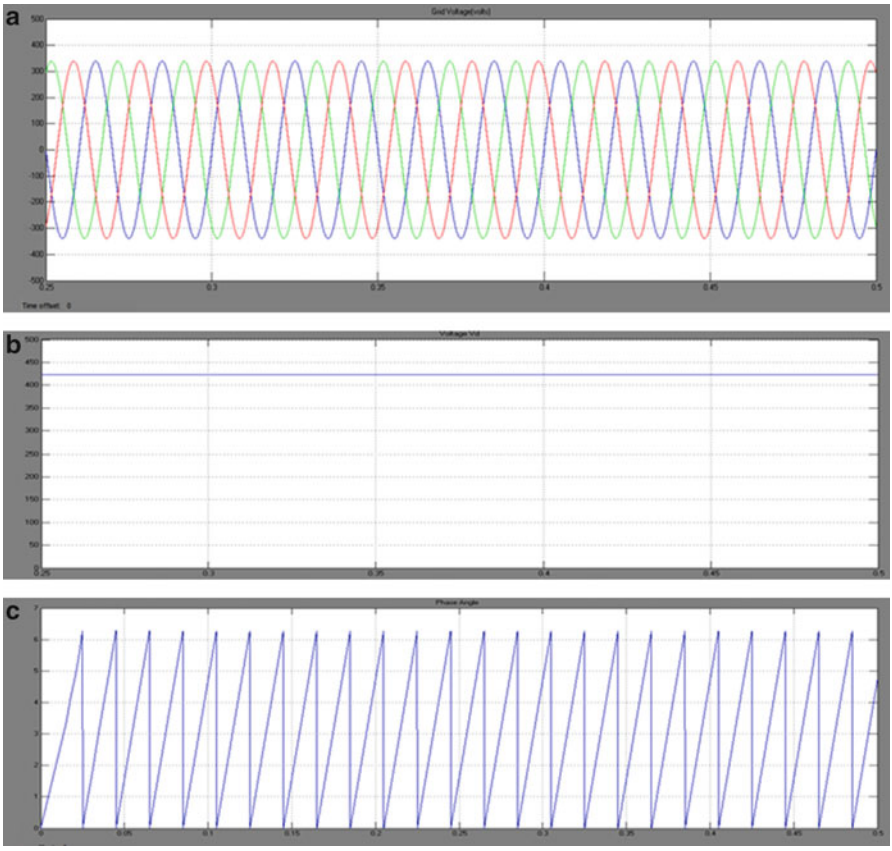

Fig. 7.53 (**a**) Grid voltage (**b**) voltage Vd and (**c**) phase angle tracked by DDSRF PLL

7.6.9.1 Voltage and Phase Angle Tracked by DDSRF PLL

The output voltage Vd is obtained as 423.3 v for an input voltage of 415 V is shown in Fig. 7.53.

7.6.10 SIMULINK Model of a DDSRF PLL During an Unbalanced Fault

The SIMULINK Model of a DDSRF PLL during an Unbalanced fault is shown in Fig. 7.54. Here an unbalanced fault is applied where there is a line to ground fault in two of the three phases.

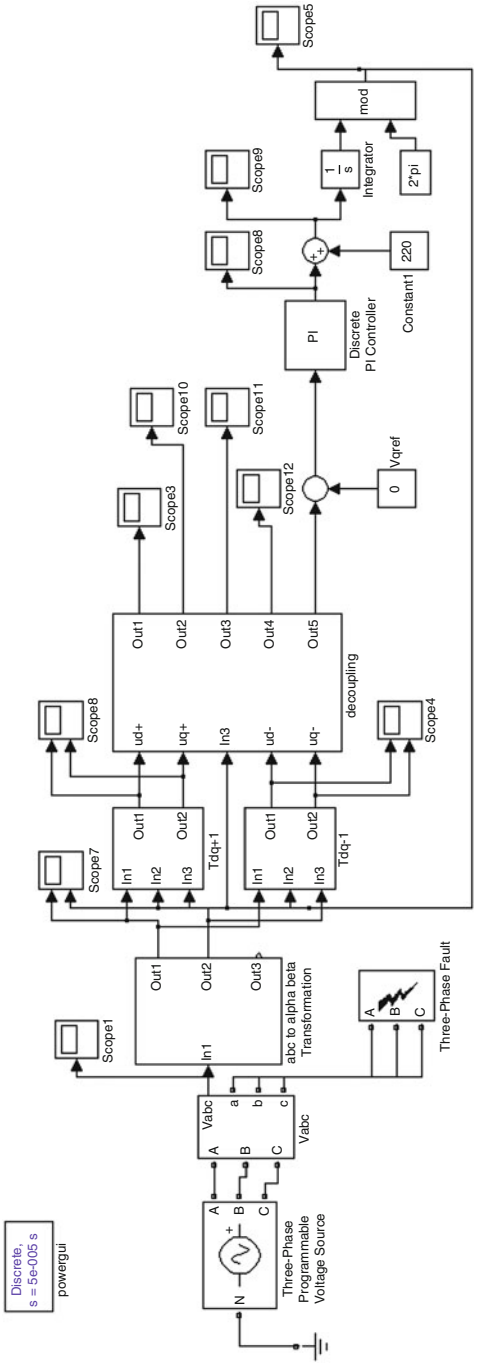

Fig. 7.54 SIMULINK model of a decoupled double synchronous reference frame PLL(DDSRF PLL) under an unbalanced fault

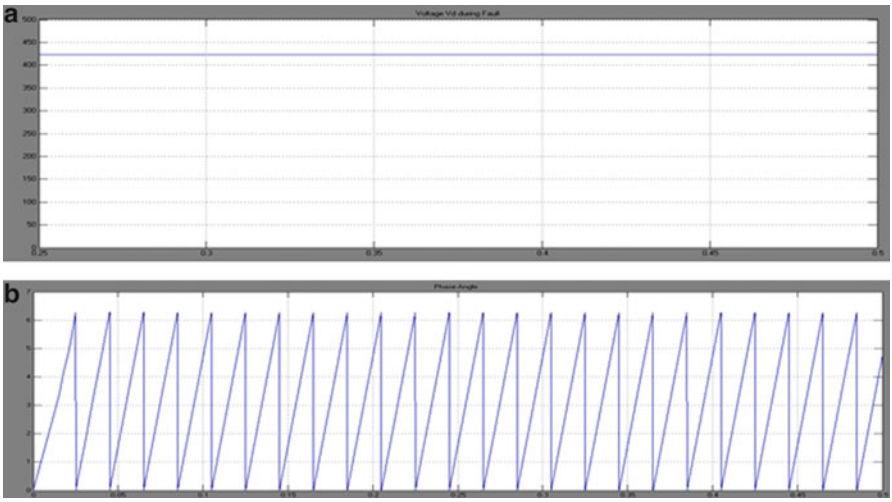

Fig. 7.55 (**a**) Voltage and (**b**) phase angle tracked by DDSRF PLL during an unbalanced fault

7.6.10.1 Voltage and Phase Angle Tracked by DDSRF PLL During an Unbalanced Fault

The Voltage and Phase Angle Tracked by DDSRF PLL during an unbalanced fault are shown in Fig. 7.55.

From the above results it is understood that when an unbalanced fault occurs, the DDSRF PLL operates as same as under normal condition. Therefore it has an improved result over the conventional SRF PLL which cannot track the phase angle under fault conditions. This is due to the decoupling of the positive and negative components present in the voltage and taking the positive component of the voltage as reference.

7.6.11 SIMULINK Diagram of Grid Synchronization of the Inverter Using the Hybrid Dαβ PLL

The hybrid Dαβ PLL is used to synchronize the inverter to grid using a current controller. The SIMULINK diagram is shown in Fig. 7.56. The current controller uses normal PI controller. To simulate the operation of the current control, a reference input active current Id whose amplitude is 2A is applied. Then followed by a reactive current reference component step Iq whose amplitude also is 2A. The simulated output inverter current of the inverter model is shown in Fig. 7.57. In this figure the output inverter current reaches its steady state value of 2A, which is exactly equal to the reference value. This proves that the current loop controller is

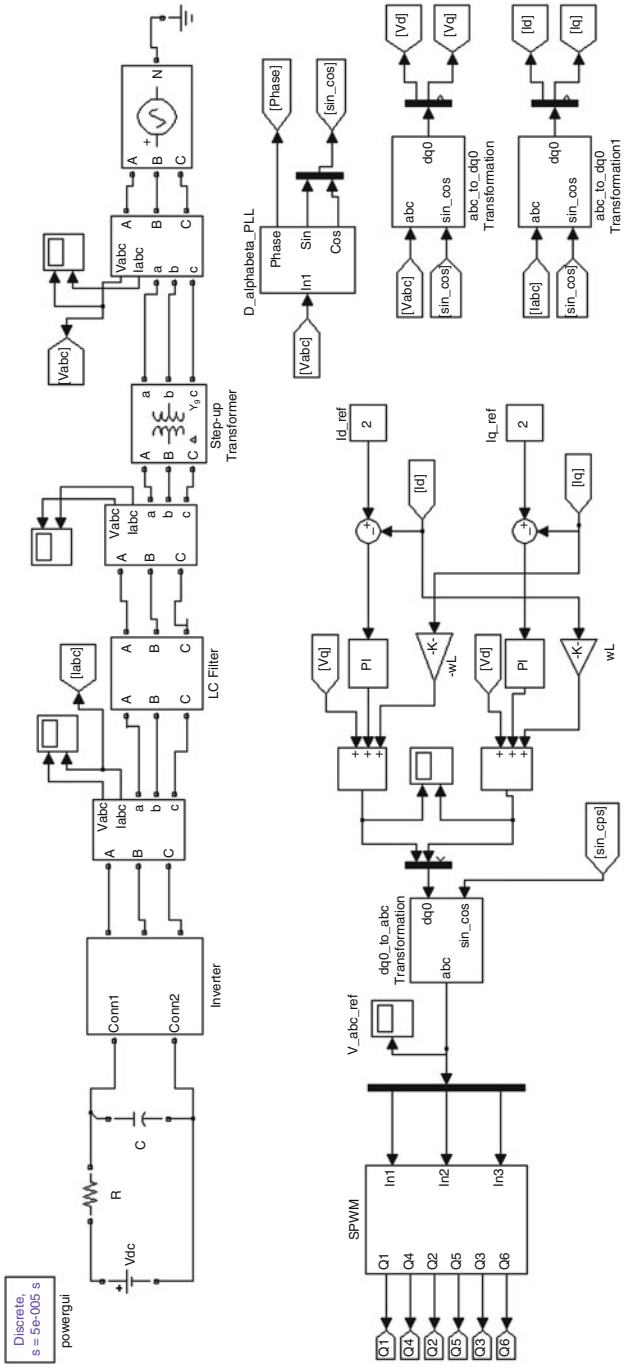

Fig. 7.56 Grid synchronization of the inverter using the hybrid PLL

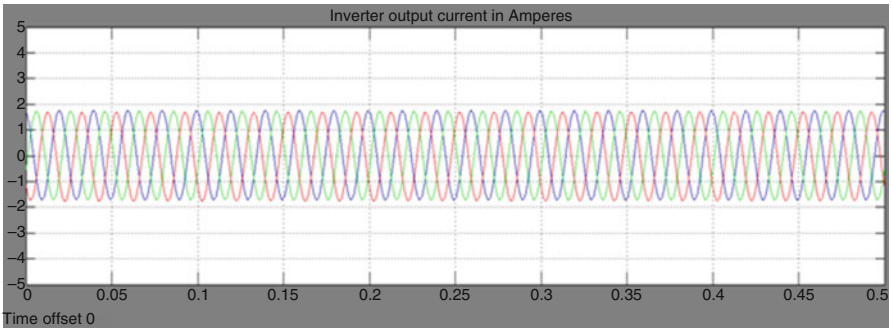

Fig. 7.57 Synchronized inverter output current in Amperes

effective such that measured currents track their references. In addition, its dynamic behavior is satisfactory.

The synchronized inverter output current is shown in Fig. 7.57. The current magnitude is almost near to that of the reference value 2A.

Thus, using the hybrid PLL the inverter is successfully synchronized to the grid.

7.6.12 SIMULINK Model of SRF PI Controlled Voltage Source Inverter

The SIMULINK model of the three phase grid connected inverter using a SRF PI controller is shown in Fig. 7.58. The above model consists of a SPWM inverter whose supply is assumed as a constant DC voltage (here 400 V). A LCL filter is connected at the output side of the inverter to attenuate the high frequency harmonics. Then the harmonic free current obtained from the inverter is given to the grid via step up transformer whose configuration is (delta-wye). A three phase programmable voltage source (available in Simpowersystems) is used as a three phase grid of 415 V. The Dαβ PLL is used to calculate the phase angle using the grid voltage.

The inverter output voltage and current is shown in Fig. 7.59.

7.6.13 SIMULINK Diagram of Grid Synchronization of the Inverter Using Cascaded Deadbeat and PI Controller

The SIMULINK model of the three phase Grid-connected inverter using a Deadbeat controller is shown in Fig. 7.60. The above model consists of a SPWM inverter whose supply is assumed as a constant DC voltage (here 400 V). A LCL filter is

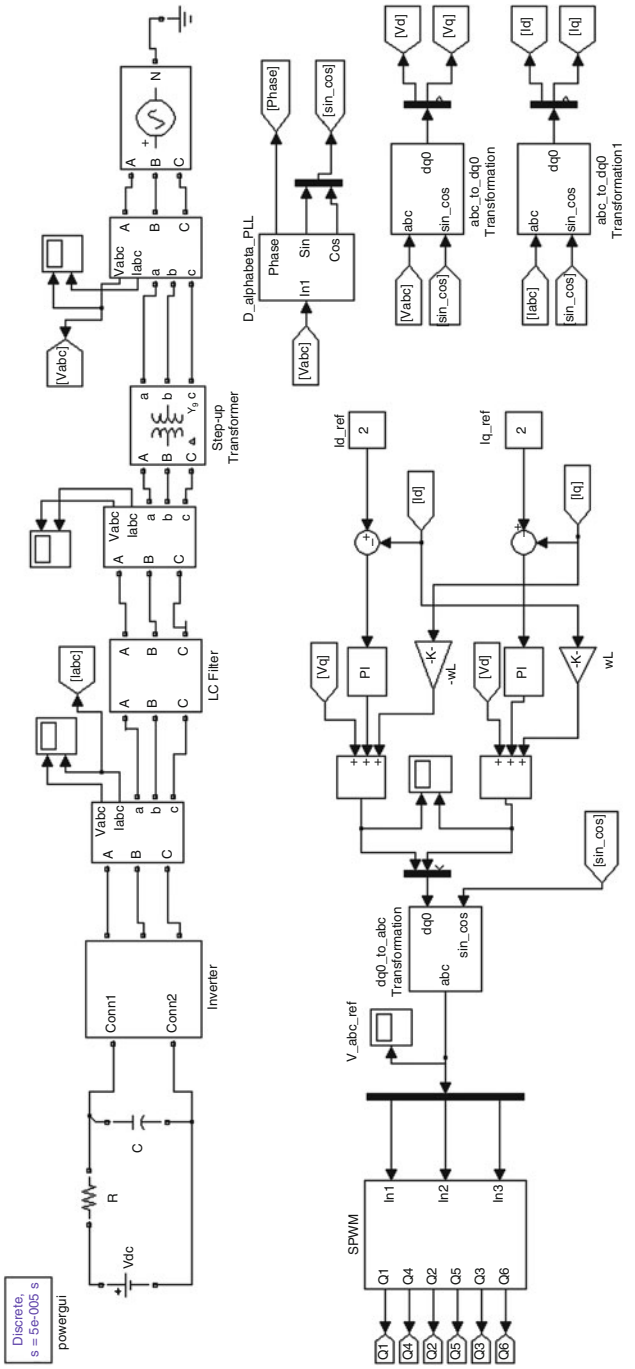

Fig. 7.58 SIMULINK diagram of a grid-connected inverter using SRF PI controller

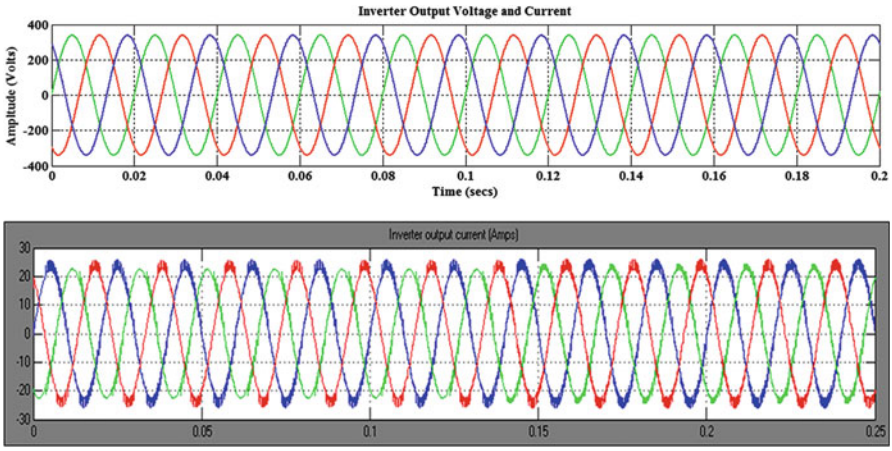

Fig. 7.59 Inverter output voltages and currents using SRF PI controller

connected at the output side of the inverter to attenuate the high frequency harmonics. Then the harmonic free current obtained from the inverter is given to the grid. A three phase programmable voltage source (available in Simpowersystems) is used as a three phase grid of 415 V. The Dαβ PLL is used to calculate the phase angle using the grid voltage and the plots are shown in Fig. 7.61.

7.6.14 Comparison of Current THD of SRF PI and Cascaded Deadbeat and PI Controllers

The THD Analysis of output inverter current of SRF PI controller is shown in Fig. 7.62. The THD is shown as 6.68 %.

The THD Analysis of output inverter current of the Deadbeat controller is shown in Fig. 7.63. The THD is shown as 0.02 %.

The above analysis shows that the cascaded Deadbeat and PI controller is more effective for integrating the inverter with the grid when compared to the SRF PI controller as the harmonics are almost negligible in the Cascaded Controller.

A benchmarking study of the effect of the time response on the overshoot of the estimated frequency and phase angle for three different PLLs is performed in this section. The investigation of dqPLL, αβPLL and ddsrfPLL motivates the proposal for a new PLL, which inherits the advantages of each PLL. The new hybrid dαβPLL is the most beneficial solution for grid synchronization compared to the other three PLLs under investigation, since it operates accurately under balanced and unbalanced conditions and also reduces the overshoot on the estimation of the phase angle and frequency, which is the main drawback of DDSRF PLL. The lower frequency overshoot of dαβPLL leads to a faster time response without any violation of the frequency limits of the grid codes. The hybrid dαβPLL could be

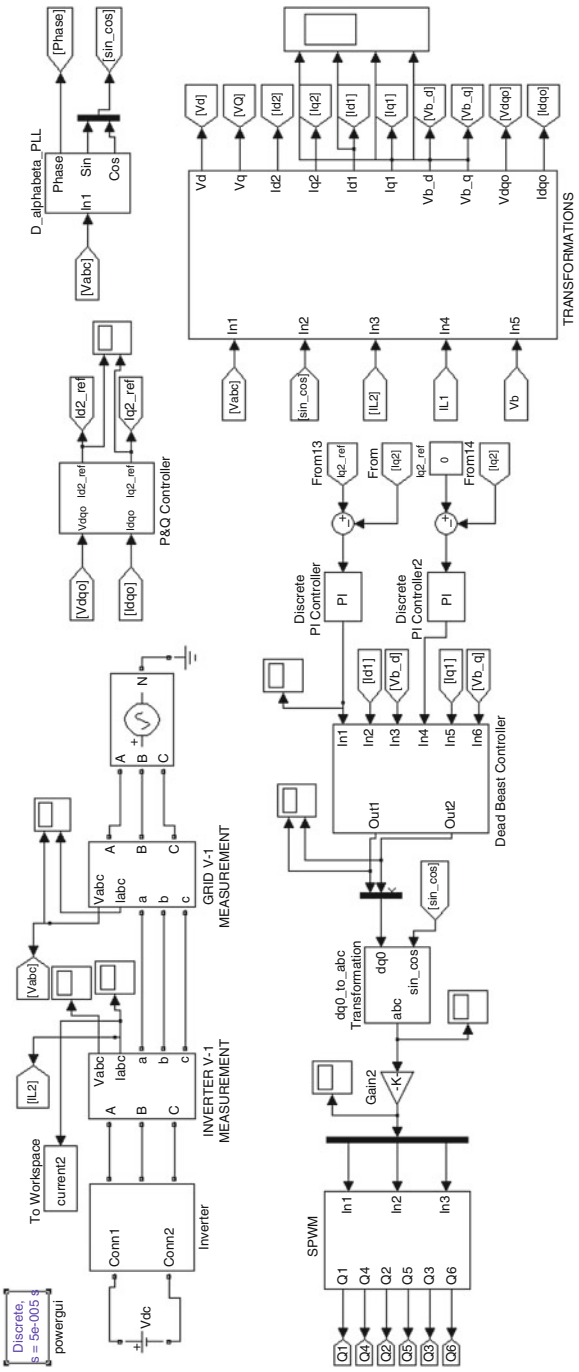

Fig. 7.60 SIMULINK diagram of a grid-connected inverter using cascaded deadbeat and PI controller

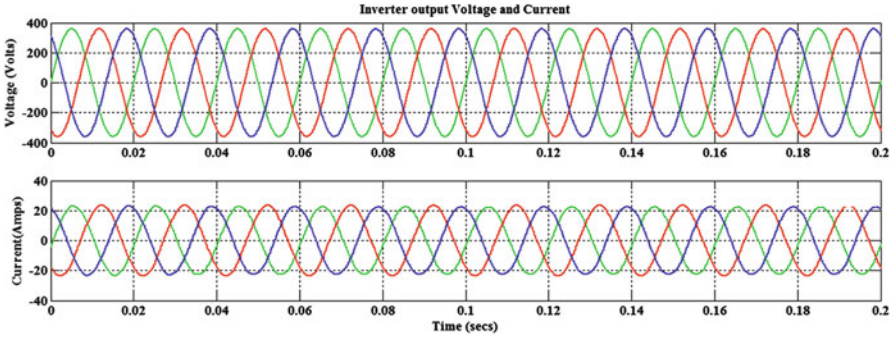

Fig. 7.61 Inverter output voltages and currents using cascaded deadbeat and PI controller

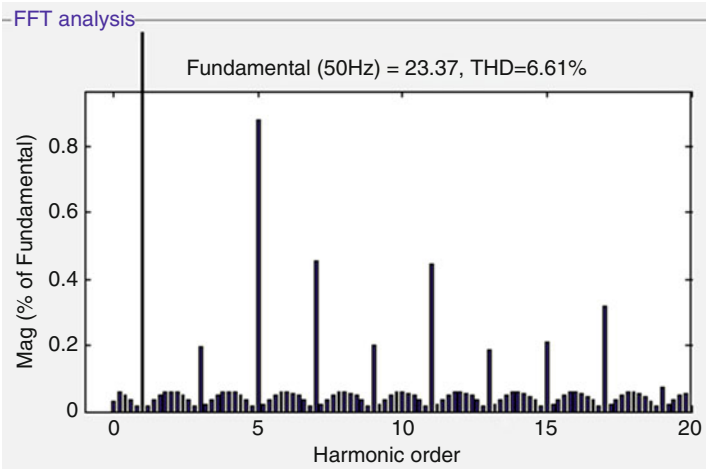

Fig. 7.62 THD analysis of SRF PI controller

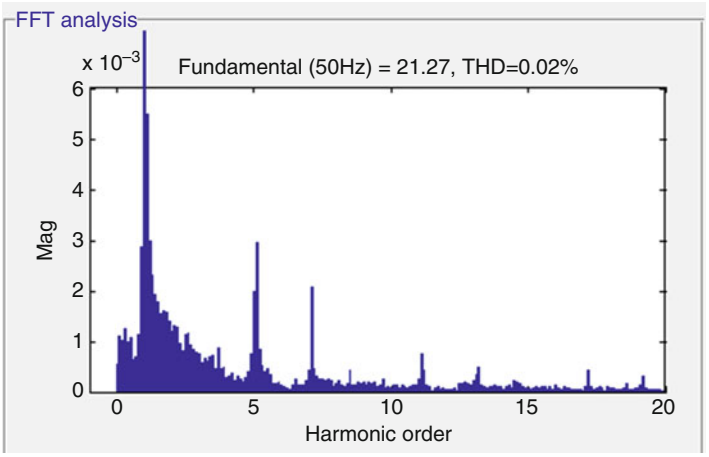

Fig. 7.63 THD analysis of cascaded deadbeat and PI controller

very useful in synchronizing the inverter to the grid. The performance of the dαβPLL in DGS is verified through results and its use is illustrated. Two control algorithms Synchronous PI control and Cascaded Dead-Beat and PI for the inverter-based DGS interface, in the Grid-connected and operation have been presented and compared in this project. The cascaded deadbeat and PI control algorithm is found appropriate to realize a robust DGS interface that guarantees stable and high power quality injection under the challenging uncertain nature of distribution systems. The Modeling and control of utility interactive inverters can be done more efficiently using the State of the art techniques that are available for Grid synchronization, anti-islanding control and current regulation. Control algorithms can be given in digital control format applicable to embedded control using digital signal processors.

7.7 Summary

Integration of renewable energy system to the grid and various problems and challenges that need to be addressed are discussed. Protection, voltage control and power quality are the major concerns related to the interconnection of the small scale renewable energy generation at the distribution level. Grid Issues in integrating renewable energy systems, converters used for grid integration techniques and its control strategy are discussed in this chapter. MATLAB/SIMULINK models of Synchronous Reference Frame PLL (dq PLL), Stationary Reference Frame PLL (αβ PLL), Decoupled Synchronous Reference Frame PLL (DSRF PLL), Decoupled Stationary Reference frame PLL (Dαβ PLL) and Hybrid Dαβ PLL are developed and the results are presented. Filters used for grid integration techniques and its control strategy is also explained in this chapter.

Review Questions

1. List the different types of interfacing technology used between renewable energy systems and grid unit.
2. What are the challenges involved in grid integration of renewable energy sources?
3. State the grid Interconnection standards.
4. Discuss the challenges imposed on an Inverter-Based DG Interface.
5. Mention the requirements for establishing a Grid Connection using PLL.
6. Discuss Grid Synchronization of Inverter Using Cascaded Deadbeat and PI Controller.
7. What are the advantages of using LCL filter in grid systems?
8. Mention the role of damping resistance in LCL filter.
9. Differentiate between SRF and DSRF PLL in Grid connected inverters.

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